élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

1994 Data Book

SALES OFFICES

EAST
Elantec, Inc.
Mark 128 Office Park
140 Wood Road, Suite 104
Braintree, MA 02184
Telephone: (617) 849-9181
Fax: (617) 849-0285

WEST
Elantec, Inc.
1996 Tarob Court
Milpitas, CA 95035
Telephone: (408) 945-1323
Fax: (408) 945-9305
800-333-6314

EUROPE
Elantec, Inc.
Gordon House Business Centre
First Floor
6 Lissenden Gardens
London NW5 1LX
Telephone: 44-71-482-4596
Fax: 44-71-207-1026

ASIA
Elantec, Inc.
Raffine Maison,
Nakano #401
2-7-2 Arai,
Nakano-Ku
Tokyo, Japan T165
Telephone: 81-3-3388-6959
Fax: 81-3-3388-6956

FACTORY

Elantec, Inc.
1996 Tarob Court
Milpitas, CA 95035
Telephone: (408) 945-1323
Fax: (408) 945-9305

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US Patent Numbers: 4,746,877 • 4,827,223 • 4,837,523 • 4,833,424 • 4,935,704 • 4,910,477 • 5,128,564 • 4,878,034 • 4,963,802 • 5,179,355

UK Patent Numbers: 2217135 • 2217134

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Amplifiers

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

*Listed in order of decreasing bandwidth

ELANTEC Part Number	Description	Temp. Range	Min. A_{VOL} over Temp.	Max. Offset Voltage		Max. Bias Current		*Gain Bandwidth Product Typical @ A_V = xx (or f_{3dB})	Min. Slew Rate 25°C (Comp for A_V = xx)	Continuous Output Current	Max. I_{CC} (Full Temp.)	Packages
				25°C	Over Temp.	25°C	Over Temp.					
EL2075C	Monolithic 2 GHz GBWP, Voltage Mode Feedback, Gain of ≥ 10 Stable, ±5V Supplies	0 to +75°C	1500V/V @25°C	1.5 mV	2.5 mV	3.5 μA	6.0 μA	2 GHz (A_V = 20)	350 V/μs (A_V = 10)	±56 mA Min.	25 mA	8-Pin P-DIP, 8-Lead SO
EL2038C	1 GHz GBW Op-Amp Monolithic, C.B. Gain of 20V/V @ 50 MHz	0°C to +75°C	74 dB	4 mV	6 mV	20 μA	25 μA	1000 MHz (A_V = 20)	1000 V/μs (A_V = 20)	±25 mA Min.	17 mA	14-Pin P-DIP
EL2039C	600 MHz GBW, Monolithic Gain of 10 Stable, C.B. Improved Replacement for HA2539	0°C to +75°C	74 dB	2 mV	6 mV	20 μA	25 μA	600 MHz (A_V = 10)	550 V/μs (A_V = 10)	±25 mA Min.	17 mA	14-Pin P-DIP
EL2223C EL2224C	Monolithic, C.B., Dual 500 MHz GBW Gain of 10 Stable Upgrade Dual EHA2540, EL2040	0°C to +75°C	80 dB	5 mV	8 mV	4 μA	6 μA	500 MHz (A_V = 10)	250 V/μs (A_V = 10)	±50 mA Typ.	13 mA	8-Pin P-DIP, 20-Pin SOL
EL2423C EL2424C	Quad, Monolithic, C.B. 500 MHz GBW, Gain of 10 Stable	0°C to +75°C	80 dB	6 mV	10 mV	4 μA	6 μA	500 MHz (A_V = 10)	250 V/μs (A_V = 10)	±10 mA Min.	18 mA	14-Pin P-DIP
EL2074C	Monolithic, 400 MHz GBWP, Voltage Mode Feedback, Gain of ≥ 2 Stable, ±5V Supplies	6°C to +75°C	500 V/V @25°C	1.5 mV	2.5 mV	3.5 μA	6.0 μA	400 MHz (A_V = 2)	350 V/μs (A_V = 2)	±56 mA Min.	25 mA	8-Pin P-DIP, 8-Lead SO
EL2040C	400 MHz GBW, Monolithic Gain of 10 Stable, C.B. Improved Replacement for HA2540	0°C to +75°C	74 dB	2 mV	6 mV	20 μA	25 μA	400 MHz (A_V = 10)	350 V/μs (A_V = 10)	±25 mA Min.	17 mA	14-Pin P-DIP
EL2073C	Monolithic, 200 MHz GBWP, Voltage Mode Feedback, Unity Gain Stable, ±5V Supplies	0°C to +75°C	500 V/V @25°C	1.5 mV	3.0 mV	3.5 μA	6.0 μA	300 MHz (A_V = +1)	175 V/μs (A_V = 1)	±50 mA Min.	25 mA	8-Pin P-DIP, 8-Lead SO
EL400C	Monolithic, C.B., 200 MHz Unity Gain Stable Amplifier, ±5V Supplies	−40°C to +85°C	125 KV/A (Typ.)	5.5 mV	9.5 mV	25 μA	41 μA	$f_{3\,dB}$ = 200 MHz (A_V = 2)	430 V/μs (A_V = +2)	±50 mA Min.	23 mA	8-Pin P-DIP, 8-Lead SO

***Listed in order of decreasing bandwidth**

ELANTEC Part Number	Description	Temp. Range	Min. A_{VOL} over Temp.	Max. Offset Voltage		Max. Bias Current		*Gain Bandwidth Product Typical @ A_V = xx (or f_{3dB})	Min. Slew Rate 25°C (Comp for A_V = xx)	Continuous Output Current	Max. I_{CC} (Full Temp.)	Packages
				25°C	Over Temp.	25°C	Over Temp.					
EL2070C	Monolithic, C.B., 200 MHz Unity Gain Stable Amplifier, with Enable/Disable Function, ±5V Supplies	−40°C to +85°C	125 KV/A (Typ.)	5.5 mV	9.5 mV	25 µA	36 µA	$f_{3\,dB}$ = 200 MHz (A_V = 2)	430 V/µs (A_V = +2)	±50 mA Min.	23 mA	8-Pin P-DIP, 8-Lead SO
EL2171C	Monolithic, 150 MHz GBWP, Current Mode Feedback, Gain of ≥7 Stable, ±5V Supplies	−40°C to +85°C	250 V/V @25°C	6.0 mV	10.0 mV	−30 µA	−46 µA	$f_{3\,dB}$ = 150 MHz (A_V = 20)	800 V/µs (A_V = 20)	±50 mA Min.	21 mA	8-Pin P-DIP, 8-Lead SO
EL2071C	Monolithic, 150 MHz GBWP, Current Mode Feedback, Gain of ≥7 Stable, 200 ns Disable, ±5V Supplies	−40°C to +85°C	250 V/mA @25°C	6.0 mV	10.0 mV	25 µA −30 µA	41 µA −46 µA	$f_{3\,dB}$ = 150 MHz (A_V = 20)	800 V/µs (A_V = 20)	±50 mA Min.	21 mA	8-Pin P-DIP, 8-Lead SO
EL2160C	130 MHz Current Feedback Amplifier	−40°C to +85°C	2000V/mA Typ.	10 mV	15 mV	3 µA −25 µA	10 µA −35 µA	f3 dB = 130 MHz @A_V = +1	1000 V/µs @ A_V = +2	±60 mA Min.	0.2 mA	8-Pin P-DIP, SO
EL2260C	Dual Current Mode Feedback 150 MHz	0°C to +75°C	2000 V/mA (typ)	10 mV	15 mV	3 µA −25 µA	10 µA −35 µA	$f_{3\,dB}$ = 130 MHz @ A_V = +1	1000 V/µs @ A_V = +2	±60 mA Min.	9.2 mA (per Amplifier)	8-Pin P-DIP, SO
EL2460C	Quad Current Mode Feedback 130 MHz	0°C to +75°C	2000 V/mA (typ)	10 mV	15 mV	3 µA −25 µA	10 µA −35 µA	$f_{3\,dB}$ = 130 MHz @ A_V = +1	1000 V/µs @ A_V = +2	±60 mA Min.	9.2 mA (per Amplifier)	14-Pin P-DIP, SO
EL2030C	Monolithic C.B., Current Mode Feedback Unity Gain Stable, 120 MHz, Short Circuit Protected	0°C to +75°C	150 KV/A	20 mV	30 mV	+15 µA (−40 µA)	+25 µA (−50 µA)	$f_{3\,dB}$ = 120 MHz (A_V = +2)	1200 V/µs (A_V = 2)	±60 mA Min.	21 mA	8-Pin P-DIP, 20-Lead SOL,
EL2120C	Monolithic, 100 MHz, Current Mode Feedback, Unity Gain Stable, 40 ns Disable, ±5V to ±15V Supplies	0°C to +75°C	140 V/mA (typ)	20 mV	25 mV	+5 µA −10 µA	+15 µA −40 µA	$f_{3\,dB}$ = 100 MHz (A_V = 1)	600 V/µs (A_V = 1)	±50 mA Min.	20 mA	8-Pin P-DIP, 8-Lead SO

***Listed in order of decreasing bandwidth**

ELANTEC Part Number	Description	Temp. Range	Min. A_{VOL} over Temp.	Max. Offset Voltage		Max. Bias Current		*Gain Bandwidth Product Typical @ A_V = xx (or f_{3dB})	Min. Slew Rate 25°C (Comp for A_V = xx)	Continuous Output Current	Max. I_{CC} (Full Temp.)	Packages
				25°C	Over Temp.	25°C	Over Temp.					
EL2045C	Gain of 2 Stable 100 MHz	0°C to +75°C	64 dB	4 mV	6 mV	8.2 µA	9.2 µA	100 MHz (A_V = +2)	200 V/µs @ A_V = +2	±50 mA Min.	7.6 mA (per Amplifier)	8-Pin P-DIP, SO
EL2245C	Dual Gain of 2 Stable 100 MHz	0°C to +75°C	64 dB	4 mV	6 mV	8.2 µA	9.2 µA	100 MHz (A_V = +2)	200 V/µs @ A_V = +2	±50 mA Min.	7.6 mA (per Amplifier)	8-Pin P-DIP, SO
EL2445C	Quad Gain of 2 Stable 100 MHz	0°C to +75°C	64 dB	4 mV	6 mV	8.2 µA	9.2 µA	100 MHz (A_V = +2)	200 V/µs @ A_V = +2	±50 mA Min.	6.3 mA (per Amplifier)	14-Pin P-DIP, SO
EL2041C	Monolithic, C.B., 90 MHz, Unity Gain Stable, Improved Replacement for HA2541	0°C to +75°C	74 dB	2 mV	10 mV	15 µA	20 µA	90 MHz (A_V = 1)	180 V/µs (A_V = 1)	+25 mA Min.	17 mA	8-Pin P-DIP, 12-Pin TO-8
EL2130C	Monolithic, C.B. Current Mode Feedback, Unity Gain Stable 85 MHz, ±5V Supplies	0°C to +75°C	56 dB	10 mV	15 mV	40 µA	50 µA	$f_{3\,dB}$ = 85 MHz (A_V = 2)	625 V/µs (Typ.) (A_V = +2)	±30 mA	21 mA	8-Pin P-DIP, 8-Lead SO
EL2243C	Monolithic, C.B. Dual, Single Supply, LM324 Upgrade 70 MHz Min. Gain of 5 Stable	0°C to +75°C	98 dB	7 mV	9 mV	1.0 µA	2.0 µA	$f_{3\,dB}$ = 70 MHz (A_V = 5)	90 V/µs (Typ.) (A_V = 5)	±16 mA Min.	10 mA (2 Amplifiers)	8-Pin P-DIP, 20-Lead SOL
EL2044C	Low-Power, 60 MHz Unity Gain Stable	−40°C to +85°C	60 dB	7 mV	9 mV	8.2 µA	9.2 µA	60 MHz (A_V = 1)	250 V/µs	±50 mA Typ.	7.6 mA	8-Pin P-DIP 8-Pin SO
EL2244C	Dual Low-Power 60 MHz Unity Gain Stable	−40°C to +85°C	60 dB	4 mV	6 mV	8.2 µA	9.2 µA	60 MHz (A_V = +1)	250 V/µs @ A_V = +1	±50 mA Min.	7.6 µA (per Amplifier)	8-Pin P-DIP, SO
EL2444C	Quad Low-Power 60 MHz Unity Gain Stable	−40°C to +85°C	60 dB	4 mV	6 mV	8.2 µA	9.2 µA	60 MHz (A_V = +1)	250 V/µs @ A_V = +1	±50 mA Min.	7.6 µA (per Amplifier)	14-Pin P-DIP, SO
EL2224C	Monolithic, C.B., Dual, 60 MHz, Unity Gain Stable Dual A_V = 1 Upgrade to EHA2540, EL2040	0°C to +75°C	68 dB	5 mV	8 mV	4 µA	6 µA	60 MHz (A_V = 1)	150 V/µs (A_V = 10)	±50 mA Typ.	13 mA	8-Pin P-DIP, 20-Pin SOL

*Listed in order of decreasing bandwidth

ELANTEC Part Number	Description	Temp. Range	Min. A_{VOL} over Temp.	Max. Offset Voltage		Max. Bias Current		*Gain Bandwidth Product Typical @ A_V = xx (or f_{3dB})	Min. Slew Rate 25°C (Comp for A_V = xx)	Continuous Output Current	Max. I_{CC} (Full Temp.)	Packages
				25°C	Over Temp.	25°C	Over Temp.					
EL2232C	Monolithic, Fast Settling, Dual Current Mode Feedback Amp, 60 MHz	0°C to +75°C	600 KV/A	7 mV	10 mV	+5 μA (−20)	+7.5 μA (−25)	$f_{3\,dB}$ = 60 MHz (A_V = +1)	400 V/μs (A_V = 1)	±23 mA Min.	14 mA (2 Amplifiers)	8-Pin P-DIP 16-Lead SOL
EL2020C	Monolithic, C.B., Current Mode Feedback, Unity Gain Stable, 50 MHz, Current Limited, Enable/Disable Function	0°C to +75°C	60 dB	10 mV	15 mV	15 μA	25 μA	$f_{3\,dB}$ = 50 MHz (A_V = 2)	300 V/μs (A_V = 1)	±30 mA Min.	15 mA	8-Pin P-DIP
EL2242C	Monolithic, C.B., Dual Single Supply, 30 MHz Unity Gain Stable, LM324 Upgrade	0°C to +75°C	84 dB	7 mV	9 mV	1.0 μA	2.0 μA	$f_{3\,dB}$ = 30 MHz (A_V = 1)	40 V/μs (Typ.) (A_V = 1)	±12 mA Min.	10 mA (2 Amplifiers)	8-Pin P-DIP, 20-Lead SOL

Note: Some specifications in table are for the best version available.
Consult individual data sheets for product details.

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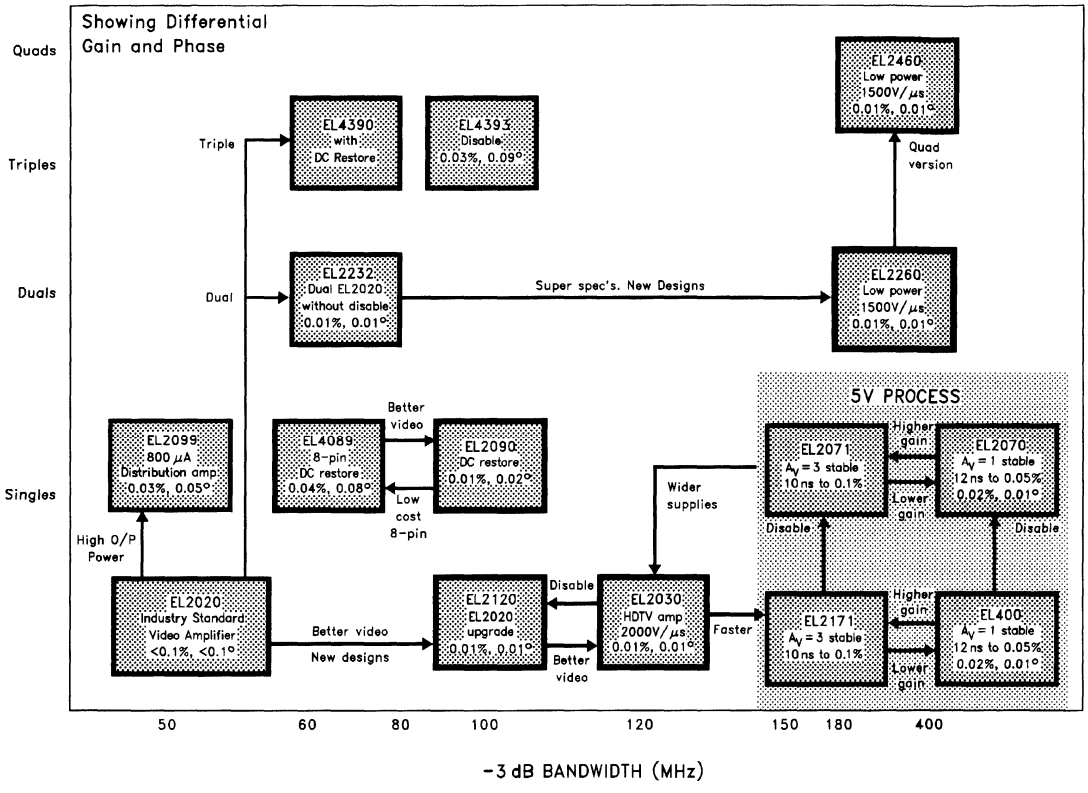
Amplifier MHz Bandwidth Selector

Current Mode Feedback Amplifiers



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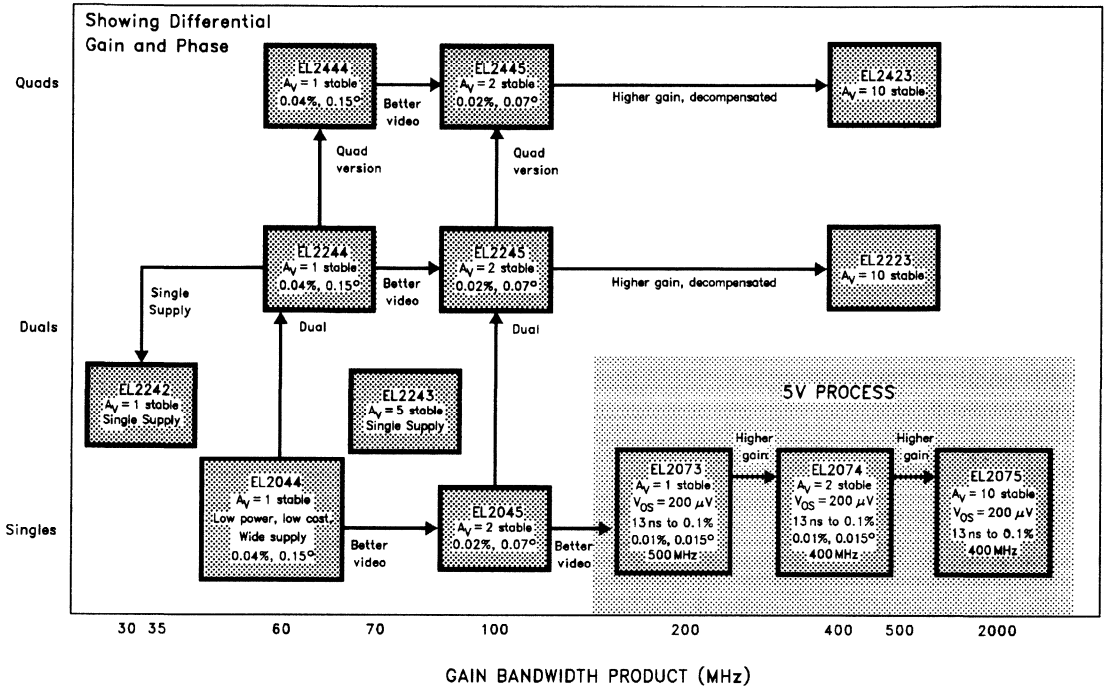
Voltage Feedback Amplifiers



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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2020C
50 MHz Current Feedback Amplifier

Features

- Slew rate 500 V/μs
- ±33 mA output current
- Drives ±2.4V into 75Ω
- Differential phase <0.1°
- Differential gain <0.1%
- V supply ±5V to ±18V
- Output short circuit protected
- Uses current mode feedback
- 1% settling time of 50 ns for 10V step
- Low cost
- 9 mA supply current
- 8-pin mini-dip

Applications

- Video gain block
- Residue amplifier
- Radar systems
- Current to voltage converter
- Coax cable driver with gain of 2

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2020CN	0°C to +75°C	P-DIP	MDP0031
EL2020CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EL2020 is a fast settling, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain then a conventional voltage feedback operational amplifier.

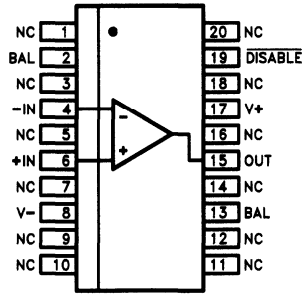
The EL2020 will drive two double terminated 75Ω coax cables to video levels with low distortion. Since it is a closed loop device, the EL2020 provides better gain accuracy and lower distortion than an open loop buffer. The device includes output short circuit protection, and input offset adjust capability.

The bandwidth and slew rate of the EL2020 are relatively independent of the closed loop gain taken. The 50 MHz bandwidth at unity gain only reduces to 30 MHz at a gain of 10. The EL2020 may be used in most applications where a conventional op amp is used, with a big improvement in speed power product.

Elantec products and facilities comply with Elantec document, QRA-1: *Processing-Monolithic Products.*

Connection Diagrams

SOL



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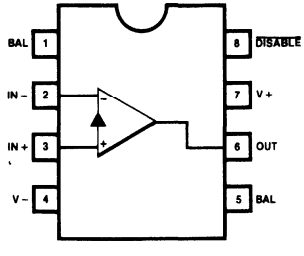
DIP



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Absolute Maximum Ratings (25°C)

V_S	Supply Voltage	±18V or 36V	T_A	Operating Temperature Range	0°C to +75°C
V_{IN}	Input Voltage	±15V or V_S	T_J	Operating Junction Temperature	
ΔV_{IN}	Differential Input Voltage	±10V		Plastic Package, SOL	150°C
I_{IN}	Input Current (Pins 2 or 3)	±10 mA	T_{ST}	Storage Temperature	−65°C to +150°C
I_{INS}	Input Current (Pins 1, 5, or 8)	±5 mA		Lead Temperature	
P_D	Maximum Power Dissipation			(Soldering, 5 seconds)	300°C
	(See Curves)	1.25W			
I_{OP}	Peak Output Current	Short Circuit Protected			
	Output Short Circuit Duration (Note 2)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX2002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX2002.
III	QA sample tested per QA test plan QCX2002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop Characteristics V_S = ±15V

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
V_{OS} (Note 1)	Input Offset Voltage	25°C	−10	3	+10	I	mV
		T_{MIN}, T_{MAX}	−15		+15	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			−30		V	µV/°C
CMRR (Note 3)	Common Mode Rejection Ratio	ALL	50	60		II	dB
PSRR (Note 4)	Power Supply Rejection Ratio	25°C	65	75		I	dB
		T_{MIN}, T_{MAX}	60			III	dB
$+I_{IN}$	Non-inverting Input Current	25°C, T_{MAX}	−15	5	+15	II	µA
		T_{MIN}	−25		+25	III	µA
$+R_{IN}$	Non-Inverting Input Resistance	ALL	1	5		II	MΩ
+IPSR (Note 4)	Non-Inverting Input Current Power Supply Rejection	25°C, T_{MAX}		0.05	0.5	II	µA/V
		T_{MIN}			1.0	III	µA/V
$-I_{IN}$ (Note 1)	−Input Current	25°C, T_{MAX}	−40	10	+40	II	µA
		T_{MIN}	−50		+50	III	µA

EL2020C
50 MHz Current Feedback Amplifier

Open Loop Characteristics $V_S = \pm 15V$ — Contd.

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
−ICMR (Note 3)	−Input Current Common Mode Rejection	25°C, T_{MAX}		0.5	2.0	II	μA/V
		T_{MIN}			4.0	III	μA/V
−IPSR (Note 4)	−Input Current Power Supply Rejection	25°C, T_{MAX}		0.05	0.5	II	μA/V
		T_{MIN}			1.0	III	μA/V
R_{ol}	Transimpedence ($\Delta V_{OUT}/\Delta(-I_{IN})$) $R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25°C, T_{MAX}	300	1000		II	V/mA
		T_{MIN}	50			III	V/mA
A_{VOL1}	Open Loop DC Voltage Gain $R_L = 400\Omega$, $V_{OUT} = \pm 10V$	25°C, T_{MAX}	70	80		II	dB
		T_{MIN}	60			III	dB
A_{VOL2}	Open Loop DC Voltage Gain $R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	25°C, T_{MAX}	60	70		II	dB
		T_{MIN}	55			III	dB
V_O	Output Voltage Swing $R_L = 400\Omega$	25°C, T_{MAX}	±12	±13		II	V
		T_{MIN}	±11			III	V
I_{OUT}	Output Current $R_L = 400\Omega$	25°C, T_{MAX}	±30	±32.5		II	mA
		T_{MIN}	±27.5			III	mA
I_s	Quiescent Supply Current	25°C		9	12	I	mA
		T_{MIN}, T_{MAX}			15	III	mA
$I_{s\ off}$	Supply Current, Disabled, $V_8 = 0V$	ALL		5.5	7.5	II	mA
I_{logic}	Pin 8 Current, Pin 8 = 0V	ALL		1.1	1.5	II	mA
I_D	Min Pin 8 Current to Disable	ALL		120	250	II	μA
I_e	Max Pin 8 Current to Enable	ALL			30	II	μA

AC Closed Loop Characteristics EL2020C $V_S = \pm 15V, T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
	Closed Loop Gain of 1 V/V (0 dB), $R_F = 1\ k\Omega$					
SR1	Slew Rate, $R_l = 400\Omega$, $V_O = \pm 10V$, test at $V_O = \pm 5V$	300	500		I	V/μs
FPBW1	Full Power Bandwidth (Note 5)	4.77	7.95		I	MHz
t_r1	Rise Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		6		V	ns
t_f1	Fall Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		6		V	ns
t_p1	Propagation Delay, $R_l = 100\Omega$, $V_{OUT} = 1V$, 50% Points		8		V	ns
	Closed Loop Gain of 1 V/V (0 dB), $R_F = 820\Omega$					
BW	−3 dB Small Signal Bandwidth, $R_l = 100\Omega$, $V_O = 100$ mV		50		V	MHz
t_s	1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		50		V	ns
t_s	0.1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		90		V	ns
	Closed Loop Gain of 10 V/V (20 dB), $R_F = 1\ k\Omega$, $R_G = 111\Omega$					
SR10	Slew Rate, $R_l = 400\Omega$, $V_O = \pm 10V$, Test at $V_O = \pm 5V$	300	500		I	V/μs
FPBW10	Full Power Bandwidth (Note 5)	4.77	7.95		I	MHz
t_r10	Rise Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		25		V	ns
t_f10	Fall Time, $R_l = 100\Omega$, $V_{OUT} = 1V$, 10% to 90%		25		V	ns
t_p10	Propagation Delay, $R_l = 100\Omega$, $V_{OUT} = 1V$, 50% points		12		V	ns
	Closed Loop Gain of 10 V/V (20 dB), $R_F = 680\Omega$, $R_G = 76\Omega$					
BW	−3 dB Small Signal Bandwidth, $R_l = 100\Omega$, $V_O = 100$ mV		30		V	MHz
t_s	1% Settling Time, $R_l = 400\ \Omega$, $V_O = 10V$		55		V	ns
t_s	0.1% Settling Time, $R_l = 400\Omega$, $V_O = 10V$		280		V	ns

Note 1: The offset voltage and inverting input current can be adjusted with an external 10 kΩ pot between pins 1 and 5 with the wiper connected to V_{CC} (Pin 7) to make the output offset voltage zero.

Note 2: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 3: $V_{CM} = \pm 10V$.

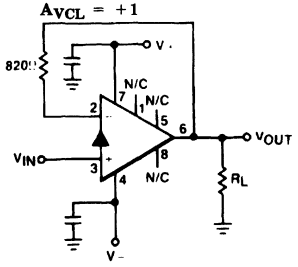
Note 4: $\pm 4.5V \leq V_S \leq \pm 18V$.

Note 5: Full Power Bandwidth is guaranteed based on Slew Rate measurement. $FPBW = SR/2\pi V_{peak}$.

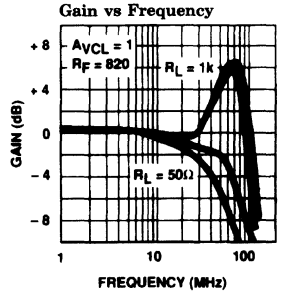
EL2020C
50 MHz Current Feedback Amplifier

Typical Performance Curves Non-Inverting Gain of One

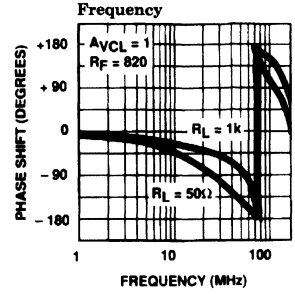
A_{VCL} = +1



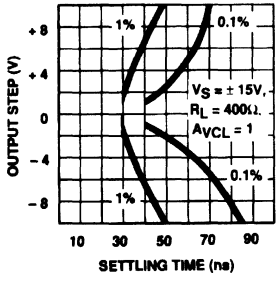
Gain vs Frequency



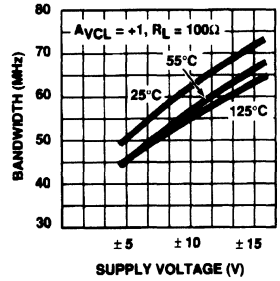
Phase Shift vs Frequency



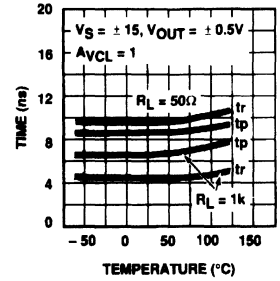
Settling Time vs Output Swing



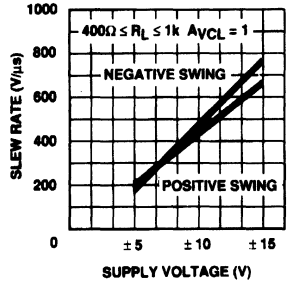
−3 dB Bandwidth vs Supply Voltage



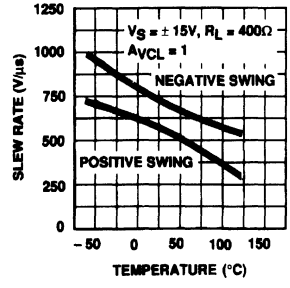
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



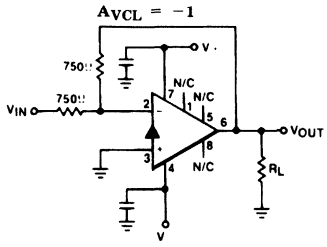
Slew Rate vs Temperature



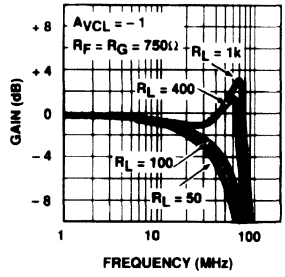
2020-4

Typical Performance Curves — Contd. Inverting Gain of One

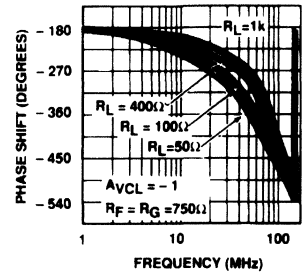
$A_{VCL} = -1$



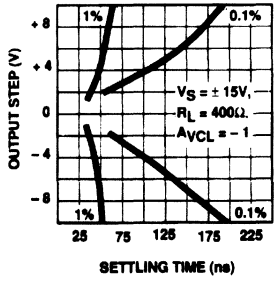
Gain vs Frequency



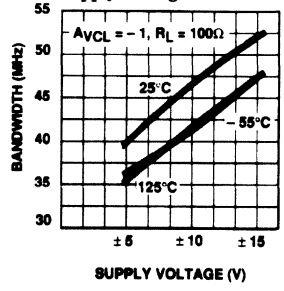
Phase Shift vs Frequency



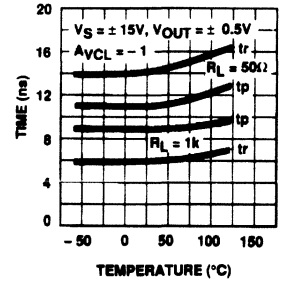
Settling Time vs Output Swing



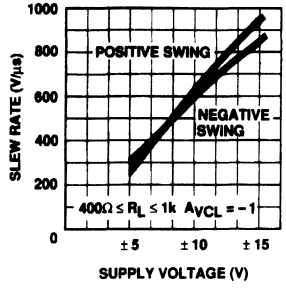
−3 dB Bandwidth vs Supply Voltage



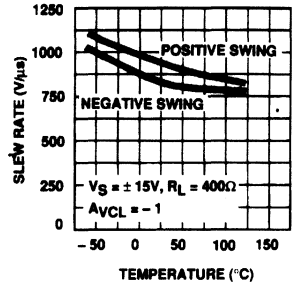
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



Slew Rate vs Temperature



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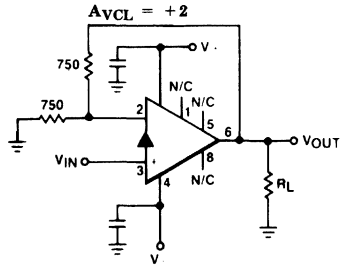
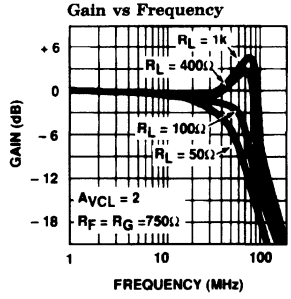
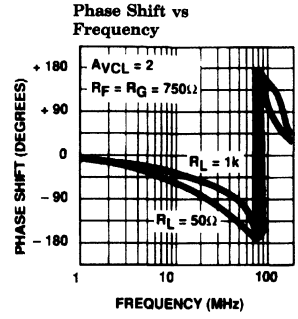
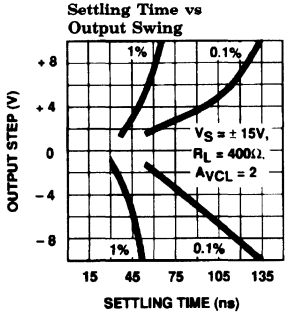
EL2020C
50 MHz Current Feedback Amplifier

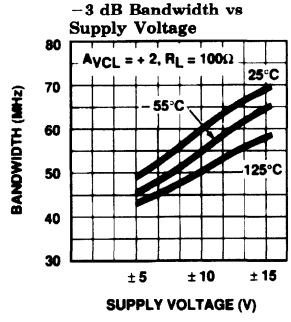
Typical Performance Curves — Contd. Non-Inverting Gain of Two

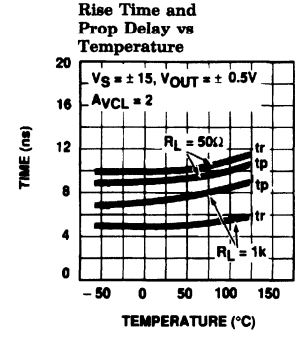


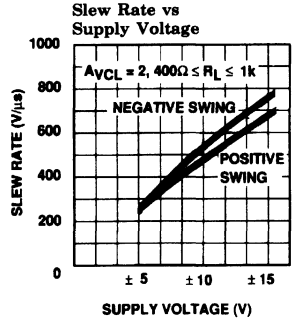


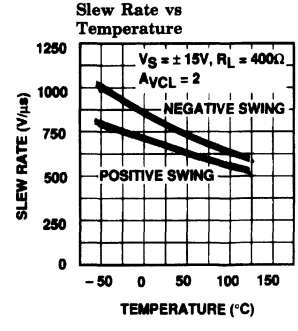








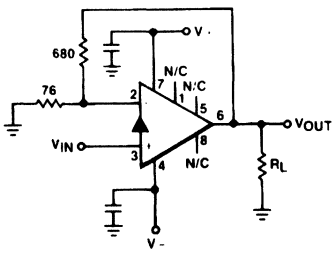




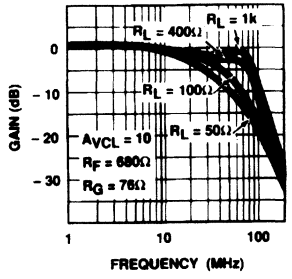
2020-6

Typical Performance Curves — Contd. Non-Inverting Gain of Ten

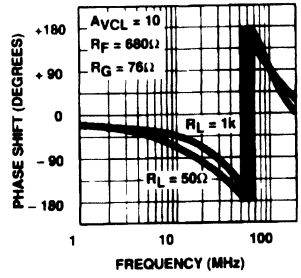
A_{VCL} = +10



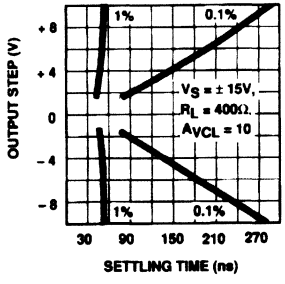
Gain vs Frequency



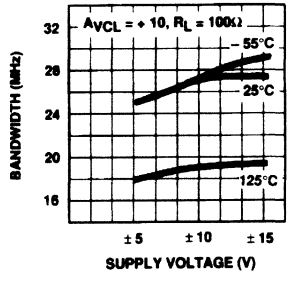
Phase Shift vs Frequency



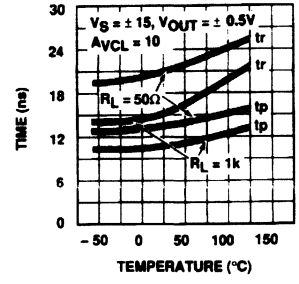
Settling Time vs Output Swing



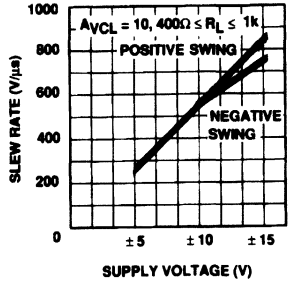
-3 dB Bandwidth vs Supply Voltage



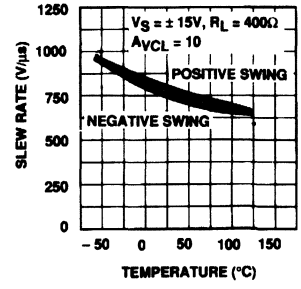
Rise Time and Prop Delay vs Temperature



Slew Rate vs Supply Voltage



Slew Rate vs Temperature



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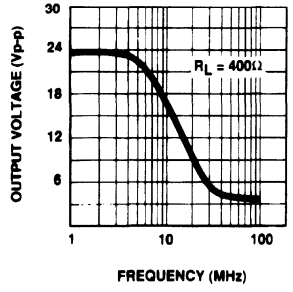
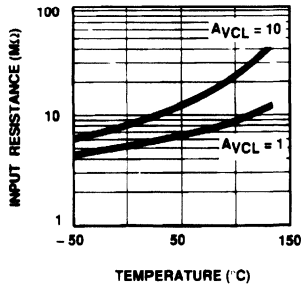
EL2020C
50 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

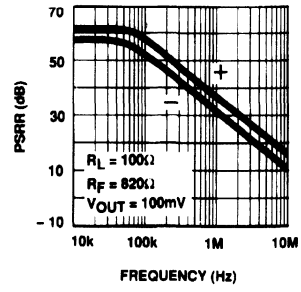
Maximum Undistorted Output Voltage vs Frequency



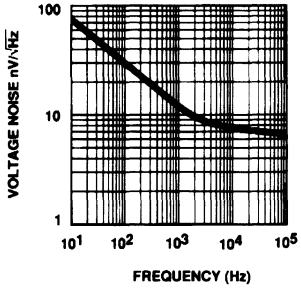
Input Resistance vs Temperature



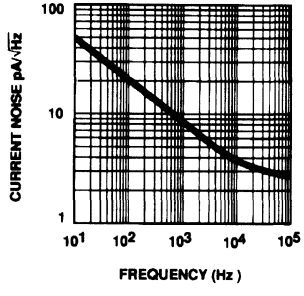
PSRR vs Frequency



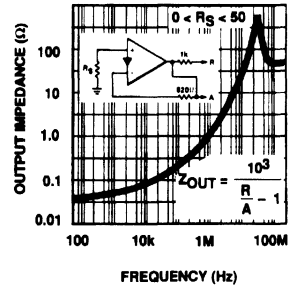
Voltage Noise vs Frequency



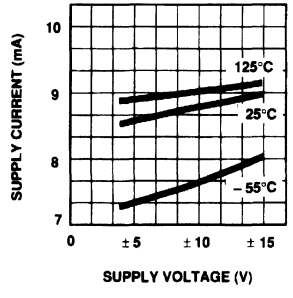
Current Noise vs Frequency



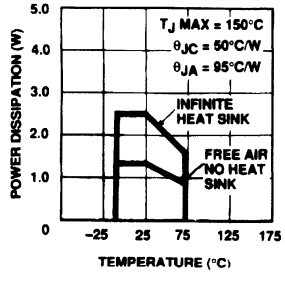
Output Impedance vs Frequency



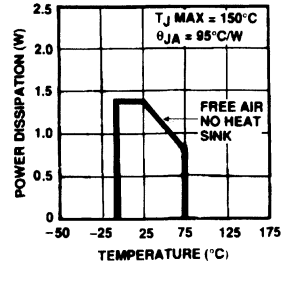
Supply Current vs Supply Voltage



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2020-8

Application Information

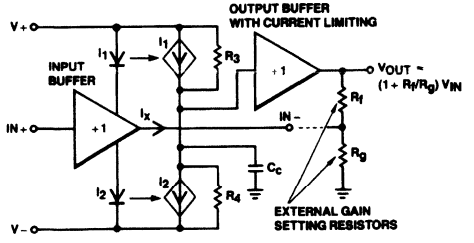
Theory of Operation

The EL2020 has a unity gain buffer similar to the EL2003 from the non-inverting input to the inverting input. The error signal of the EL2020 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is the transresistance (R_{OL}) of the EL2020 [$V_{OUT} = R_{OL} * I_{INV}$]. Since R_{OL} is very large ($\approx 10^6$), the current flowing into the inverting input in the steady state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first order approximation for circuit analysis, namely that...

1. The voltage across the inputs $\approx$ 0 and
2. The current into the inputs is $\approx$ 0

Simplified Block Diagram of EL2020



Resistor Value Selection and Optimization

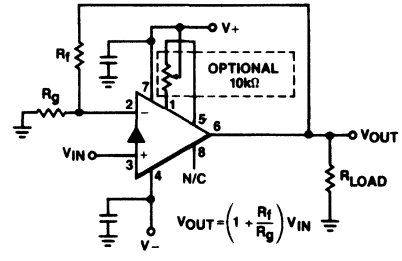
The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2020. A nominal value for the feedback resistor is 1 kΩ, which is the value used for production testing. This value guarantees stability. For a given gain, the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth will be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed loop transfer function which results from stray capacitance between the inverting input and ground.

Power Supplies

The EL2020 may be operated with single or split power supplies as low as ±3V (6V total) to as high as ±18V (36V total). The slew rate degrades significantly for supply voltages less than ±5V (10V total), but the bandwidth only changes 25% for supplies from ±3V to ±18V. It is not necessary to use equal value split power supplies, i.e., −5V and +12V would be excellent for 0V to 1V video signals. Bypass capacitors from each supply pin to a ground plane are recommended. The EL2020 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate supply ringing and the errors it might cause, a 4.7 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rate and longer settling times.

Non-Inverting Amplifier



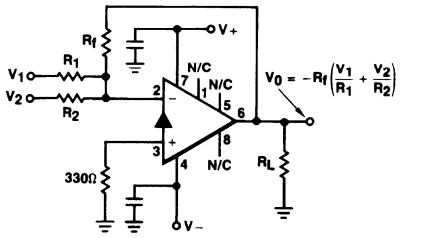
EL2020 Typical Non-Inverting Amplifier Characteristics

A_V	R_F	R_G	Bandwidth	10V Settling Time	
				1%	0.1%
+1	820Ω	None	50 MHz	50 ns	90 ns
+2	750Ω	750Ω	50 MHz	50 ns	100 ns
+5	680Ω	170Ω	50 MHz	50 ns	200 ns
+10	680Ω	76Ω	30 MHz	55 ns	280 ns

EL2020C
50 MHz Current Feedback Amplifier

Application Information — Contd.

Summing Amplifier



EL2020 Typical Inverting Amplifier Characteristics

A_V	R_F	R_1, R_2	Bandwidth	10V Settling Time	
				1%	0.1%
−1	750Ω	750Ω	40 MHz	50 ns	130 ns
−2	750Ω	375Ω	40 MHz	55 ns	160 ns
−5	680Ω	130Ω	40 MHz	55 ns	160 ns
−10	680Ω	68Ω	30 MHz	70 ns	170 ns

Input Range

The non-inverting input to the EL2020 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit.

The input charactersitics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that Schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2020 is fairly tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources may cause oscillations; a 1 kΩ resistor in series with the input lead will usually eliminate problems without sacrificing too much speed.

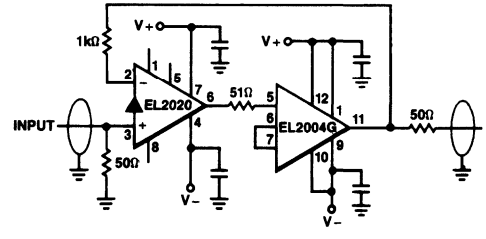
Current Limit

The EL2020 has internal current limits that protect the output transistors. The current limit goes down with junction temperature rise. At a junction temperature of +175°C the current limits are at about 50 mA. If the EL2020 output is shorted to ground when operating on ±15V supplies, the power dissipation could be as great as 1.1W. A heat sink is required in order for the EL2020 to survive an indefinite short. Recovery time to come out of current limit is about 50 ns.

Using the 2020 with Output Buffers

When more output current is required, a wideband buffer amplifier can be included in the feedback loop of the EL2020. With the EL2003 the subsystem overshoots about 10% due to the phase lag of the EL2003. With the EL2004 in the loop, the overshoot is less than 2%. For even more output current, several buffers can be paralleled.

EL2020 Buffered with an EL2004



Capacitive Loads

The EL2020 is like most high speed feedback amplifiers in that it does not like capacitive loads between 50 pF and 1000 pF. The output resistance works with the capacitive load to form a second non-dominate pole in the loop. This results in excessive peaking and overshoot and can lead to oscillations. Standard resistive isolation techniques used with other op amps work well to isolate capacitive loads from the EL2020.

Application Information — Contd.

Offset Adjust

To calculate the amplifier system offset voltage from input to output we use the equation:

Output Offset Voltage = V_{OS} (R_F/R_G+1) ± I_{BIAS} (R_F)

The EL2020 output offset can be nulled by using a 10 kΩ potentiometer from pins 1 to 5 with the slider tied to pin 7 ($+V_{CC}$). This adjusts both the offset voltage and the inverting input bias current. The typical adjustment range is ±80 mV at the output.

Compensation

The EL2020 is internally compensated to work with external feedback resistors for optimum bandwidth over a wide range of closed loop gain. The part is designed for a nominal 1 kΩ of feedback resistance, although it is possible to get more bandwidth by decreasing the feedback resistance.

The EL2020 becomes *less* stable by adding capacitance in parallel with the feedback resistor, so feedback capacitance is not recommended.

The EL2020 is also sensitive to stray capacitance from the inverting input to ground, so the board should be laid out to keep the physical size of this node small, with ground plane kept away from this node.

Active Filters

The EL2020's low phase lag at high frequencies makes it an excellent choice for high performance active filters. The filter response more closely approaches the theoritical response than with conventional op amps due to the EL2020's smaller propagation delay. Because the internal compensation of the EL2020 depends on resistive feedback, the EL2020 should be set up as a gain block.

Driving Cables

The EL2020 was designed with driving coaxial cables in mind. With 30 mA of output drive and low output impedance, driving one to three 75Ω double terminated coax cables with one EL2020 is practical. Since it is easy to set up a gain of +2, the double matched method is the best way to drive coax cables, because the impedance match on both ends of the cable will suppress reflections. For a discussion on some of the other ways to drive cables, see the section on driving cables in the EL2003 data sheet.

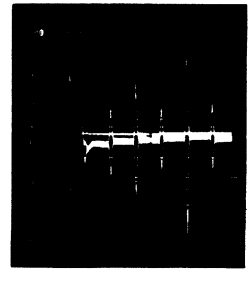
Video Performance Characteristics

The EL2020 makes an excellent gain block for video systems, both RS-170 (NTSC) and faster. It is capable of driving 3 double terminated 75Ω cables with distortion levels acceptable to broadcasters. A common video application is to drive a 75Ω double terminated coax with a gain of 2.

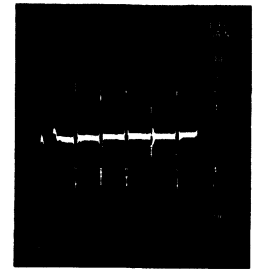
To measure the video performance of the EL2020 in the non-inverting gain of 2 configuration, 5 identical gain-of-two circuits were cascaded (with a divide by two 75Ω attenuator between each stage) to increase the errors.

The results, shown in the photos, indicate the entire system of 5 gain-of-two stages has a differential gain of 0.5% and a differential phase of 0.5°. This implies each device has a differential gain/phase of 0.1% and 0.1°, but these are too small to measure on single devices.

Differential Phase of 5 Cascaded Gain-Of-Two Stages



Differential Gain of 5 Cascaded Gain-Of-Two Stages



2020-14

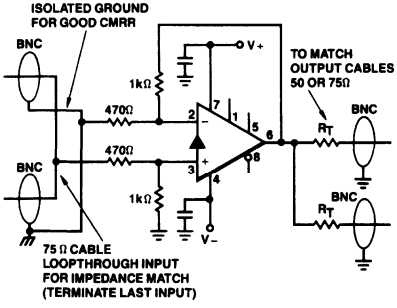
EL2020C
50 MHz Current Feedback Amplifier

Application Information — Contd.

Video Distribution Amplifier

The distribution amplifier shown below features a difference input to reject common mode signals on the 75Ω coax cable input. Common mode rejection is often necessary to help to eliminate 60 Hz noise found in production environments.

Video Distribution Amplifier with Difference Input



2020-15

EL2020 Disable/Enable Operation

The EL2020 has an enable/disable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to pin 7, V_{CC}. When more than 250 μA is pulled from pin 8, the EL2020 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is halved. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (~1.1 mA) if pin 8 is grounded.

To draw current out of pin 8 an "open collector output" logic gate or a discrete NPN transistor can be used. This logic interface method has the advantage of level shifting the logic signal from 5V supplies to whatever supply the EL2020 is operating on without any additional components.

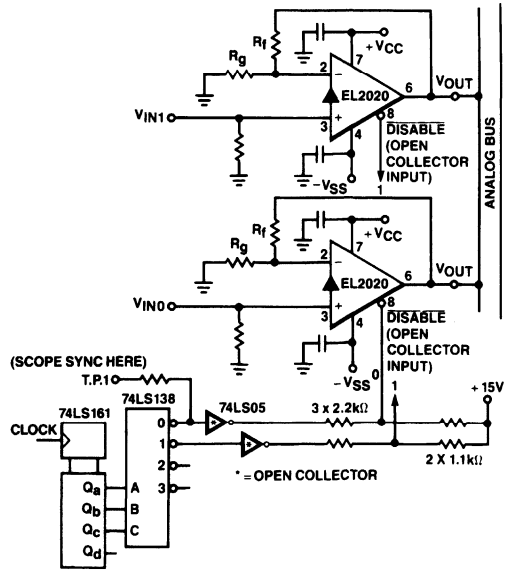
Using the EL2020 as a Multiplexer

An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown.

When the EL2020 is disabled, the DC output impedance is very high, over 10 kΩ. However there is also an output capacitance that is non-linear. For signals of less than 5V peak to peak, the output capacitance looks like a simple 15 pF capacitor. However, for larger signals the output capacitance becomes much larger and non-linear.

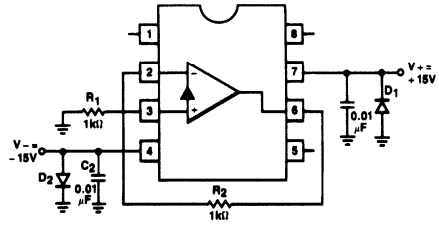
The example multiplexer will switch between amplifiers in 5 μs for signals of less than ±2V on the outputs. For full output signals of 20V peak to peak, the selection time becomes 25 μs. The disabled outputs also present a capacitive load and therefore only three amplifiers can have their outputs shorted together. However an unlimited number can sum together if a small resistor (25Ω) is inserted in series with each output to isolate it from the "bus". There will be a small gain loss due to the resistors of course.

Using the EL2020 as a Multiplexer



2020-16

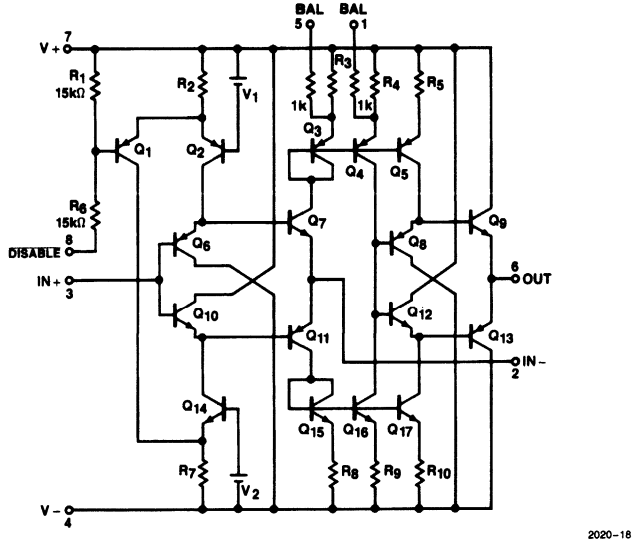
Burn-In Circuit



2020-17

Pin numbers are for DIP Packages.
All Packages Use the Same Schematic.

Equivalent Circuit



2020-18

EL2020 Macromodel

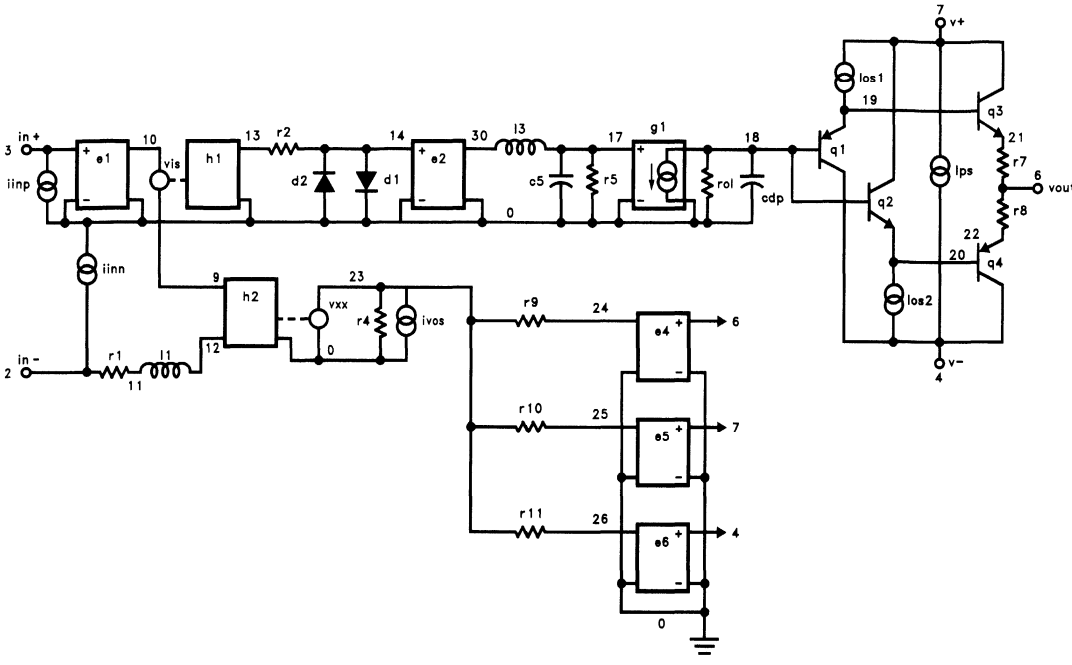
```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2020       3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 29nH
iinp 3 0 10µA
iinm 2 0 5µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
15 30 17 1.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 1Meg
cdp 18 0 5pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
```

EL2020 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply
*
ips 7 4 3mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 6 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is = 5e - 15 bf = 100 tf = 0.2nS)
.model qp pnp (is = 5e - 15 bf = 100 tf = 0.2nS)
.model dclamp d(is = 1e - 30 ibv = 0.266 bv = 1.67 n = 4)
.ends
```

EL2020C
50 MHz Current Feedback Amplifier

EL2020 Macromodel



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EL2030C

120 MHz Current Feedback Amplifier

Features

- −3 dB bandwidth = 120 MHz, A_V = 1
- −3 dB bandwidth = 110 MHz, A_V = 2
- 0.01% differential gain and 0.01° differential phase (NTSC, PAL)
- 0.05% differential gain and 0.02° differential phase (HDTV)
- Slew rate 2000 V/μs
- 65 mA output current
- Drives ±10V into 200Ω load
- Characterized at ±5V and ±15V
- Low voltage noise
- Current mode feedback
- Settling time of 40 ns to 0.25% for a 10V step
- Output short circuit protected
- Low cost

Applications

- Video gain block
- Video distribution amplifier
- HDTV amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coax cable driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2030CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2030CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EL2030 is a very fast, wide bandwidth amplifier optimized for gains between −10 and +10. Built using the Elantec monolithic Complementary Bipolar process, this amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

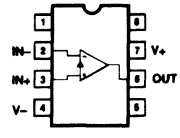
Due to its wide operating supply range (±15V) and extremely high slew rate of 2000 V/μs, the EL2030 drives ±10V into 200Ω at a frequency of 30 MHz, while achieving 110 MHz of small signal bandwidth at A_V = +2. This bandwidth is still 95 MHz for a gain of +10. On ±5V supplies the amplifier maintains a 90 MHz bandwidth for A_V = +2. When used as a unity gain buffer, the EL2030 has a 120 MHz bandwidth with the gain precision and low distortion of closed loop buffers.

The EL2030 features extremely low differential gain and phase, a low noise topology that reduces noise by a factor of 2 over competing amplifiers, and settling time of 40 ns to 0.25% for a 10V step. The output is short circuit protected. In addition, datasheet limits are guaranteed for ±5V and ±15V supplies.

Elantec's products and facilities comply with applicable quality specifications. See Elantec document, QRA-1: *Processing, Monolithic Integrated Circuits.*

Connection Diagrams

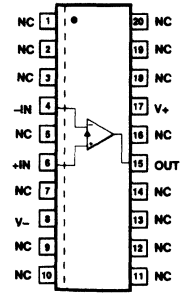
Mini DIP



2030-1

Top View

SOL



2030-3

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

EL2030C
120 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V	T_J	Operating Junction Temperature	
V_{IN}	Input Voltage	±15V or V_S		Plastic Packages	150°C
ΔV_{IN}	Differential Input Voltage	±6V	T_{ST}	Storage Temperature	−65°C to +150°C
P_D	Maximum Power Dissipation	See Curves		Lead Temperature	
I_{IN}	Input Current	±10 mA		DIP Package	300°C
I_{OP}	Peak Output Current	Short Circuit Protected		(Soldering: <5 seconds—CN;	
	Output Short Circuit Duration (Note 1)	Continuous		<10 seconds—J)	
				SOL Package	
T_A	Operating Temperature Range	0°C to +75°C		Vapor Phase (60 seconds)	215°C
				Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±15V, R_L = 200Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level EL2030C	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		10	20	I	mV
			T_{MIN}, T_{MAX}			30	III	mV
		V_S = ±5V	25°C		5	10	I	mV
			T_{MIN}, T_{MAX}			15	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift				25		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		5	15	I	µA
			T_{MIN}, T_{MAX}			25	III	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		10	40	I	µA
			T_{MIN}, T_{MAX}			50	III	µA
$+R_{IN}$	+Input Resistance		Full	1.1	2.0		II	MΩ
C_{IN}	Input Capacitance		25°C		1		V	pF
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	Full	50	60		II	dB
−ICMR	Input Current Common Mode Rejection (Note 2)		25°C		5	10	I	µA/V
			T_{MIN}, T_{MAX}			20	III	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		Full	60	70		II	dB
+IPSR	+Input Current Power Supply Rejection (Note 3)		25°C		0.1	0.5	II	µA/V
			T_{MIN}, T_{MAX}			1.0	III	µA/V
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.5	5.0	II	µA/V
			T_{MIN}, T_{MAX}			8.0	III	µA/V

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 200Ω, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level EL2030C	Units
R_{OL}	Transimpedance ($\Delta V_{OUT}/\Delta(-I_{IN})$) V_{OUT} = ±10V	V_S = ±15V	25°C	88	150		II	V/mA
			T_{MIN}, T_{MAX}	75			III	V/mA
	V_{OUT} = ±2.5V (Note 6)	V_S = ±5V	25°C	80	120		II	V/mA
			T_{MIN}, T_{MAX}		70		III	V/mA
A_{VOL}	Open Loop DC Voltage Gain V_{OUT} = ±10V	V_S = ±15V	Full	60	70		II	dB
	V_{OUT} = ±2.5V (Note 6)	V_S = ±5V	Full	56	65		II	dB
V_O	Output Voltage Swing (Note 6)	V_S = ±15V	Full	12	13		II	V
		V_S = ±5V	Full	3	3.5		II	V
I_{OUT}	Output Current (Note 9)	V_S = ±15V	Full	60	65		II	mA
		V_S = ±5V	Full	30	35		II	mA
R_{OUT}	Output Resistance		25°C		5		V	Ω
I_S	Quiescent Supply Current		Full		15	21	II	mA
I_{SC}	Short Circuit Current		25°C		85		V	mA

Closed Loop AC Electrical Characteristics

V_S = ±15V, A_V = +2, R_F = 820Ω, R_G = 820Ω and R_L = 200Ω

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level EL2030C	Units
SR	Slew Rate (Note 7)		25°C	1200	2000		IV	V/μs
FPBW	Full Power Bandwidth (Note 4)		25°C	19	31.8		IV	MHz
t_r, t_f	Rise Time. Fall Time	V_{pp} = 250 mV	25°C		3		V	ns
t_s	Settling Time to 0.25% for 10V step (Note 5)		25°C		40		V	ns
ΔG	Differential Gain (Note 8)		25°C		0.01		V	% p-p
Δϕ	Differential Phase (Note 8)		25°C		0.01		V	° p-p
eN	Input Spot Noise at 1 kHz R_G = 101; R_F = 909		25°C		4		V	nV/√Hz

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: V_{CM} = ±10V for V_S = ±15V. For V_S = ±5V, V_{CM} = ±2.5V.
Note 3: V_{OS} is measured at V_S = ±4.5V and at V_S = ±18V. Both supplies are changed simultaneously.
Note 4: Full Power Bandwidth is specified based on Slew Rate measurement FPBW = $SR/2\pi V_P$.
Note 5: Settling Time measurement techniques are shown in: "Take The Guesswork Out of Settling Time Measurements", EDN, September 19, 1985. Available from the factory upon request.
Note 6: R_L = 100Ω.
Note 7: V_O = ±10V, tested at V_O = ±5. See test circuit.
Note 8: NTSC (3.58 MHz) and PAL (4.43 MHz).
Note 9: For V_S = ±15V, V_{OUT} = ±10V. For V_S ±5V, V_{OUT} = ±2.5V.

EL2030C
120 MHz Current Feedback Amplifier

Typical Performance Curves

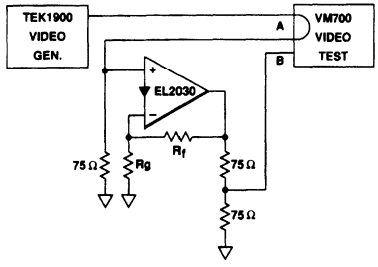
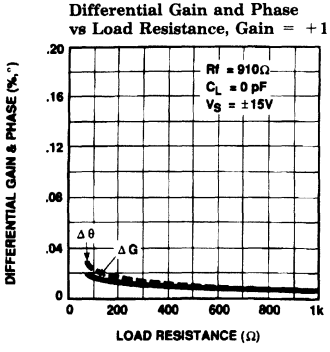
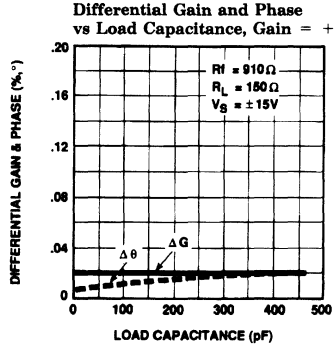
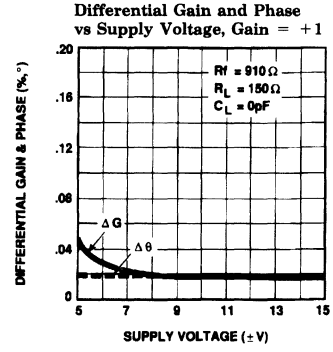
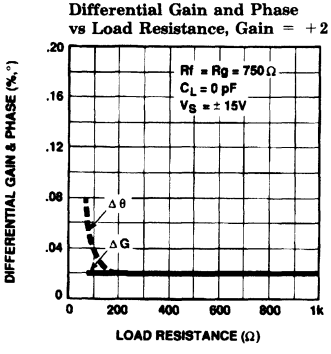


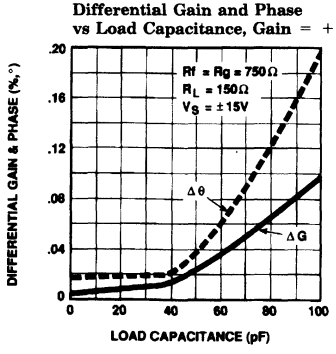
Figure 1. NTSC Video Differential Gain and Phase Test Set-Up

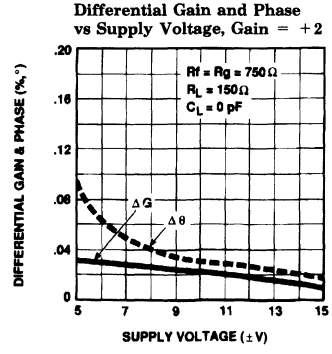












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Typical Performance Curves — Contd.

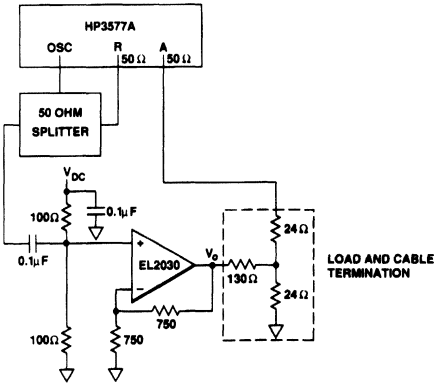
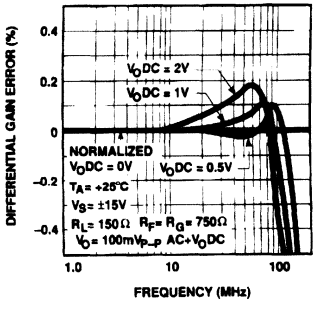
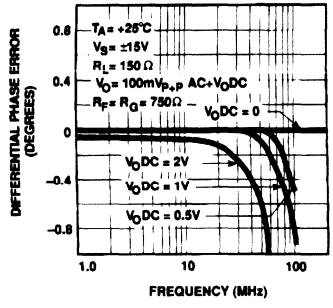


Figure 2. HDTV and Wideband Video Differential Gain and Phase Test Set-Up

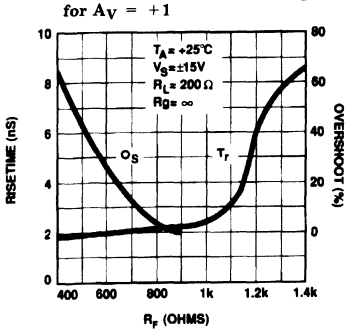
Differential Gain Error vs Frequency for Various DC Output Levels



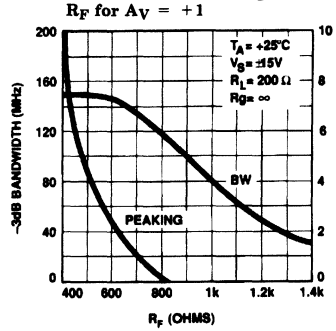
Differential Phase Error vs Frequency for Various DC Output Levels



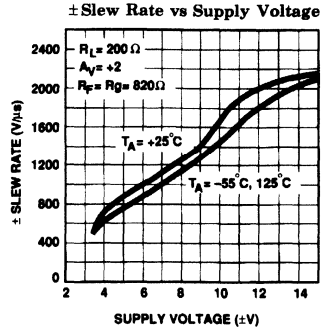
Risetime and Overshoot vs R_F for A_V = +1



Bandwidth and Peaking vs R_F for A_V = +1



±Slew Rate vs Supply Voltage



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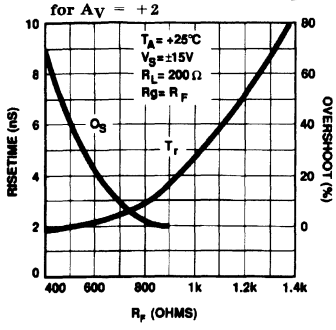
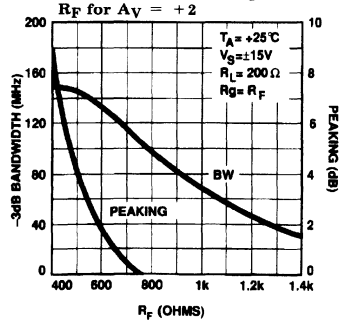
EL2030C
120 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

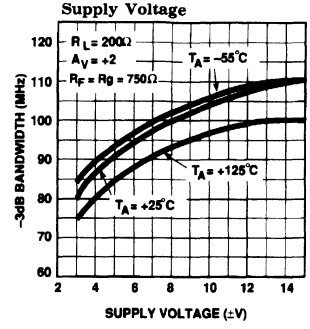
Risetime and Overshoot vs R_F for $A_V = +2$



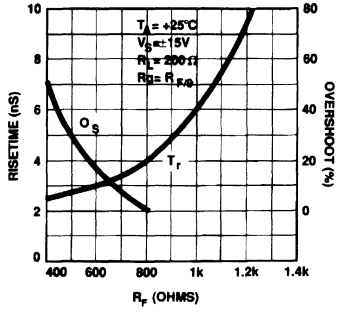
Bandwidth and Peaking vs R_F for $A_V = +2$



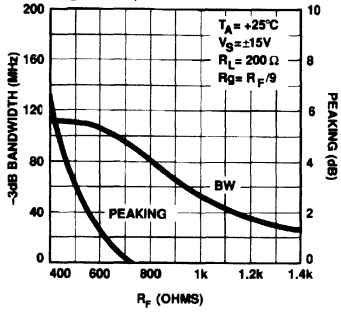
−3 dB Bandwidth vs Supply Voltage



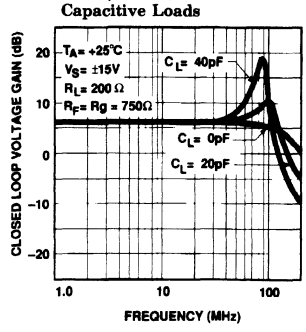
Risetime and Overshoot vs R_F for $A_V = +10$



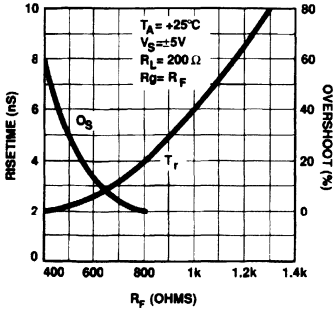
Bandwidth and Peaking vs R_F for $A_V = +10$



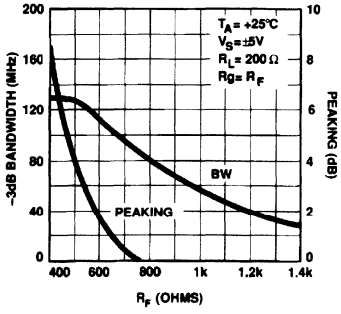
Voltage Gain vs Frequency for $A_V = +2$, various Capacitive Loads



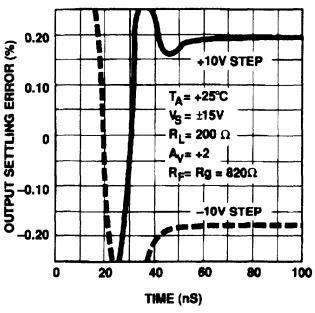
Risetime and Overshoot vs R_F for $A_V = +2$, $V_S = \pm 5V$



Bandwidth and Peaking vs R_F for $A_V = +2$, $V_S = +5V$



Output Settling Error vs Time



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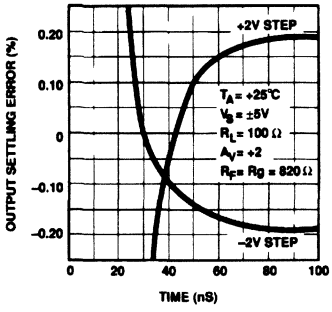
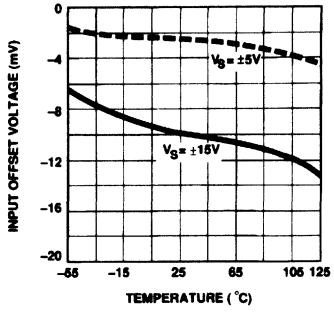
Typical Performance Curves — Contd.

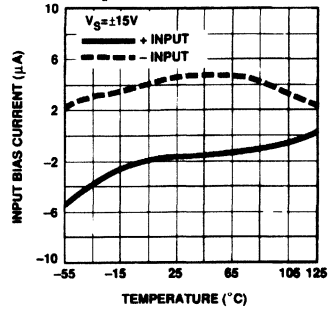
Output Settling Error vs Time, $V_S = \pm 5V$



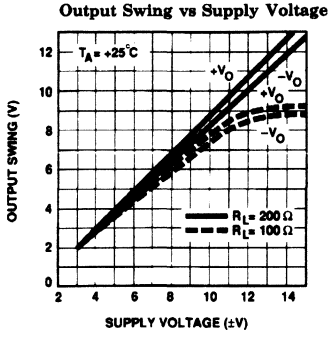
Input Offset Voltage vs Temperature



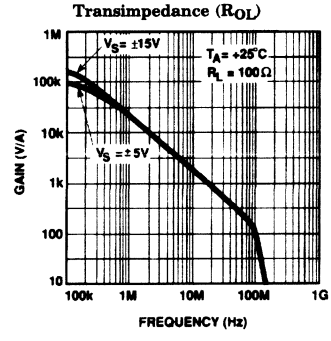
Input Bias Current vs Temperature



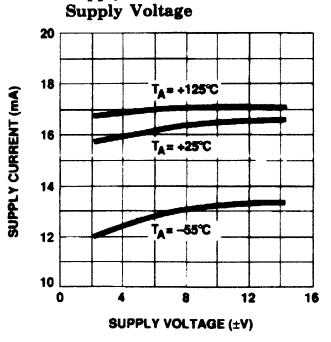
Output Swing vs Supply Voltage



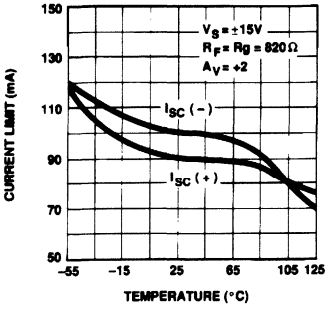
Transimpedance (R_{OL})



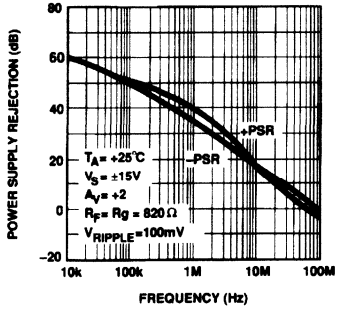
Supply Current vs Supply Voltage



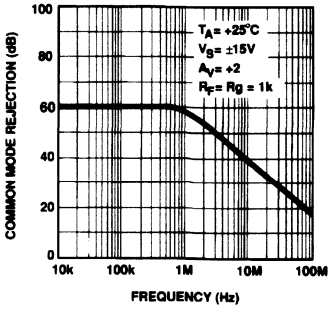
Current Limit vs Temperature



Power Supply Rejection vs Frequency



Common Mode Rejection vs Frequency

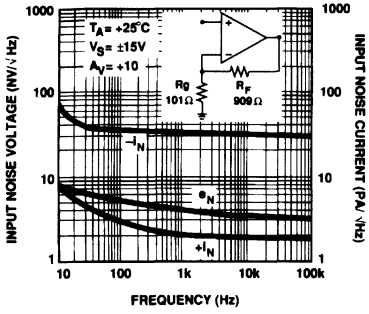


2030-10

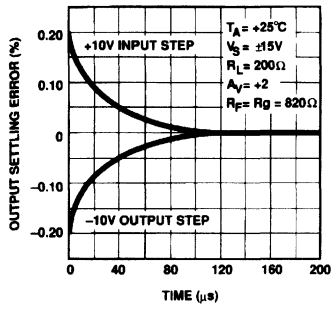
EL2030C
120 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

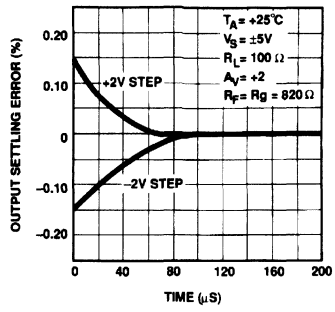
Equivalent Input Noise



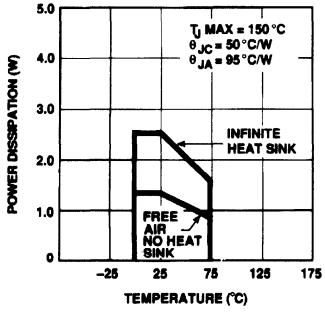
Long-Term Output Settling Error vs Time



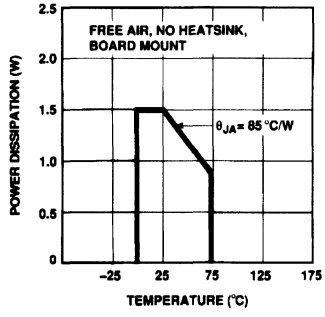
Long-Term Output Settling Error vs Time, V_S = ±5V



8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



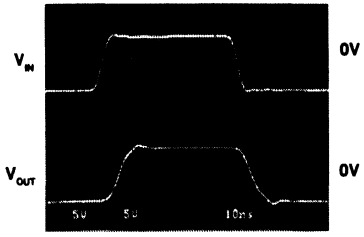
20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2030-11

Typical Performance Curves — Contd.

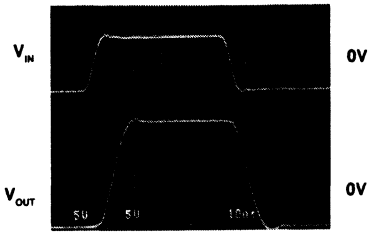
Large Signal Response



$A_V = +1$, $R_F = 1\ k\Omega$,
$R_L = 200\Omega$, $V_S = \pm 15V$

2030-12

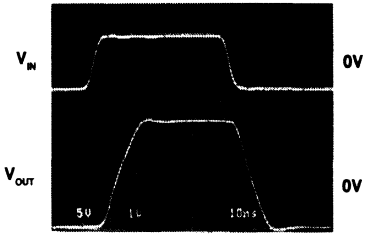
Large Signal Response



$A_V = +2$, $R_F = R_G = 820$,
$R_L = 200\Omega$, $V_S = \pm 15V$

2030-13

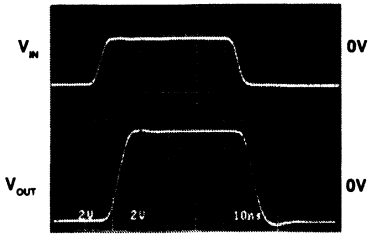
Large Signal Response



$A_V = +10$, $R_F = 750$, $R_G = 82\Omega$,
$R_L = 200\Omega$, $V_S = \pm 15V$

2030-14

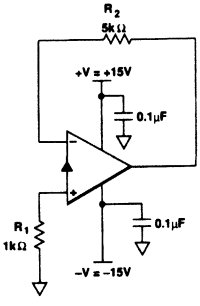
Large Signal Response



$A_V = +2$, $R_F = R_G = 750\Omega$,
$R_L = 200\Omega$, $V_S = \pm 15V$

2030-15

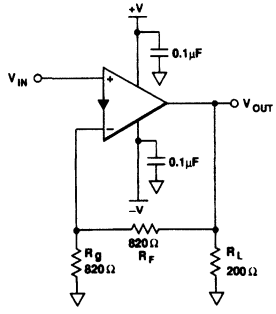
Burn-In Circuit



2030-16

ALL PACKAGES USE THE SAME SCHEMATIC.

Test Circuit



2030-17

EL2030C
120 MHz Current Feedback Amplifier

Application Information

Product Description

The EL2030 is a current mode feedback amplifier similar to the industry standard EL2020, but with greatly improved AC characteristics. Most significant among these are the extremely wide bandwidth and very low differential gain and phase. In addition, the EL2030 is fully characterized and tested at ±5V and ±15V supplies.

Power Supply Bypassing/Lead Dressing

It is important to bypass the power supplies of the EL2030 with 0.1 μF ceramic disc capacitors. Although the lead length is not critical, it should not be more the ½ inch from the IC pins. Failure to do this will result in oscillation, and possible destruction of the part. Another important detail is the lead length of the inputs. The inputs should be designed with minimum stray capacitance and short lead lengths to avoid ringing and distortion.

Latch Mode

The EL2030 can be damaged in certain circumstances resulting in catastrophic failure in which destructive supply currents flow in the device. Specifically, an input signal greater than ±5 volts at currents greater than 5 mA is applied to the device when the power supply voltages are zero will result in failure of the device.

In addition, the EL2030 will be destroyed or damaged in the same way for momentary power supply voltage reversals. This could happen, for example, during a power turn on transient, or if the power supply voltages were oscillating and the positive rail were instantaneously negative with respect to the negative rail or vice versa.

Differential Gain and Differential Phase

Composite video signals contain intensity, color, hue, timing and audio information in AM, FM, and Phase Modulation. These video signals pass through many stages during their production, processing, archiving and transmission. It is important that each stage not corrupt these signals to provide a "high fidelity" image to the end viewer.

An industry standard way of measuring the distortion of a video component (or system) is to measure the amount of differential gain and phase error it introduces. A 100 mV peak to peak sine wave at 3.58 MHz for NTSC (4.3 MHz for PAL), with 0V DC component serves as the reference. The reference signal is added to a DC offset, shifting the sine wave from 0V to 0.7V which is then applied to the device under test (DUT). The output signal from the DUT is compared to the reference signal. The Differential Gain is a measure of the change in amplitude of the sine wave and is measured in percent. The Differential Phase is a measure of the change in the phase of the sine wave and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak differential gain and differential phase errors. The test setup in Figure 1 was used to characterize the EL2030. For higher than NTSC and PAL frequencies, an alternate Differential Gain and Phase measurement can be made using an HP3577A Network Analyser and the setup shown in Figure 2. The frequency response is normalized to gain or phase with 0V DC at the input. From the normalized value a DC offset voltage is introduced and the Differential Gain or Phase is the deviation from the normalized value.

Video Applications

The video signals that must be transmitted for modest distances are usually amplified by a device such as the EL2030 and carried via coax cable. There are at least two ways to drive cables, single terminated and double terminated.

When driving a cable, it is important to terminate it properly to avoid unwanted signal reflections. Single termination (75Ω to ground at receive end) may be sufficient for less demanding applications. In general, a double terminated cable (75Ω in series at drive end and 75Ω to ground at receive end) is preferred since the impedance match at both ends of the line will absorb signal reflections. However, when double termination is used (a total impedance of 150Ω), the received signal is reduced by half; therefore, the amplifier is usually set at a gain of 2 or higher to compensate for attenuation.

Video Applications — Contd.

Video signals are 1V peak-peak in amplitude, from sync tip to peak white. There are 100 IRE (0.714V) of picture (from black to peak white of the transmitted signal) and 40 IRE (0.286V) of sync in a composite video signal (140 IRE = 1V).

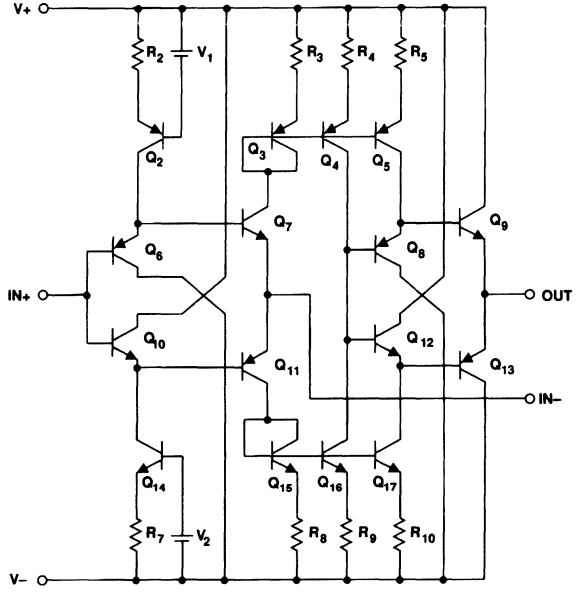
For video applications where a gain of two is used (double termination), the output of the video amplifier will be a maximum of 2V peak-peak. With ±5V power supply, the EL2030 output swing of 3.5V is sufficient to satisfy the video output swing requirements. The EL2030 can drive two double terminated coax cables under these conditions. With ±15V supplies, driving four double terminated cables is feasible.

Although the EL2030's video characteristics (differential gain and phase) are impressive with ±5V supplies at NTSC and PAL frequencies, it can be optimized when the supplies are increased to ±15V, especially at 30 MHz HDTV applications. This is primarily due to a reduction in internal parasitic junction capacitance with increased power supply voltage.

The following table summarizes the behavior of the EL2030 at ±5V and ±15V for NTSC. In addition, 30 MHz HDTV data is included. Refer to the differential gain and phase typical performance curves for more data.

$\pm V_S$	Rload	A_V	ΔGain	ΔPhase	Comments
15V	75Ω	1	0.02%	0.03°	Single terminated
15V	150Ω	1	0.02%	0.02°	Double terminated
5V	150Ω	1	0.05%	0.02°	Double terminated
15V	75Ω	2	0.02%	0.08°	Single terminated
15V	150Ω	2	0.01%	0.02°	Double terminated
5V	150Ω	2	0.03%	0.09°	Double terminated
15V	150Ω	2	0.05%	0.02°	HDTV, Double terminated

Equivalent Circuit



2030-18

EL2030 Macromodel

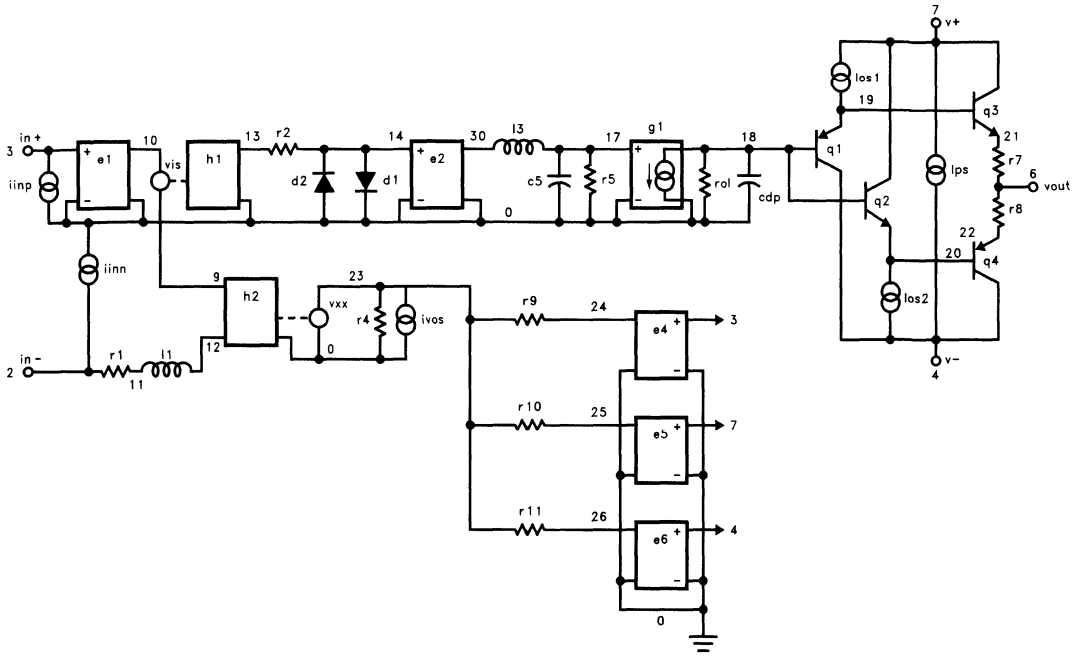
```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2030       3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 5µA
iinm 2 0 10µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4

.
```

EL2030 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 3 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.1nS)
.model qp pnp (is=5e-15 bf=100 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.266 bv=3.7 n=4)
.ends
```

EL2030C
120 MHz Current Feedback Amplifier

EL2030 Macromodel — Contd.



2030-19

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2038C
1 GHz Operational Amplifier

Features

- Wide gain-bandwidth—1 GHz
- High slew rate—1000 V/μs
- High power bandwidth—16 MHz
- Low offset voltage—0.5 mV
- Low supply current—13 mA
- Standard ±15V op amp supplies
- Large Open Loop Gain—15 kV/V (83 dB)
- MIL-STD-883 Rev. C Compliant
- Output voltage swing ±11V

Applications

- Pulse and Video amplifiers
- Wideband amplifiers
- High speed sample-hold circuits
- Local area Networks

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2038CN	0°C to +75°C	P-DIP	MDP0031

General Description

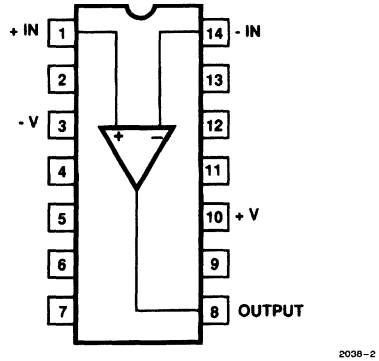
The EL2038 monolithic operational amplifier offers a 1 GHz gain-bandwidth and 1000 V/μs slew rate with excellent DC accuracy. The EL2038 is 67% faster than the HA2539 but with a typical power reduction of 35%. This patented amplifier is stable when driving capacitive loads and is well behaved when the output is overdriven. The EL2038 is compensated for closed loop gains ≥ 20. The EL2038 is fabricated with Elantec's Complementary Bipolar process, and is zener zap trimmed for low offset voltage.

Elantec's high speed amplifiers are widely used in military, video and medical applications. The EL2038 is especially well-suited for high speed video amplifiers, pulse detectors and wide bandwidth filters.

Elantec's facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing—Monolithic Products.*

Connection Diagram

EL2038CN



Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

EL2038C
1 GHz Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Operating Temperature Range	0°C to +75°C
Differential Input Voltage	6V	Operating Junction Temperature	150°C
Output Current	50 mA (Peak)	Lead Temperature (Soldering, 5 seconds)	300°C
	30 mA (Continuous)	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation	See Curves		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1 kΩ; unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage	+25°C		0.5	2	I	mV
		Full			6	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V	µV/°C
I_B	Bias Current	+25°C		5	15	I	µA
		Full			20	III	µA
I_{OS}	Offset Current	+25°C		1	4	I	µA
		Full			6	III	µA
R_{IN}	Input Resistance	+25°C		10		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V	pF
V_{CM}	Common Mode Input Range	Full	±11	±12		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	+25°C		6		V	nV/$\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain	+25°C	10k	15k		I	V/V
	(Notes 1, 2)	Full	5k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)	Full	60	90		II	dB
V_O	Output Voltage Swing (Note 1)	Full	±11	±12		II	V

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1\ k\Omega$; unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_O	Output Current (Note 13)	Full	±25	±50		II	mA
R_O	Output Resistance	+25°C		30		V	Ω
I_S	Supply Current	Full		13	17	II	mA
PSRR	Power Supply Rejection Ratio (Note 8)	Full	60	85		II	dB

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1\ k\Omega$, unless otherwise specified (Note 14)

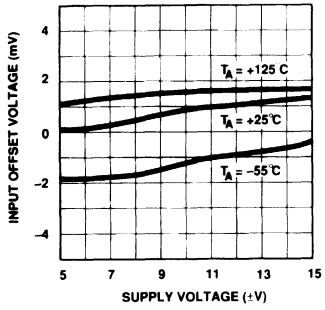
Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
GBW	Gain-Bandwidth Product (Notes 4, 5)	+25°C	0.875	1.1		III	GHz
FPBW	Full Power Bandwidth (Notes 1, 2, 6)	+25°C	13.5	16		III	MHz
t_r	Rise Time (Notes 7, 9)	+25°C		4	5	III	ns
OS	Overshoot (Notes 7, 10)	+25°C		30	40	III	%
SR	Slew Rate (Note 7)	+25°C	750	1000		III	V/μs
t_s	Settling Time (Notes 11, 12) 10V Step to 0.1%	+25°C		100		V	ns

Note 1: $R_L = 1k$, $C_L < 10\ pF$.
Note 2: $V_O = \pm 10V$.
Note 3: Two tests are performed, $V_{CM} = 0V$ to $+10V$ and $V_{CM} = 0V$ to $-10V$.
Note 4: $V_O = 90\ mV$.
Note 5: $A_V = 20$.
Note 6: Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew rate}}{2\pi\ V_{peak}}$.
Note 7: Refer to Test Circuits section of data sheet.
Note 8: Two tests are performed, V+ = +15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 9: Risetime measurement of 25% to 75% with $V_{OUT} = 200\ mV$.
Note 10: $\Delta V_O = 200\ mV$.
Note 11: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 12: $A_V = -20$, $R_L = 1k$.
Note 13: $R_L = 200\Omega$.
Note 14: 100% AC tested commercial parts available. Consult factory.

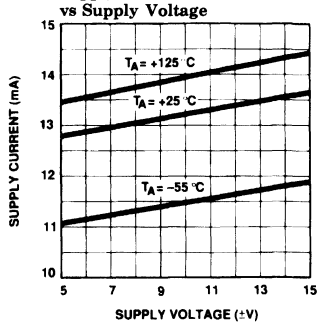
EL2038C
1 GHz Operational Amplifier

Typical Performance Curves

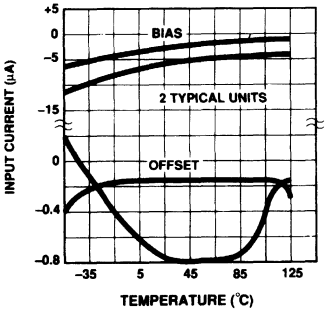
Input Offset Voltage vs Supply Voltage



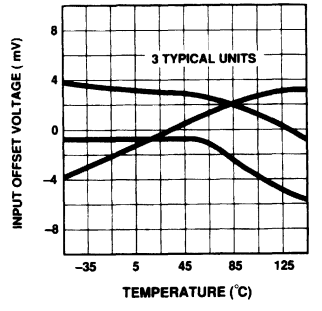
Supply Current vs Supply Voltage



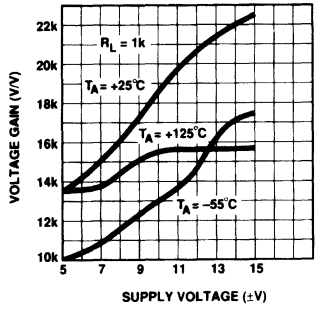
Input Currents vs Temperature



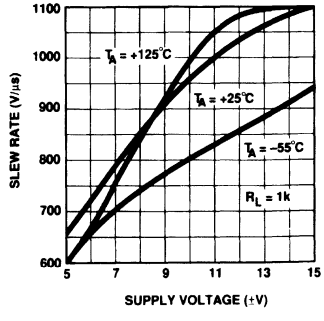
Input Offset Voltage vs Temperature



Voltage Gain vs Supply Voltage



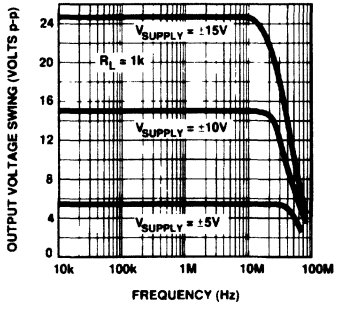
Slew Rate vs Supply Voltage



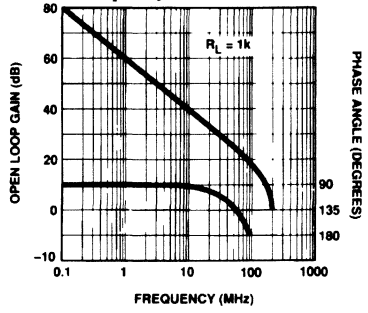
2038-3

Typical Performance Curves — Contd.

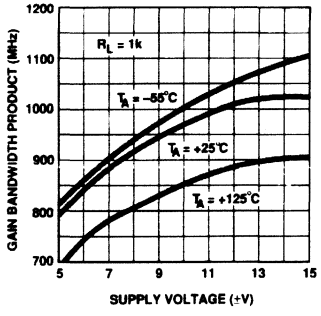
Output Voltage Swing vs Frequency



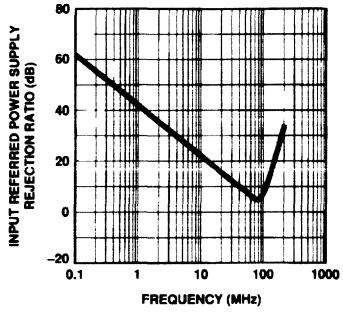
Open Loop Voltage Gain vs Frequency



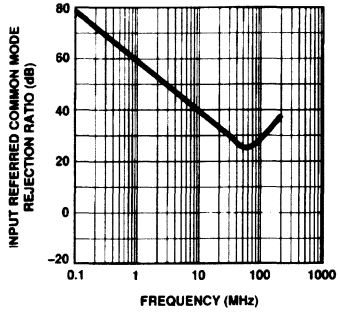
Gain Bandwidth Product at 10 MHz vs Frequency



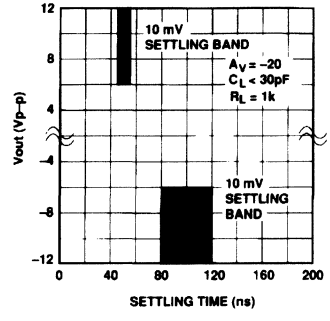
Input Referred Power Supply Rejection Ratio vs Frequency



Input Referred Common Mode Rejection Ratio vs Frequency



Settling Time

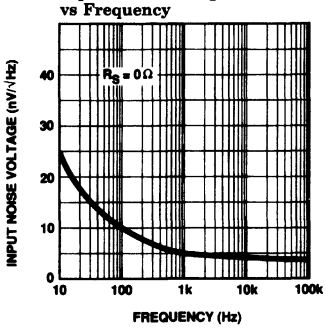


2038-4

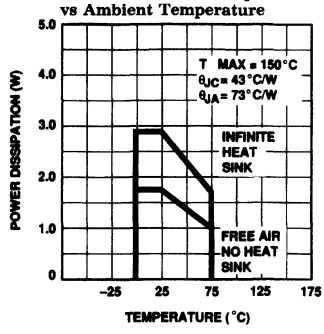
EL2038C
1 GHz Operational Amplifier

Typical Performance Curves — Contd.

Input Noise Voltage vs Frequency

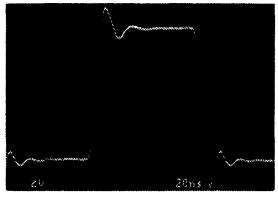


14-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature



2038-5

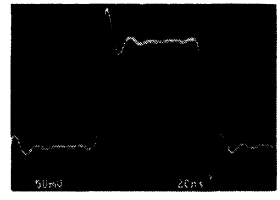
Large Signal Response



V_{IN} = ±0.25V
V_O = ±5V

2038-6

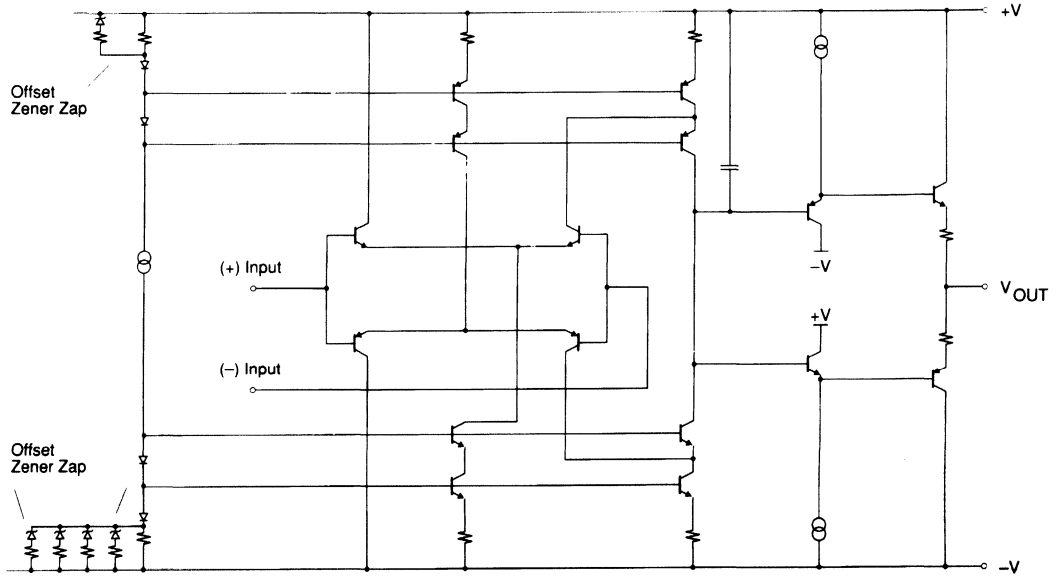
Small Signal Response



V_{IN} = ±5 mV
V_O = ±100 mV

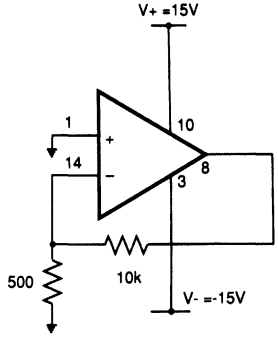
2038-7

Simplified Schematic



2038-8

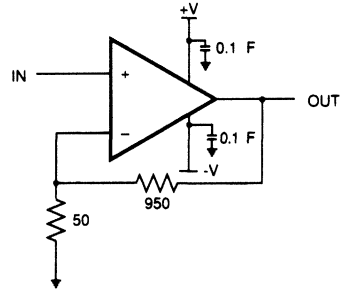
Burn-In Circuit



2038-9

Pin numbers are for 14-Lead CerDIP. All packages use the same schematic.

Test Circuit



$A_V = 20$

$C_L = 10pF$ Scope Probe

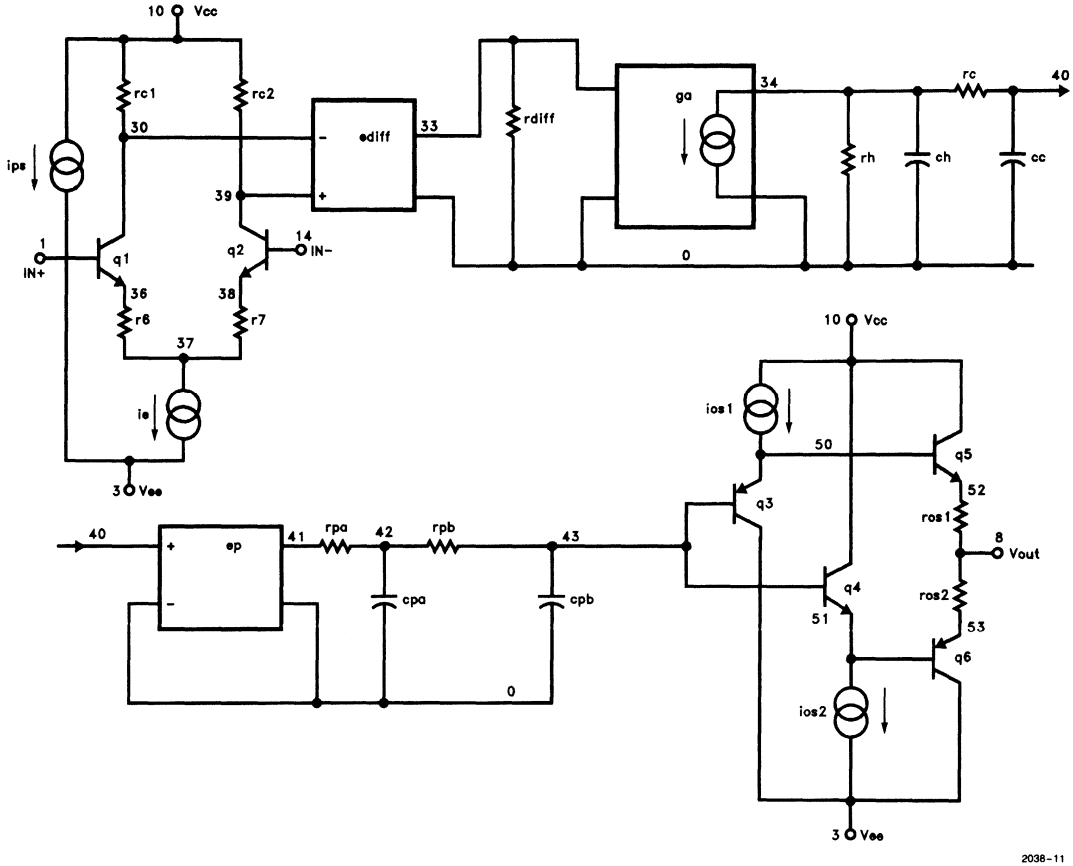
2038-10

EL2038C
1 GHz Operational Amplifier

EL2038 Macromodel

```
* Connections:      + input
*                   |     - input
*                   |     |     + Vsupply
*                   |     |     |     - Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2038       1     14    10    3     8
* Input Stage
ie 37 8 2mA
r6 36 37 65
r7 38 37 65
rc1 10 30 75
rc2 10 39 75
q1 30 1 36 qn
q2 39 14 38 qna
ediff 33 0 39 30 7.25
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 5.2m
rh 34 0 .525Meg
ch 34 0 0.5pF
rc 34 40 600
cc 40 0 4pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 17pF
rpb 42 43 50
cpb 43 0 10pF
* Output Stage
ios1 10 50 1.25mA
ios2 51 3 1.25mA
q3 3 43 50 qp
q4 10 43 51 qn
q5 10 50 52 qn
q6 3 51 53 qp
ros1 52 8 25
ros2 8 53 25
* Power Supply Current
ips 10 3 9.2mA
* Models
.model qn npn(is = 800.0E - 18 bf = 200 tf = 0.2nS)
.model qna npn(is = 864E - 18 bf = 250 tf = 0.2nS)
.model qp pnp(is = 800E - 18 bf = 60 tf = 0.2nS)
.ends
```

EL2038 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2039C/EL2040C

Very High Slew Rate Wideband Operational Amplifier

Features

- Low offset voltage—0.5 mV typ., 2 mV max
- Low supply current—13 mA typ., 17 mA max
- High slew rate—
  EL2039—600 V/μs
  EL2040—400 V/μs
- Large open loop gain—15 kV/V (83 dB)
- Wide gain-bandwidth—
  EL2039—600 MHz
  EL2040—400 MHz
- High power bandwidth—
  EL2039—9.5 MHz
  EL2040—6.3 MHz
- Output voltage swing—±11V
- MIL-STD-883 Rev. C compliant
- Improved replacements for HA2539 and HA2540

Applications

- Pulse and video amplifiers
- Wideband amplifiers
- High speed sample-hold circuits
- Local area networks

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2039CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2040CN	0°C to +75°C	14-Pin P-DIP	MDP0031

General Description

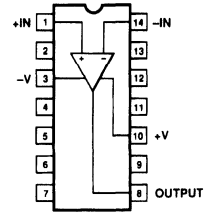
The EL2039 and EL2040 monolithic operational amplifiers are pin compatible with the HA2539 and HA2540, but have patented circuitry for improved dynamic performance and DC accuracy, and a typical power reduction of 35%. Additionally, these Elantec amplifiers are stable when driving capacitive loads and are well behaved when the output is overdriven. Both devices are compensated for closed loop gains ≥ 10. The EL2039 is the fastest of the series with a 600 V/μs slew rate and 600 MHz gain-bandwidth product. The EL2040 has a 400 V/μs slew rate and 400 MHz gain-bandwidth product. The EL2039 and EL2040 are fabricated with Elantec's Complementary Bipolar process and are zener zap trimmed for low offset voltage.

Elantec's high speed amplifiers are widely used in military, video and medical applications. They are especially suited for high speed video amplifiers, pulse detectors, and wide bandwidth filters.

Elantec's EL2039C and EL2040C comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing—Monolithic Products.*

Connection Diagrams

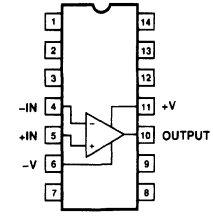
EL2039 DIP



2039-1

Top View

EL2040 DIP



2039-2

Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

EL2039C/EL2040C

Very High Slew Rate Wideband Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	35V
V_{DIFF}	Differential Input Voltage	6V
I_{OP}	Output Current, Peak	50 mA
I_{OC}	Output Current, Continuous	25 mA
P_D	Internal Power Dissipation	See Curves
T_A	Operating Temperature Range	0°C to +75°C
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature	−65°C to +150°C
T_{LT}	Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 1 kΩ, unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	25°C		0.5	2	I	mV
		Full			6	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V	µV/°C
I_B	Bias Current	25°C		5	15	I	µA
		Full			20	III	µA
I_{OS}	Offset Current	25°C		1	4	I	µA
		Full			6	III	µA
R_{IN}	Input Resistance	25°C		10		V	kΩ
C_{IN}	Input Capacitance	25°C		1		V	pF
V_{CM}	Common Mode Range	Full	±11	±12		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		6		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Note 1)	25°C	10k	15k		I	V/V
		Full	5k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 2)	Full	60	90		II	dB
V_O	Output Voltage Swing	Full	±11	±12		II	V
I_O	Output Current (Note 11)	Full	±25	±50		II	mA
R_O	Output Resistance	25°C		30		V	Ω
I_S	Supply Current	Full		13	17	II	mA
PSRR	Power-Supply Rejection Ratio (Note 7)	Full	60	85		II	dB

EL2039C/EL2040C
Very High Slew Rate Wideband Operational Amplifier

AC Electrical Characteristics—EL2039

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
GBW	Gain-Bandwidth Product (Notes 3, 4)	25°C		600		V	MHz
FPBW	Full-Power Bandwidth (Notes 1, 5, 8)	25°C	8.7	9.5		I	MHz
t_r	Rise Time (Note 6)	25°C		4		V	ns
OS	Overshoot (Note 6)	25°C		35		V	%
SR	Slew Rate (Note 6)	25°C	550	600		I	V/μs
ts	Settling Time (Note 6) 10V Step to 0.1%	25°C		100		V	ns

AC Electrical Characteristics—EL2040

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
GBW	Gain-Bandwidth Product (Notes 3, 4)	25°C		400		V	MHz
FPBW	Full-Power Bandwidth (Notes 1, 5, 8)	25°C	5.5	6		I	MHz
t_r	Rise Time (Note 6)	25°C		5		V	ns
OS	Overshoot (Note 6)	25°C		15		V	%
SR	Slew Rate (Note 6)	25°C	350	400		I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.1%	25°C		70		V	ns

Note 1: $V_O = \pm 10V$.

Note 2: Two tests are performed, $V_{CM} = 0V$ to $+10V$ and $V_{CM} = 0V$ to $-10V$.

Note 3: $V_O = 90$ mV.

Note 4: $A_V = 10$.

Note 5: Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$.

Note 6: Refer to Test Circuits section of data sheet.

Note 7: Two tests are performed. $V+ = +15V$, and $V-$ is changed from $-5V$ to $-15V$. $V- = -15V$, and $V+$ is changed from $+5V$ to $+15V$.

Note 8: $R_L = 1$ kΩ.

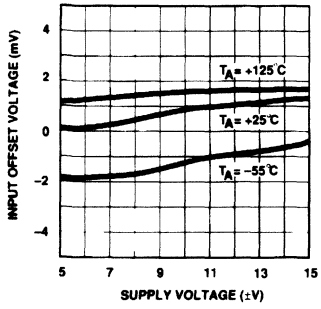
Note 9: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.

Note 10: $A_V = -10$, $R_L = 1$k.

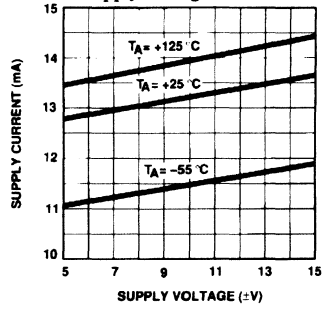
Note 11: $R_L = 200\Omega$.

EL2039/EL2040 Typical DC Performance Curves

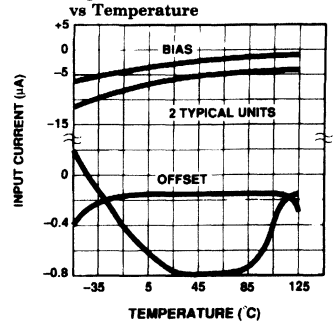
Input Offset Voltage vs Supply Voltage



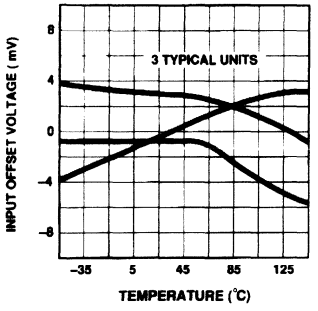
Supply Current vs Supply Voltage



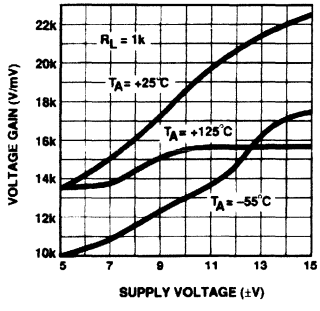
Input Currents vs Temperature



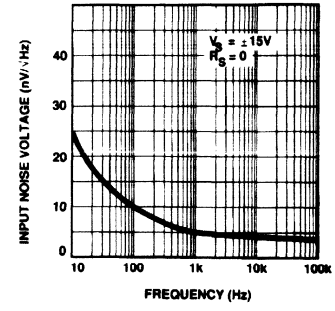
Input Offset Voltage vs Temperature



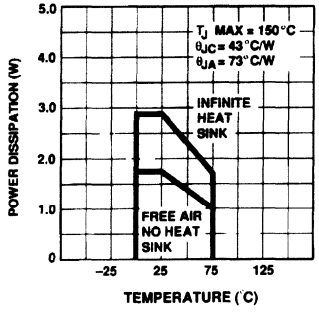
Voltage Gain vs Supply Voltage



Input Noise Voltage vs Frequency



14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature

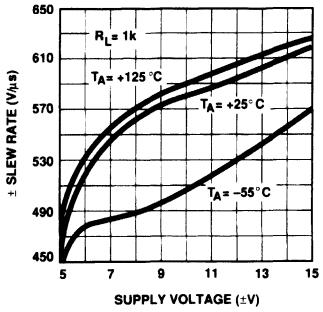


2039-5

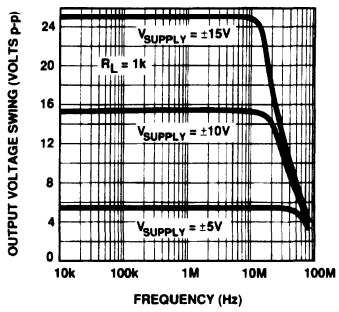
EL2039C/EL2040C
Very High Slew Rate Wideband Operational Amplifier

EL2039 Typical AC Performance Curves

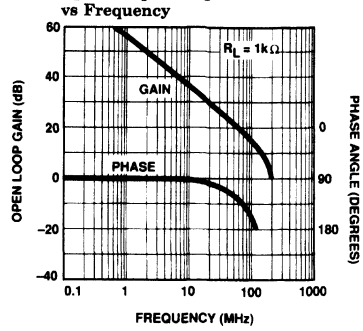
Slew Rate vs Supply Voltage



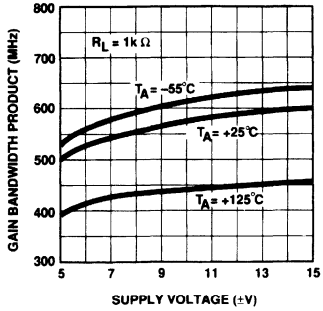
Output Voltage Swing vs Frequency



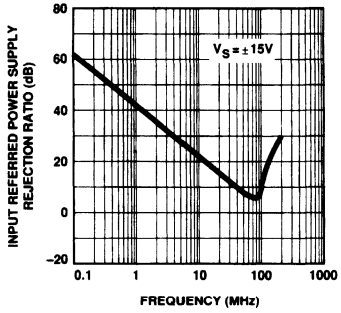
Open Loop Voltage Gain vs Frequency



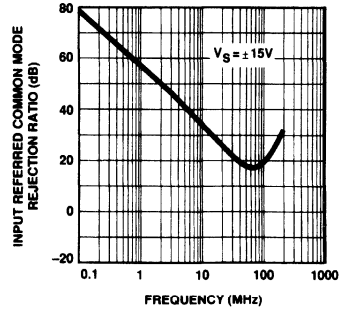
Gain Bandwidth Product at 10 MHz vs Supply Voltage



Input Referred Power Supply Rejection Ratio vs Frequency

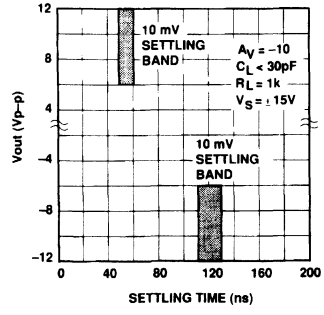


Input Referred Common Mode Rejection Ratio vs Frequency



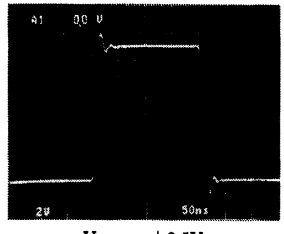
2039-6

Settling Time



2039-7

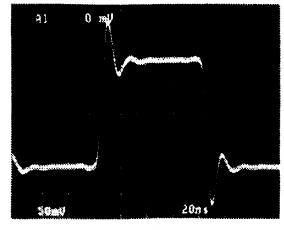
Large Signal Response



V_{IN} = ±0.5V
V_O = ±5V

2039-8

Small Signal Response

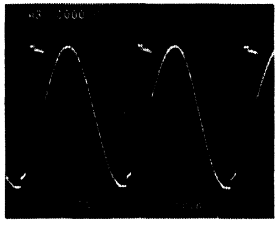


V_{IN} = ±10 mV
V_O = ±100 mV

2039-9

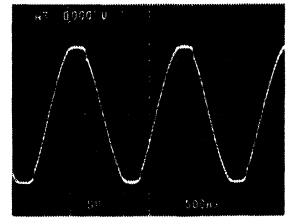
EL2039 Typical AC Performance Curves — Contd.

HA2539 at Onset of Clipping



2039-10

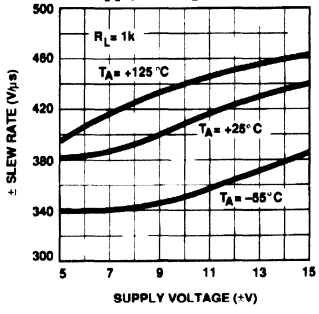
EL2039 at Onset of Clipping



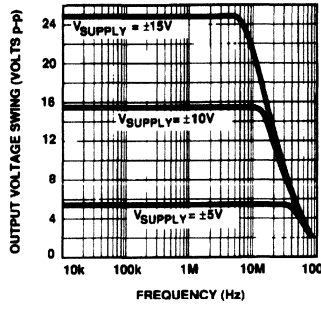
2039-11

EL2040 Typical AC Performance Curves

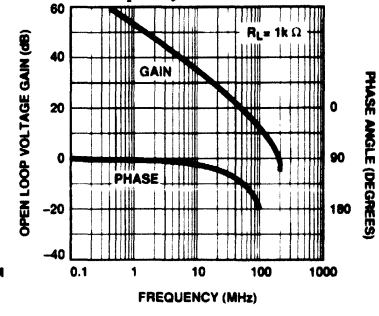
±Slew Rate vs Supply Voltage



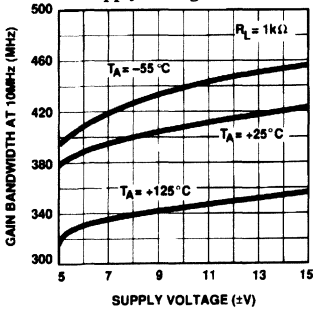
Output Voltage Swing vs Frequency



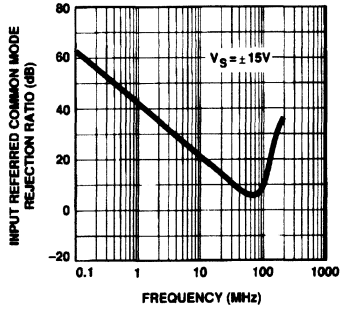
Open Loop Voltage Gain vs Frequency



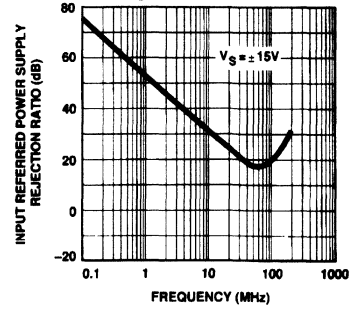
Gain Bandwidth Product at 10 MHz vs Supply Voltage



Input Referred Common Mode Rejection Ratio vs Frequency



Input Referred Power Supply Rejection Ratio vs Frequency



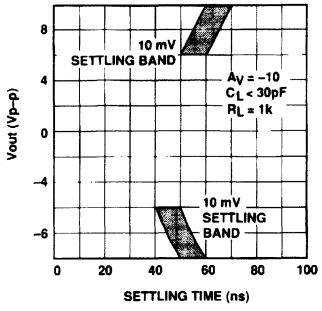
2039-12

EL2039C/EL2040C

Very High Slew Rate Wideband Operational Amplifier

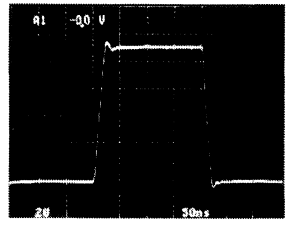
EL2040 Typical AC Performance Curves — Contd.

Settling Time



2039-13

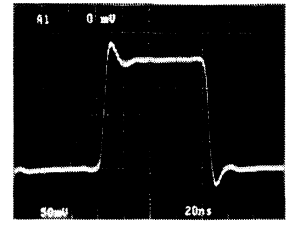
Large Signal Response



V_{IN} = ±0.5V
V_O = +5V

2039-14

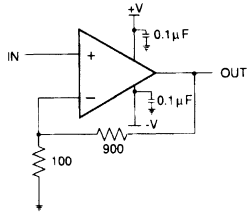
Small Signal Response



V_{IN} = ±10 mV
V_O = ±100 mV

2039-15

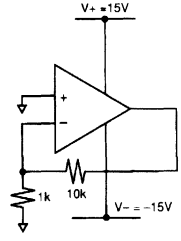
Test Circuit



2039-16

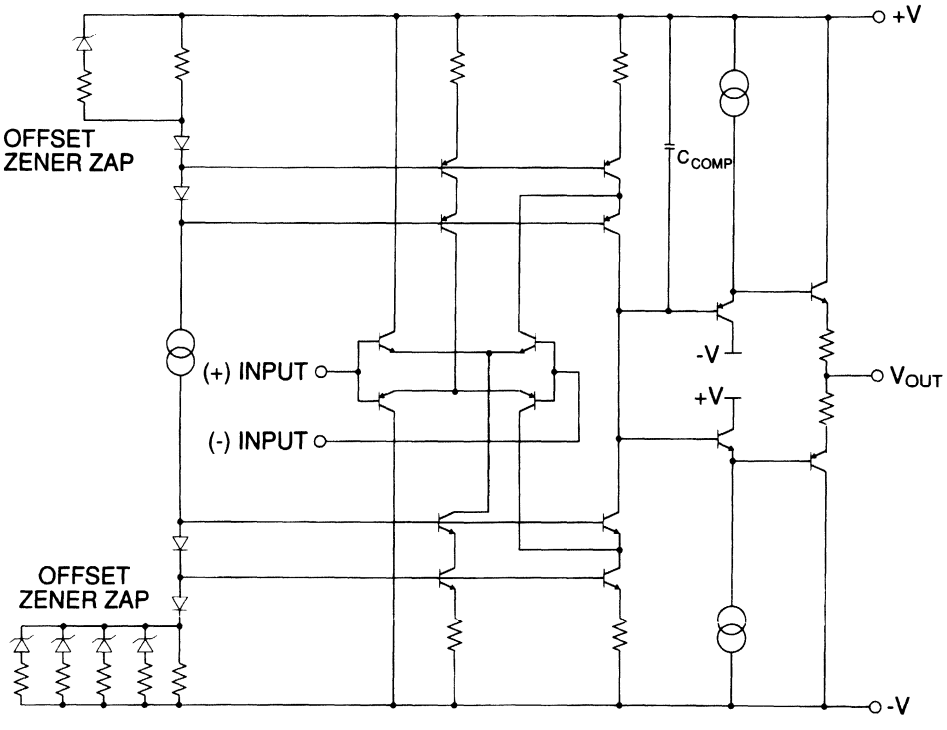
A_V = 10
C_L = 10 pF Scope Probe

Burn-In Circuit



2039-17

Schematic

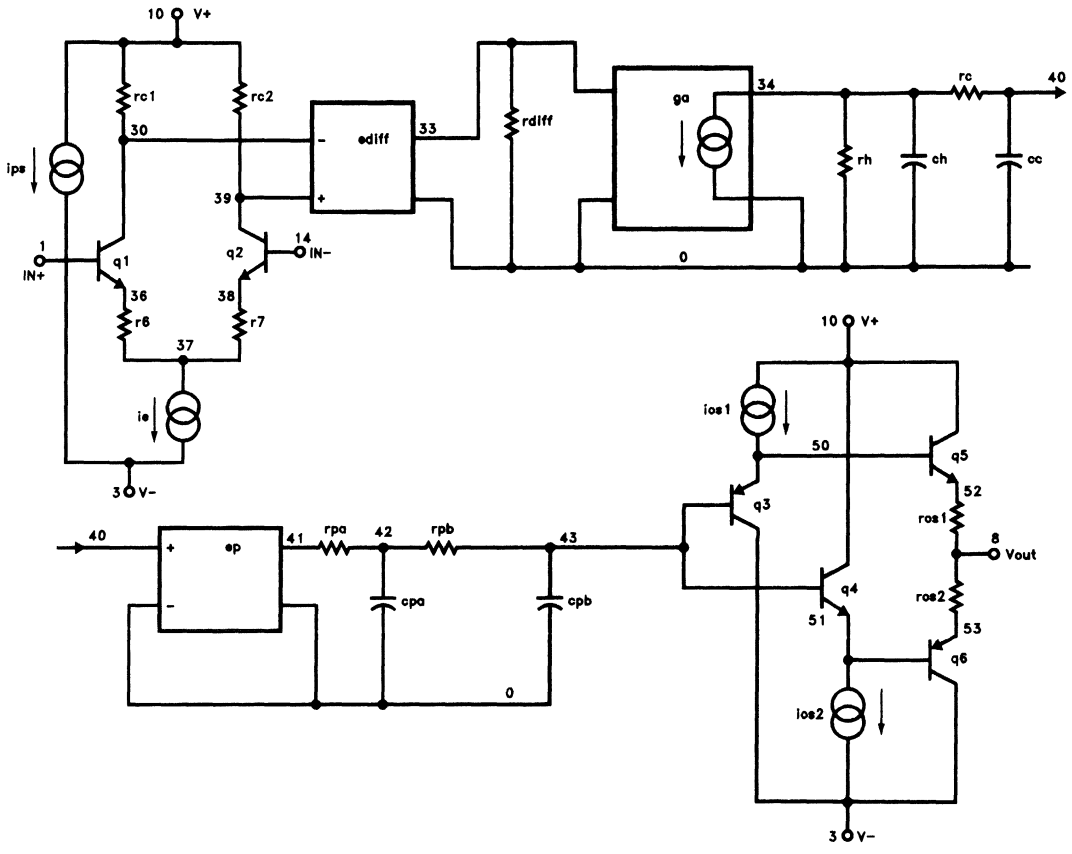

+V
OFFSET
ZENER ZAP
C_{COMP}
(+) INPUT
(-) INPUT
-V
+V
V_{OUT}
OFFSET
ZENER ZAP
-V
2039-18

EL2039C/EL2040C
Very High Slew Rate Wideband Operational Amplifier

EL2039 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2039       1     14    10    3     8
* Input Stage
ie 37 3 1.7mA
r6 36 37 60
r7 38 37 60
rc1 10 30 75
rc2 10 39 75
q1 30 1 36 qn
q2 39 14 38 qna
ediff 33 0 39 30 7.25
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 5.2m
rh 34 0 .525Meg
ch 34 0 1.5pF
rc 34 40 600
cc 40 0 7pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 7pF
rpb 42 43 50
cpb 43 0 3pF
* Output Stage
ios1 10 50 1.25mA
ios2 51 3 1.25mA
q3 3 43 50 qp
q4 10 43 51 qn
q5 10 50 52 qn
q6 3 51 53 qp
ros1 52 8 25
ros2 8 53 25
* Power Supply Current
ips 10 3 9.5mA
* Models
.model qn npn(is=800.0E-18 bf=170 tf=0.2nS)
.model qna npn(is=864E-18 bf=200 tf=0.2nS)
.model qp pnp(is=800E-18 bf=60 tf=0.2nS)
.ends
```

EL2039 Macromodel — Contd.

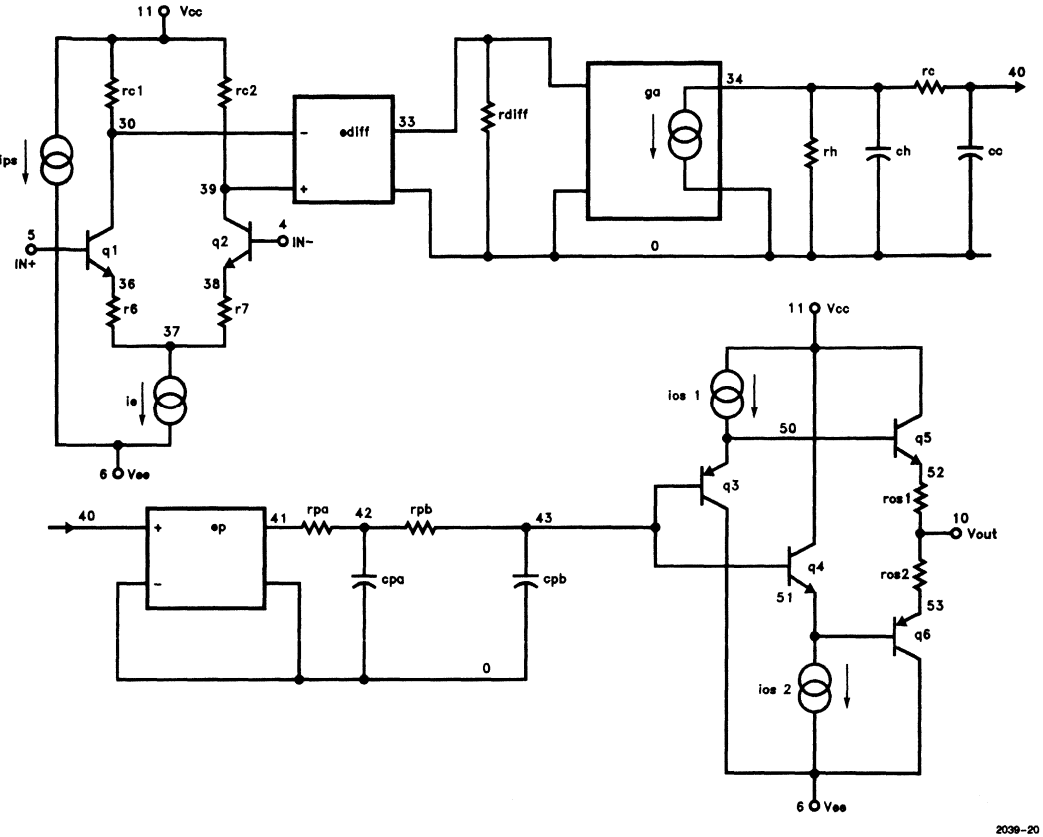


EL2039C/EL2040C
Very High Slew Rate Wideband Operational Amplifier

EL2040 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2040       5     4     11    6     10
* Input Stage
ie 37 6 1.3mA
r6 36 37 60
r7 38 37 60
rc1 11 30 75
rc2 11 39 75
q1 30 5 36 qn
q2 39 4 38 qna
ediff 33 0 39 30 7.25
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 5.2m
rh 34 0 .525Meg
ch 34 0 1.5pF
rc 34 40 600
cc 40 0 7pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 7pF
rpb 42 43 50
cpb 43 0 3pF
* Output Stage
ios1 11 50 1.25mA
ios2 51 6 1.25mA
q3 6 43 50 qp
q4 11 43 51 qn
q5 11 50 52 qn
q6 6 51 53 qp
ros1 52 10 25
ros2 10 53 25
* Power Supply Current
ips 11 6 9.5mA
* Models
.model qn npn(is=800.0E-18 bf=130 tf=0.2nS)
.model qna npn(is=864E-18 bf=150 tf=0.2nS)
.model qp pnp(is=800E-18 bf=60 tf=0.2nS)
.ends
```

EL2040 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2041C

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Features

- Open loop unity bandwidth—90 MHz
- Unity gain stable
- High gain—10k typ.
- High slew rate—250 V/μs
- Low offset voltage—0.5 mV typ., 2 mV max.
- Low supply current—13 mA typ., 17 mA max.
- Wide supply operation ±5V to ±15V
- Output voltage swing—±11V
- Power bandwidth—4 MHz
- Fast settling time
- Pin compatible with HA2541

Applications

- Pulse and video amplifiers
- Fast integrators
- Wideband filters
- High speed sample and hold circuits
- Fast, precise D/A converter output amplifier
- High speed A/D input amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2041CN	0°C to +75°C	8-Pin P-DIP	MDP0031

General Description

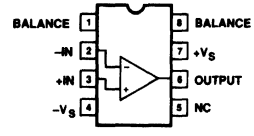
The EL2041 is a unity gain stable monolithic operational amplifier with a 90 MHz open loop unity bandwidth. This unprecedented bandwidth is accomplished with a 45° phase margin and a 6.5 dB gain margin. Unlike other wideband amplifiers, the patented EL2041 operates on standard ±15V supplies, swings ±11V at its output, and maintains an 80 dB open loop gain into a 1k load.

In addition, the EL2041 has a 250 V/μs slew rate while drawing only 13 mA of supply current. Zener Zap techniques are used to trim the offset voltage to 2 mV maximum, making the EL2041 an excellent choice for applications requiring both speed and accuracy.

Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing—Monolithic Products.*

Connection Diagram

Plastic DIP



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Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,837,523

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−		35V
Differential Input Voltage		6V
Output Current	Continuous	25 mA
	Peak	50 mA
Internal Power Dissipation	See Curves	
Operating Temperature Range		0°C to +75°C

Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 5 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTS77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 1 kΩ, unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage	+25°C		0.5	5	I	mV
		Full			10	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		20		V	µV/°C
I_B	Bias Current	+25°C		5	15	I	µA
		Full			20	III	µA
I_{OS}	Offset Current	+25°C		1	4	I	µA
		Full			6	III	µA
R_{IN}	Input Resistance	+25°C		20		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V	pF
V_{CM}	Common Mode Input Range	Full	±8	±11		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω	+25°C		10		V	$nV\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain (Notes 1, 2)	+25°C	5k	10k		I	V/V
		Full	4k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 3)	Full	60	80		II	dB
V_O	Output Voltage Swing	Full	±11	±12		II	V
I_O	Output Current (Note 11)	Full	±25	±50		I	mA
R_O	Output Resistance	+25°C		40		V	Ω
I_S	Supply Current	Full		13	17	II	mA
PSRR	Power Supply Rejection Ratio (Note 7)	Full	60	80		II	dB

EL2041C

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

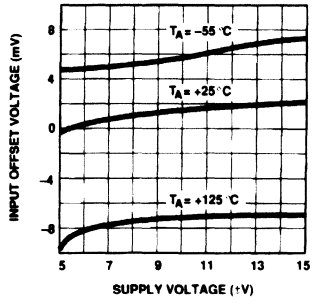
AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 1\ k\Omega$, unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
f_u	Open Loop Unity Bandwidth (Notes 4, 10)	+25°C		90		V	MHz
FPBW	Full Power Bandwidth (Notes 1, 5)	+25°C	2.8	4		I	MHz
t_r	Rise Time (Note 6)	+25°C		4		V	ns
OS	Overshoot (Note 6)	+25°C		10		V	%
SR	Slew Rate (Note 6)	+25°C	180	250		I	V/μs
t_s	Settling Time (Notes 8, 9, 10) 10V Step to 0.05%	+25°C		90		V	ns

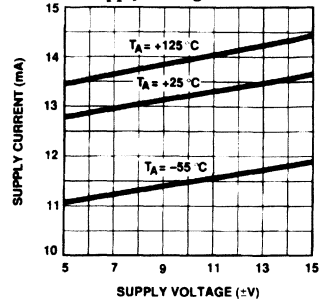
Note 1: $V_O = \pm 10V$.
Note 2: $R_L = 1\ k\Omega$.
Note 3: Two tests are performed. $V_{CM} = 0V$ to $+8V$ and $V_{CM} = 0V$ to $-8V$.
Note 4: $V_O = 90$ mV.
Note 5: Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi\ Vpeak}$.
Note 6: Refer to Test Circuits section of data sheet.
Note 7: Two tests are performed. V+ = +15V, and V− is changed from −7V to −15V. V− = −15V, and V+ changed from +7 to +15V.
Note 8: Settling time measurements are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN, September 19, 1985.
Note 9: $A_V = +1$, $R_L = 1k$.
Note 10: 200Ω, 20 pF output snubber, see application section.
Note 11: $R_L = 200\Omega$.

Typical Performance Curves

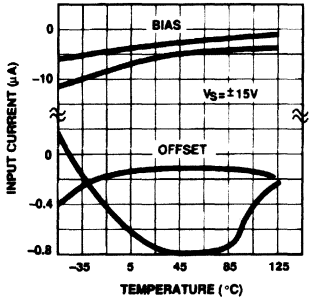
Input Offset Voltage
vs Supply Voltage



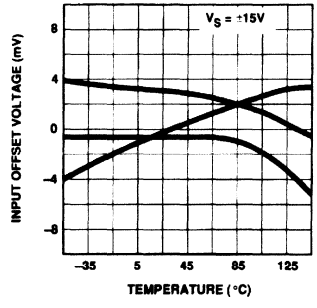
Supply Current
vs Supply Voltage



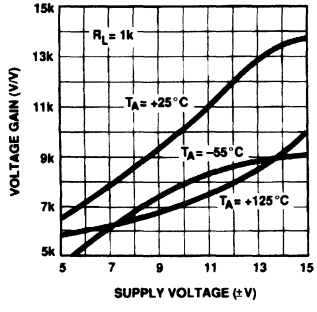
Input Current
vs Temperature
(2 Typical units)



Input Offset Voltage
vs Temperature
(3 Typical units)



Voltage Gain
vs Supply Voltage



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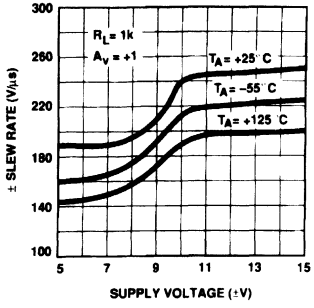
EL2041C

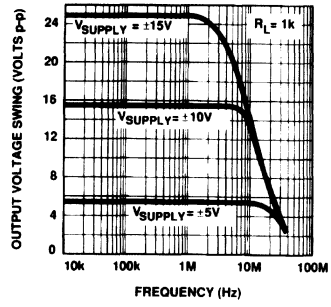
Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Typical Performance Curves — Contd.

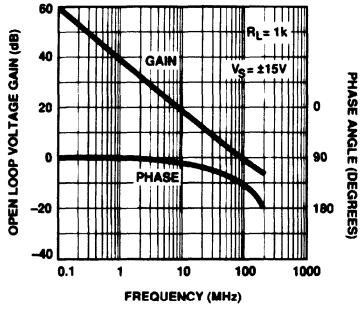
Slew Rate vs Supply Voltage



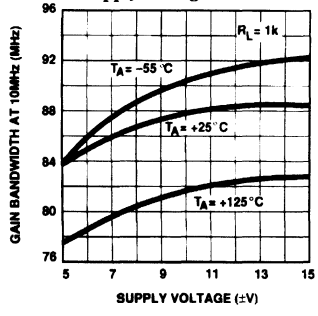
Output Voltage Swing vs Frequency



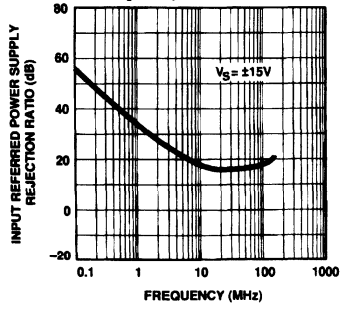
Open Loop Voltage Gain vs Frequency



Gain Bandwidth Product at 10 MHz vs Supply Voltage



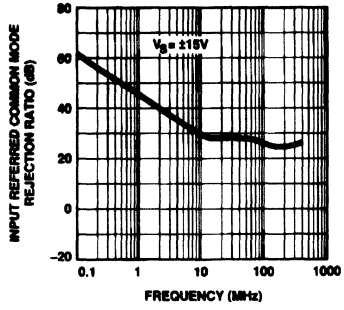
Input Referred Power Supply Rejection Ratio vs Frequency



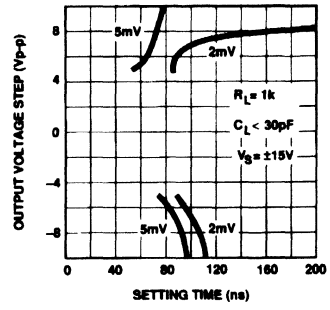
2041-5

Typical Performance Curves — Contd.

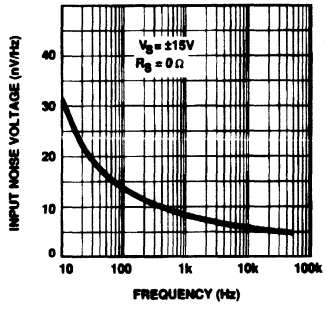
Input Referred Common Mode Rejection Ratio vs Frequency



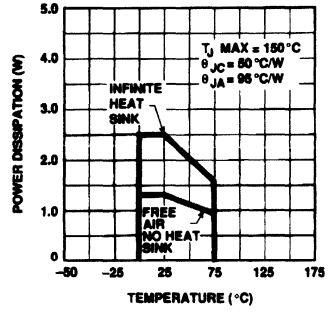
Settling Time Av = +1



Input Noise Voltage vs Frequency



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



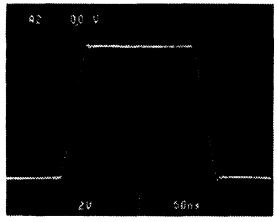
2041-6

EL2041C

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Typical Performance Curves — Contd.

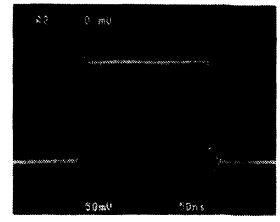
Large Signal Response



2041-7

$A_V = +1$
$V_{IN} = \pm 5V$
$V_O = \pm 5V$

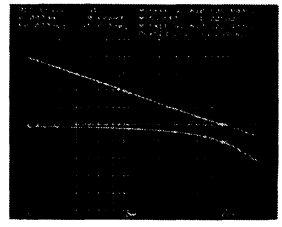
Small Signal Response



2041-8

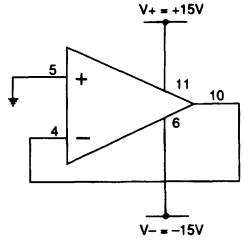
$A_V = +1$
$V_{IN} = \pm 100\ mV$
$V_O = \pm 100\ mV$

Open Loop Gain and Phase Response



2041-9

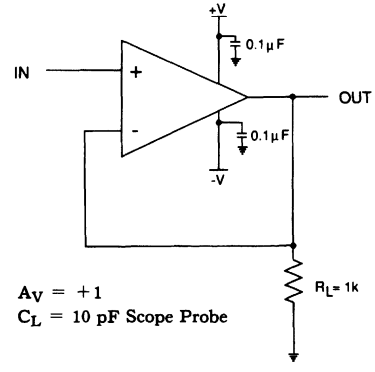
Burn-In Circuit



2041-10

Pin numbers are for 14-Lead cerDIP. Burn-in circuit is identical for all package types.

Test Circuit



$A_V = +1$
$C_L = 10\ pF$ Scope Probe

2041-11

Application Hints

Product Description

The EL2041 is a wideband monolithic operational amplifier built on Elantec's proprietary Complementary Bipolar process. Unlike many ±5V wideband op amps available today, the EL2041 operates from ±5V to ±15V and is capable of driving ±11V at its output. The large signal swing and open loop voltage gain of 80 dB with a 1 kΩ load, differentiate the EL2041 from other op amps that do not have sufficient load isolation. Another unusual characteristic of the amplifier is the extremely wide unity gain bandwidth of 90 MHz. This bandwidth is accomplished with a 45° phase margin, a 6.5 dB gain margin, and a slew rate of 250 V/μs. These AC characteristics are realized with a 13 mA supply current, which means lower power dissipation and higher reliability than competing products.

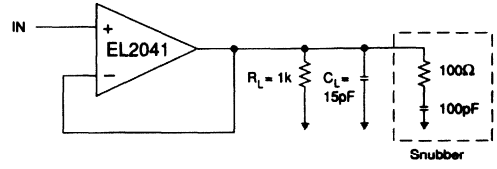
Power Supply Bypass

It is important to bypass the power supplies of the EL2041 with 0.1 μF or 0.01 μF ceramic disc capacitors. Failure to do this will result in oscillation or signal distortion. Although the lead length is not critical, it should not be more than ½" from the IC pins.

Capacitive Loading

Like all high speed op amps, the EL2041 is sensitive to capacitive loading. There are at least two ways to approach this problem: The use of a snubber (Q spoiler), or the use of feedback isolation.

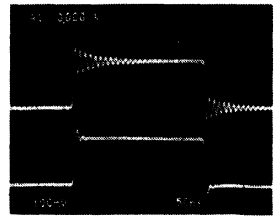
The first approach is to consider the output stage of the amplifier as a highly inductive element due to the application of feedback. When this output stage is loaded with a capacitance a natural resonance occurs. By putting a series RC at the output of the amplifier, the energy of the tank can be absorbed, quenching the instability. The way to select the RC values for the Q spoiler is to drive a small signal (few 100 mV) squarewave into the desired capacitive load. Place a small resistor (few 100Ω) at the output to ground, and note the reduction in ringing. When the desired response has been obtained, the capacitance value can be chosen. Start with a few 10's of pico farads in series with the selected resistor. Adjust the capacitor for the desired response. The capacitor value cannot be chosen arbitrarily large because of the reduction in open loop gain the series resistor will cause. In the example shown, the effects of a 15 pF load have been eliminated. Larger values of load capacitance can be tamed with a different RC value.



2041-12

2041-13

Frequency Response +6 dB Peak without Snubber and +2 dB with 200Ω, 20 pF Snubber.



2041-14

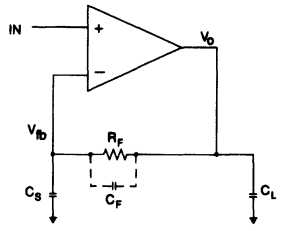
Top Trace is without Snubber; Bottom Trace is 100Ω, 100 pF Snubber.

Another way to look at the effect of capacitive loading is in the frequency domain. The open loop output impedance of the EL2041 is about 40Ω; when the output is loaded with 15 pF, an output pole is formed at 265 MHz. This pole sounds innocent enough until it's realized that it causes a phase shift of $\tan^{-1}$ ωRC, and at 100 MHz that is 21°. If the amplifier has a 45°

Application Hints — Contd.

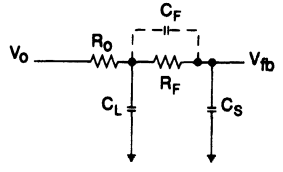
phase margin with no capacitive loading, then with 15 pF it will reduce to 24° and considerable ringing will occur. Some help can be obtained by isolating the output from the capacitance on the inverting input.

Voltage Follower with Feedback Isolation



2041-15

Equivalent Circuit for Signal, Fed Back



2041-16

The signal fed back is:

$$\frac{V_{FB}}{V_O} = \frac{1}{(1+SC_LR_O)(1+SR_FC_S)}$$

The situation now appears to have been made worse with an output pole and a feedback pole, but with the addition of a capacitor C_F, the effects of the stray capacitance at the inverting input can be swamped.

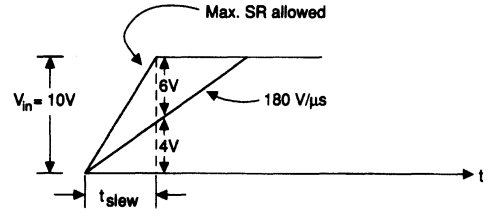
$$\frac{V_{FB}}{V_O} = \frac{1+SC_FR_F}{(1+SC_LR_O)(1+SR_F[C_F+C_S])}$$

The trick here is to pick C_F large enough to overwhelm C_S and cancel the feedback pole. However C_F cannot be made too large or it will look like an AC short and C_S will again appear in parallel with C_L. Some typical values to begin design work are: $R_F = 200$, $C_F = 15$ pF, for C_L = 15 pF, and C_S depends on board layout (try to minimize). It should also be realized that these values of R_F and C_F will begin to roll-off the close loop gain at 40 MHz.

Input Overdrive

It is important not to overdrive the input of the EL2041. Input slew rates in excess of 180 V/μs can cause distortion in the large signal square wave response, and this will show up as an increase in settling time (see typical performance curves). There are several solutions to this: Slew rate limit the input source, put clamp diodes across the amplifier inputs, or take some voltage gain in the amplifier.

Slew rate limit the input: For example with a 10 V_{p-p} step at the input, the input rate should be limited to:



2041-17

$$t_{SLEW} = \frac{V_{IN} - V_{ZENER}}{\min SR},$$

$$\text{Max source SR} = \frac{V_{IN}}{t_{SLEW}}$$

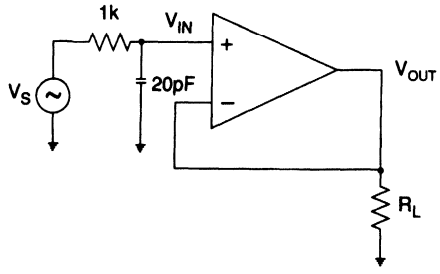
or

$$\frac{10-6}{180\ V/\mu s} = 22\ ns\ ,\quad \text{Max SR} = \frac{10}{22\ ns} = 450\ V/\mu s$$

If the input slew rate is limited by a 1k resistor, how large a capacitor is needed?

$$\frac{10V}{1k} = 10\ mA = C\frac{dv}{dt}\ ,\quad C = \frac{10\ mA}{450\ V/\mu s} = 22\ pF$$

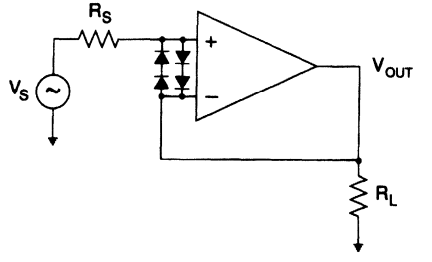
Application Hints — Contd.



2041-18

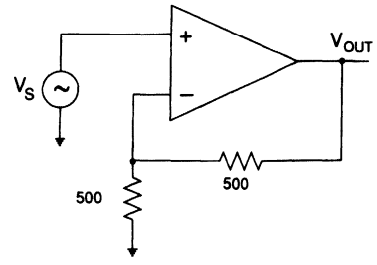
This value of R and C will give a −3 dB bandwidth of 8 MHz through the op amp. This technique should be avoided if the intended use is a small signal sinewave application.

Clamp diodes across the inputs: To obtain full slew rate at elevated temperature requires a V_{BE} of overdrive across the inputs. To insure adequate protection and slew rate requires two diodes in each direction across the inputs. A small series resistance in the input will limit the current through the diodes.



2041-19

Take voltage gain in the op amp: By taking voltage gain, the input stage does not have to handle as large a signal swing for a given output swing. For a voltage gain of 2, remember that the closed loop bandwidth will go to 45 MHz.

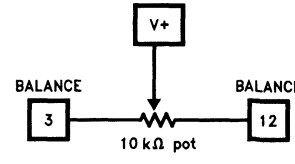


2041-20

Using the BALANCE Pins on the EL2041 Operational Amplifier

The BALANCE pins on the EL2041 can be used to tune out or adjust the input offset voltage of the op amp. To use these pins, ignore the connections shown on the simplified schematic on page 1-171. The adjust current is mirrored up to pnp current sources near V+ and the BALANCE adjustment pot goes between the collectors of two same-sex transistors. Take a 10 kΩ potentiometer (or lower) and connect the ends of the pot to the BALANCE pins and then connect the wiper to +V as shown (see Figure below). Moving the wiper between the two values should zero out the offset voltage.

In hooking up the example test circuit and measuring the voltage between pins 4 and 5 of an EL2041J, with supply voltages of ±15V and a 10 kΩ pot between pins 3 and 12, an example adjustment range of +10.3 mV to −13.4 mV for V_{OS} was measured. The adjust range can be increased by lowering the size of the trim pot and decreased by increasing it. Adjustment range will vary slightly from part to part.

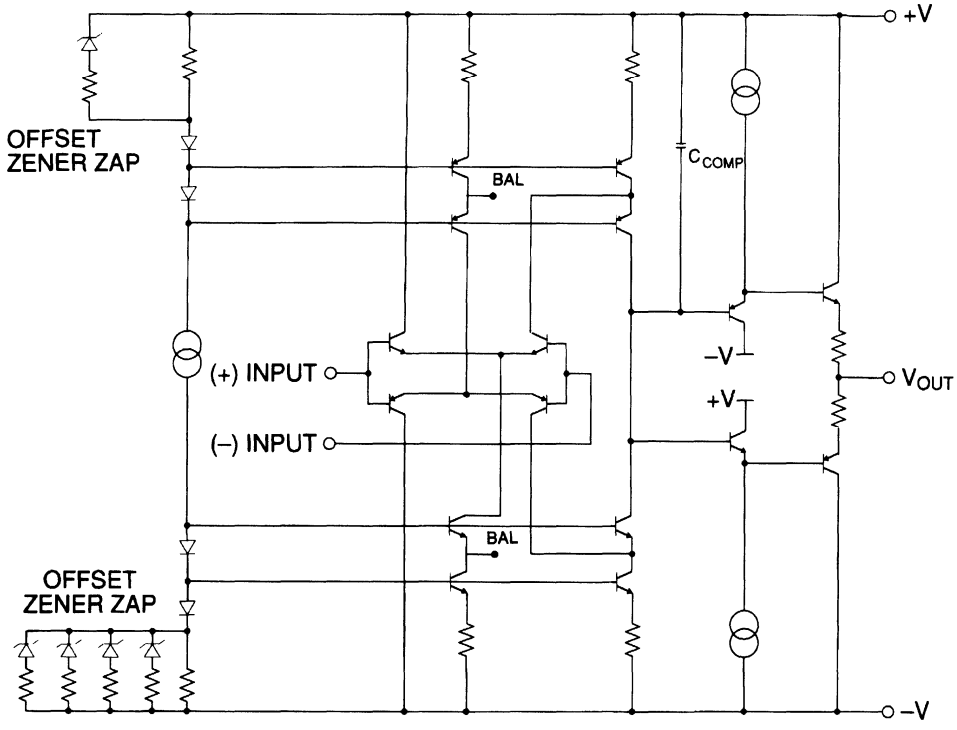


2041-23

EL2041C

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

Simplified Schematic



2041-21

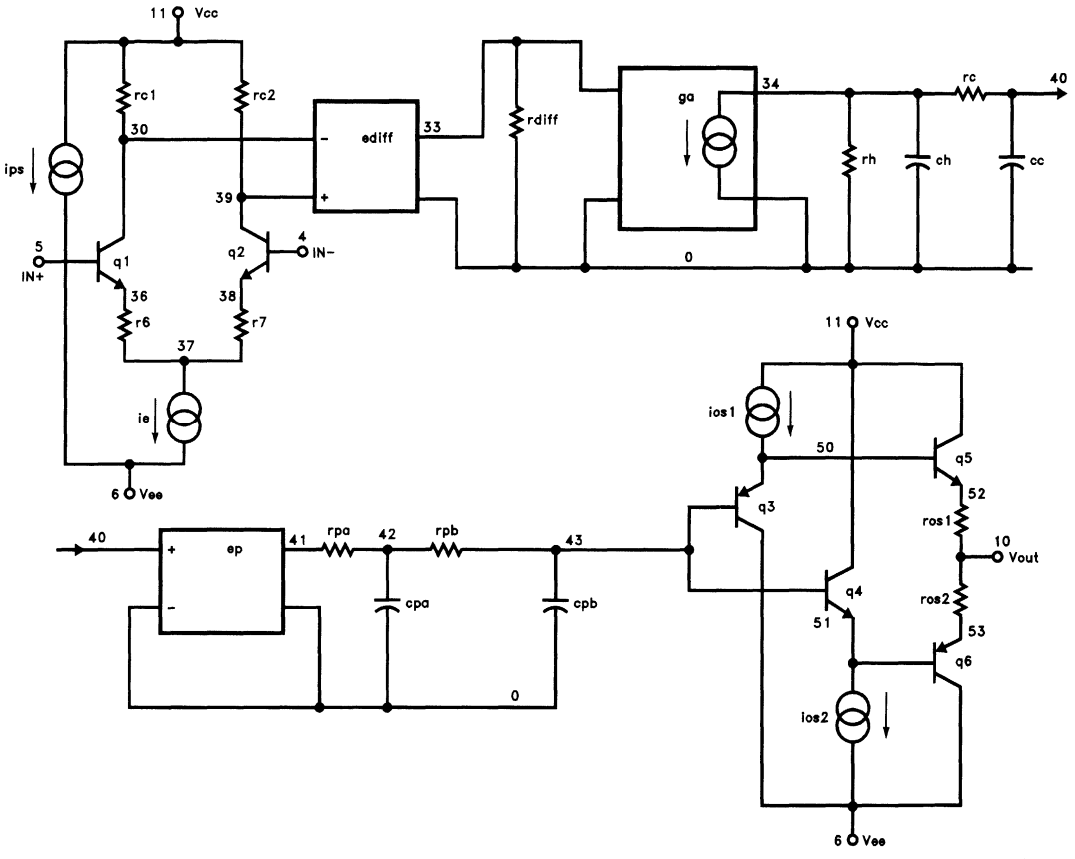
EL2041 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2041       5     4     11    6     10
* Input stage
ie 37 6 3.7mA
r6 36 37 75
r7 38 37 75
rc1 11 30 75
rc2 11 39 75
q1 30 5 36 qn
q2 39 4 38 qna
ediff 33 0 39 30 3
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 5.2m
rh 34 0 1Meg
ch 34 0 16pF
rc 34 40 300
cc 40 0 1.5pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 2pF
rpb 42 43 50
cpb 43 0 3pF
* Output Stage
ios1 11 50 1.25mA
ios2 51 6 1.25mA
q3 6 43 50 qp
q4 11 43 51 qn
q5 11 50 52 qn
q6 6 51 53 qp
ros1 52 10 25
ros2 10 53 25
* Power Supply Current
ips 11 6 6.5mA
* Models
.model qn npn(is=800.0E-18 bf=340 tf=0.2nS)
.model qna npn(is=864E-18 bf=400 tf=0.2nS)
.model qp pnp(is=800E-18 bf=60 tf=0.2nS)
.ends
```

EL2041C

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

EL2041 Macromodel — Contd.



EL2044C

Low-Power 60 MHz Unity-Gain Stable Operational Amplifier

Features

- 60 MHz gain-bandwidth product
- Unity-gain stable
- Low supply current = 5.2 mA at $V_S = \pm 15V$
- Wide supply range = $\pm 2V$ to $\pm 18V$ dual-supply = 2.5V to 36V single-supply
- High slew rate = 325 V/μs
- Fast settling = 80 ns to 0.1% for a 10V step
- Low differential gain = 0.04% at $A_V = +2$, $R_L = 150\Omega$
- Low differential phase = 0.15° at $A_V = +2$, $R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing = $\pm 13.6V$ with $V_S = \pm 15V$, $R_L = 1000\Omega$ = 3.8V/0.3V with $V_S = +5V$, $R_L = 500\Omega$
- Low cost, enhanced replacement for the AD847 and LM6361

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2044CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2044CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL2044C is a high speed, low power, low cost monolithic operational amplifier built on Elantec's proprietary complementary bipolar process. The EL2044C is unity-gain stable and features a 325 V/μs slew rate and 60 MHz gain-bandwidth product while requiring only 5.2 mA of supply current.

The power supply operating range of the EL2044C is from $\pm 18V$ down to as little as $\pm 2V$. For single-supply operation, the EL2044C operates from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2044C makes it an obvious choice for applications on a single $+5V$ supply.

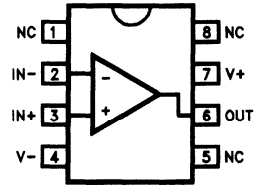
The EL2044C also features an extremely wide output voltage swing of $\pm 13.6V$ with $V_S = \pm 15V$ and $R_L = 1000\Omega$. At $\pm 5V$, output voltage swing is a wide $\pm 3.8V$ with $R_L = 500\Omega$ and $\pm 3.2V$ with $R_L = 150\Omega$. Furthermore, for single-supply operation at $+5V$, output voltage swing is an excellent 0.3V to 3.8V with $R_L = 500\Omega$.

At a gain of $+1$, the EL2044C has a -3 dB bandwidth of 120 MHz with a phase margin of 50°. It can drive unlimited load capacitance, and because of its conventional voltage-feedback topology, the EL2044C allows the use of reactive or non-linear elements in its feedback network. This versatility combined with low cost and 75 mA of output-current drive makes the EL2044C an ideal choice for price-sensitive applications requiring low power and high speed.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



2044-3

EL2044C

Low-Power 60 MHz Unity-Gain Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±18V or 36V	Operating Junction Temperature (T_J)	150°C
Peak Output Current (I_{OP})	Short-Circuit Protected	Storage Temperature (T_{ST})	−65°C to +150°C
Output Short-Circuit Duration (Note 1)	Infinite	Lead Temperature	
Input Voltage (V_{IN})	±V_S	DIP Package (Soldering: < 5 seconds)	300°C
Differential Input Voltage (dV_{IN})	±10V	SO Package Vapor Phase (60 seconds)	215°C
Power Dissipation (P_D)	See Curves	Infrared (15 seconds)	220°C
Operating Temperature Range (T_A)	−40°C to +85°C		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		0.5	7.0	I	mV
			T_{MIN}, T_{MAX}			13.0	IV	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)	All		10.0		V	µV/°C
I_B	Input Bias Current	V_S = ±15V	25°C		2.8	8.2	I	µA
			T_{MIN}, T_{MAX}			11.2	IV	µA
		V_S = ±5V	25°C		2.8		V	µA
I_{OS}	Input Offset Current	V_S = ±15V	25°C		50	300	I	nA
			T_{MIN}, T_{MAX}			500	IV	nA
		V_S = ±5V	25°C		50		V	nA
TCI_{OS}	Average Offset Current Drift	(Note 2)	All		0.3		V	nA/°C
A_{VOL}	Open-Loop Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1000Ω	25°C	1000	1500		I	V/V
			T_{MIN}, T_{MAX}	800			IV	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 500Ω	25°C		1200		V	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 150Ω	25°C		1000		V	V/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	25°C	70	80		I	dB
			T_{MIN}, T_{MAX}	65			IV	dB

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1000\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$, $V_{OUT} = 0V$	25°C	70	90		I	dB
			T_{MIN}, T_{MAX}	70			IV	dB
CMIR	Common-Mode Input Range	$V_S = \pm 15V$	25°C		±14.0		V	V
		$V_S = \pm 5V$	25°C		±4.2		V	V
		$V_S = +5V$	25°C		4.2/0.1		V	V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 1000\Omega$	25°C	±13.4	±13.6		I	V
			T_{MIN}, T_{MAX}	±13.1			IV	V
		$V_S = \pm 15V$, $R_L = 500\Omega$	25°C	±12.0	±13.4		I	V
		$V_S = \pm 5V$, $R_L = 500\Omega$	25°C	±3.4	±3.8		IV	V
		$V_S = \pm 5V$, $R_L = 150\Omega$	25°C		±3.2		V	V
		$V_S = +5V$, $R_L = 500\Omega$	25°C	3.6/0.4	3.8/0.3		I	V
			T_{MIN}, T_{MAX}	3.5/0.5			IV	V
I_{SC}	Output Short Circuit Current		25°C	50	75		I	mA
			T_{MIN}, T_{MAX}	35			IV	mA
I_S	Supply Current	$V_S = \pm 15V$, No Load	25°C		5.2	6.3	I	mA
			T_{MIN}, T_{MAX}			7.6	IV	mA
		$V_S = \pm 5V$, No Load	25°C		5.0		V	mA
R_{IN}	Input Resistance	Differential	25°C		150		V	kΩ
		Common-Mode	25°C		15		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$@ 10 MHz	25°C		1.0		V	pF
R_{OUT}	Output Resistance	$A_V = +1$	25°C		50		V	mΩ
PSOR	Power-Supply Operating Range	Dual-Supply	25°C	±2.0		±18.0	V	V
		Single-Supply	25°C	2.5		36.0	V	V

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +1$, $R_L = 1000\Omega$ unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	$V_S = \pm 15V$, $A_V = +1$	25°C		120		V	MHz
		$V_S = \pm 15V$, $A_V = -1$	25°C		60		V	MHz
		$V_S = \pm 15V$, $A_V = +2$	25°C		60		V	MHz
		$V_S = \pm 15V$, $A_V = +5$	25°C		12		V	MHz
		$V_S = \pm 15V$, $A_V = +10$	25°C		6		V	MHz
		$V_S = \pm 5V$, $A_V = +1$	25°C		80		V	MHz
GBWP	Gain-Bandwidth Product	$V_S = \pm 15V$	25°C		60		V	MHz
		$V_S = \pm 5V$	25°C		45		V	MHz
PM	Phase Margin	$R_L = 1$ kΩ, $C_L = 10$ pF	25°C		50		V	°

Closed-Loop AC Electrical Characteristics

V_S = ±15V, A_V = +1, R_L = 1000Ω unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 3)	V_S = ±15V, R_L = 1000Ω	25°C	250	325		I	V/μs
		V_S = ±5V, R_L = 500Ω	25°C		200		V	V/μs
FPBW	Full-Power Bandwidth (Note 4)	V_S = ±15V	25°C	4.0	5.2		I	MHz
		V_S = ±5V	25°C		12.7		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step	25°C		3.0		V	ns
OS	Overshoot	0.1V Step	25°C		20		V	%
t_{PD}	Propagation Delay		25°C		2.5		V	ns
t_s	Settling to +0.1% (A_V = +1)	V_S = ±15V, 10V Step	25°C		80		V	ns
		V_S = ±5V, 5V Step	25°C		60		V	ns
dG	Differential Gain (Note 5)	NTSC/PAL	25°C		0.04		V	%
dP	Differential Phase (Note 5)	NTSC/PAL	25°C		0.15		V	°
eN	Input Noise Voltage	10 kHz	25°C		15.0		V	nV/√Hz
iN	Input Noise Current	10 kHz	25°C		1.50		V	pA/√Hz
CI STAB	Load Capacitance Stability	A_V = +1	25°C		Infinite		V	pF

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 2: Measured from T_{MIN} to T_{MAX}.

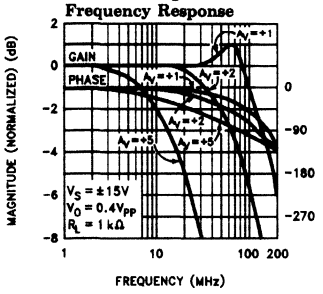
Note 3: Slew rate is measured on rising edge.

Note 4: For V_S = ±15V, V_{OUT} = 20 V_{PP}. For V_S = ±5V, V_{OUT} = 5 V_{PP}. Full-power bandwidth is based on slew rate measurement using: FPBW = SR/(2π * Vpeak).

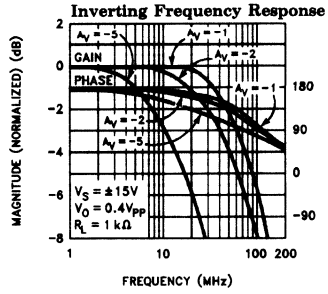
Note 5: Video Performance measured at V_S = ±15V, A_V = +2 with 2 times normal video level across R_L = 150Ω. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L, see curves.

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified)

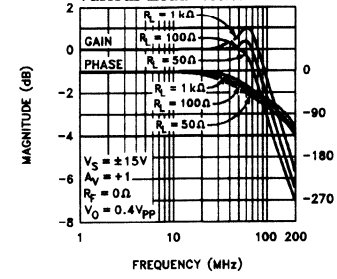
Non-Inverting Frequency Response



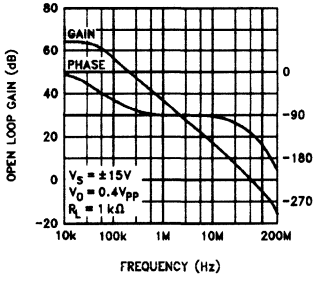
Inverting Frequency Response



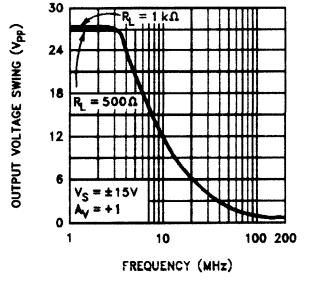
Frequency Response for Various Load Resistances



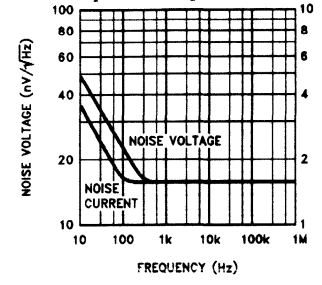
Open-Loop Gain and Phase vs Frequency



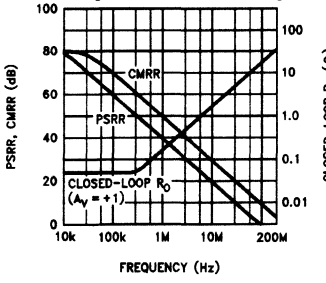
Output Voltage Swing vs Frequency



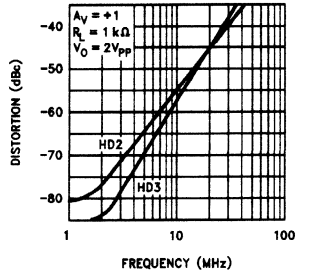
Equivalent Input Noise



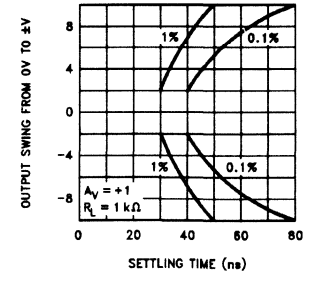
CMRR, PSRR and Closed-Loop Output Resistance vs Frequency



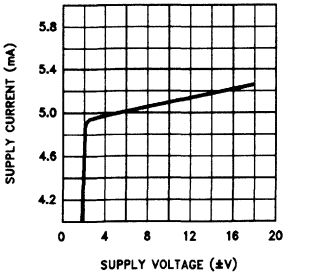
2nd and 3rd Harmonic Distortion vs Frequency



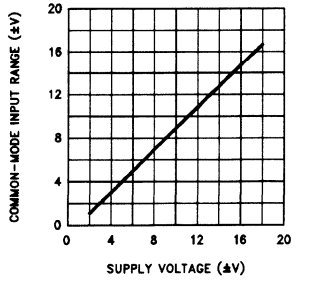
Settling Time vs Output Voltage Change



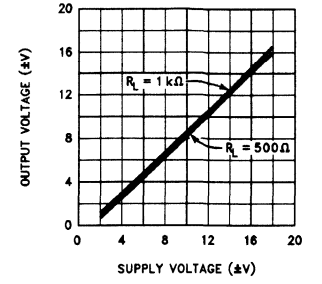
Supply Current vs Supply Voltage



Common-Mode Input Range vs Supply Voltage



Output Voltage Range vs Supply Voltage



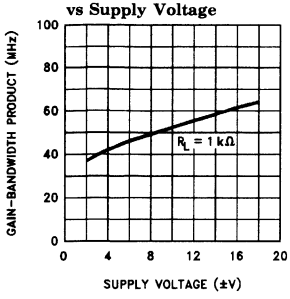
2044-5

EL2044C

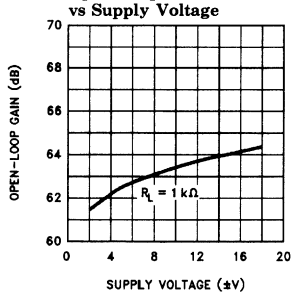
Low-Power 60 MHz Unity-Gain Stable Operational Amplifier

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

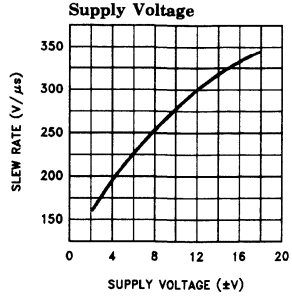
Gain-Bandwidth Product vs Supply Voltage



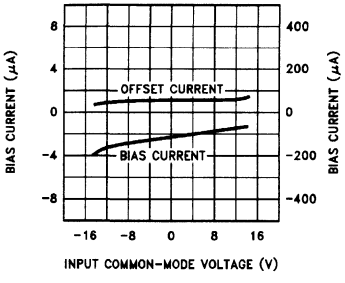
Open-Loop Gain vs Supply Voltage



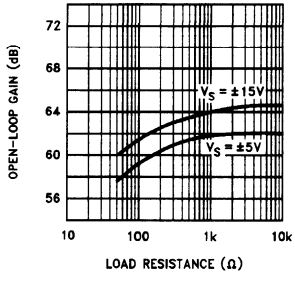
Slew-Rate vs Supply Voltage



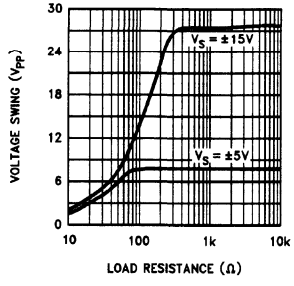
Bias and Offset Current vs Input Common-Mode Voltage



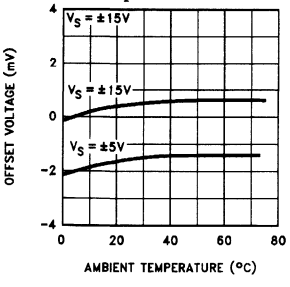
Open-Loop Gain vs Load Resistance



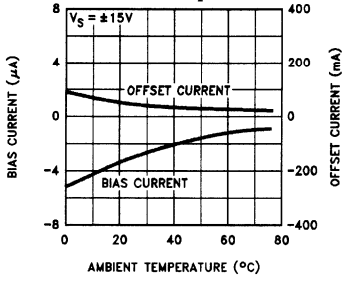
Voltage Swing vs Load Resistance



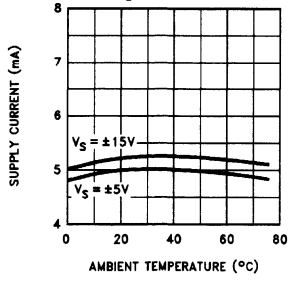
Offset Voltage vs Temperature



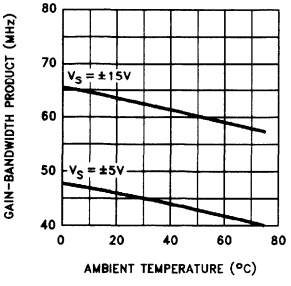
Bias and Offset Current vs Temperature



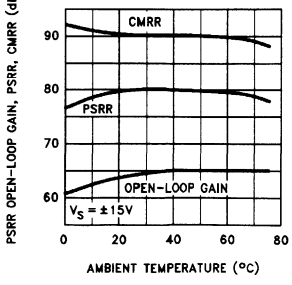
Supply Current vs Temperature



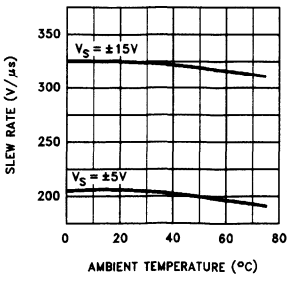
Gain-Bandwidth Product vs Temperature



Open-Loop Gain PSRR and CMRR vs Temperature



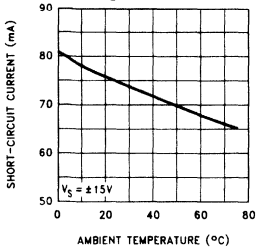
Slew Rate vs Temperature



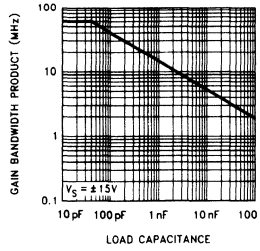
2044-6

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

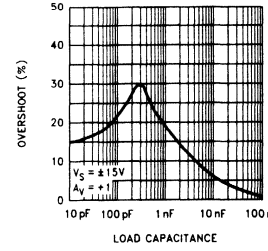
Short-Circuit Current vs Temperature



Gain-Bandwidth Product vs Load Capacitance

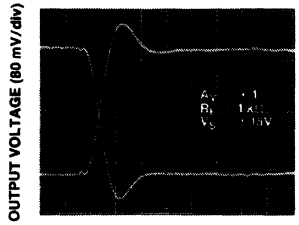


Overshoot vs Load Capacitance



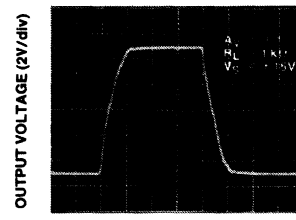
2044-7

Small-Signal Step Response



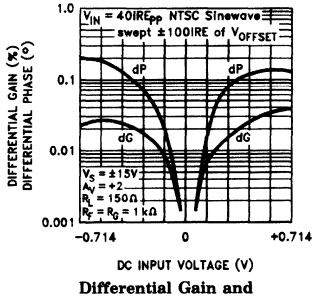
2044-8

Large-Signal Step Response

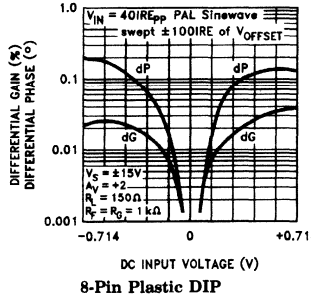


2044-9

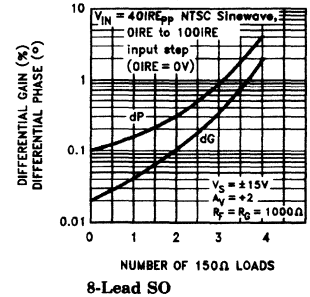
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



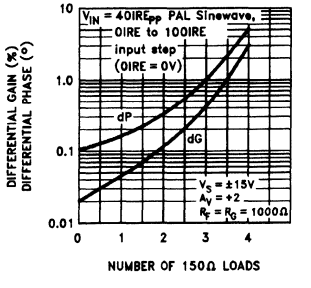
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



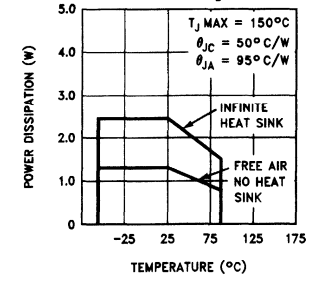
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



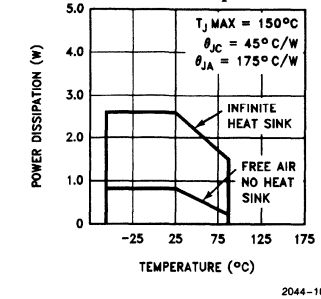
Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature

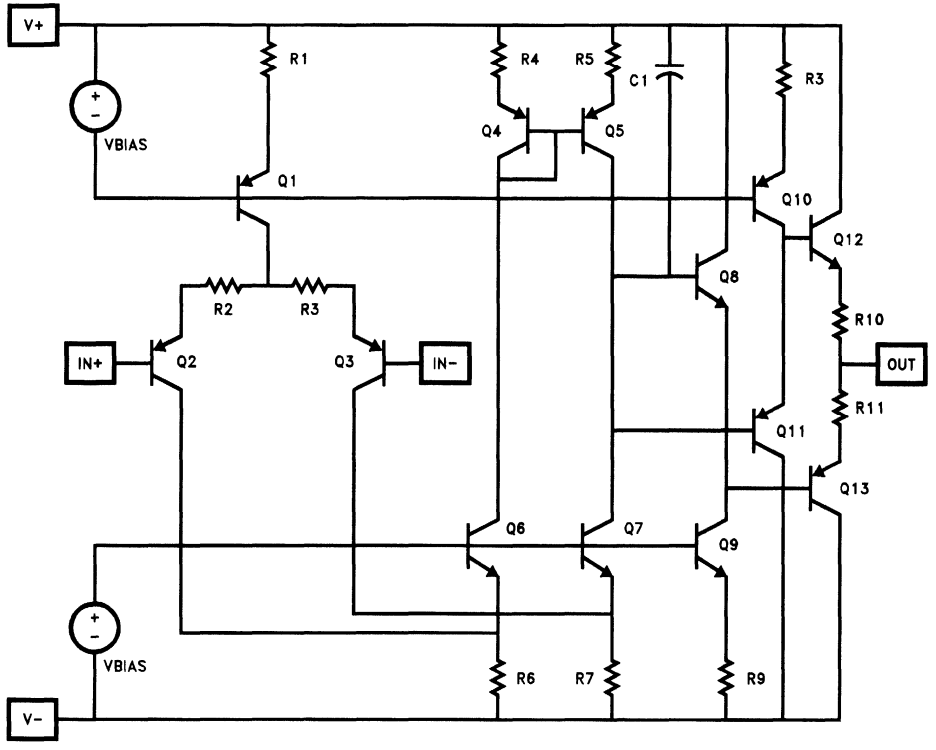


2044-10

EL2044C

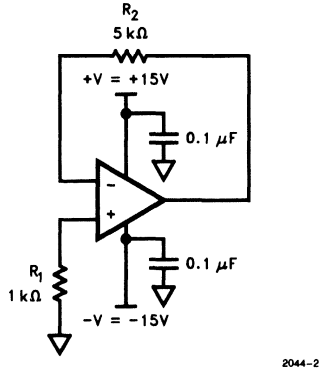
Low-Power 60 MHz Unity-Gain Stable Operational Amplifier

Simplified Schematic



2044-1

Burn-In Circuit



All Packages Use the Same Schematic

Applications Information

Product Description

The EL2044C is a low-power wideband monolithic operational amplifier built on Elantec's proprietary high-speed complementary bipolar process. The EL2044C uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2044C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2044C is an excellent choice for applications such as fast log amplifiers.

Single-Supply Operation

The EL2044C has been designed to have a wide input and output voltage range. This design also makes the EL2044C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (R_L = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2044C still has 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth

The EL2044C has a gain-bandwidth product of 60 MHz while using only 5.2 mA of supply current. For gains greater than 4, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2044C has a −3 dB bandwidth of 120 MHz at a gain of +1, dropping to 60 MHz at a gain of +2. It is important to note that the EL2044C has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2044C in a gain of +1 only exhibits 1.0 dB of peaking with a 1000Ω load.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2044C is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2044C has been designed as an economical solution for applications requiring low video distortion. It has been thoroughly characterized

EL2044C
Low-Power 60 MHz Unity-Gain Stable Operational Amplifier

Applications Information — Contd.

for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2044C exhibits dG and dP of only 0.04% and 0.15° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2044C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The output drive capability of the EL2044C allows it to drive up to 2 back-terminated loads with good video performance. For more demanding applications such as greater output drive or better video distortion, a number of alternatives such as the EL2120, EL400, or EL2073 should be considered.

Output Drive Capability

The EL2044C has been designed to drive low impedance loads. It can easily drive 6 V_{PP} into a 150Ω load. This high output drive capability makes the EL2044C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2044C remains a minimum of 35 mA at low temperatures. The EL2044C is current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2044C has been designed to drive any capacitive load. However, the EL2044C remains stable by automatically reducing its gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2044C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2044C is well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2044C Macromodel

This macromodel has been developed to assist the user in simulating the EL2044C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

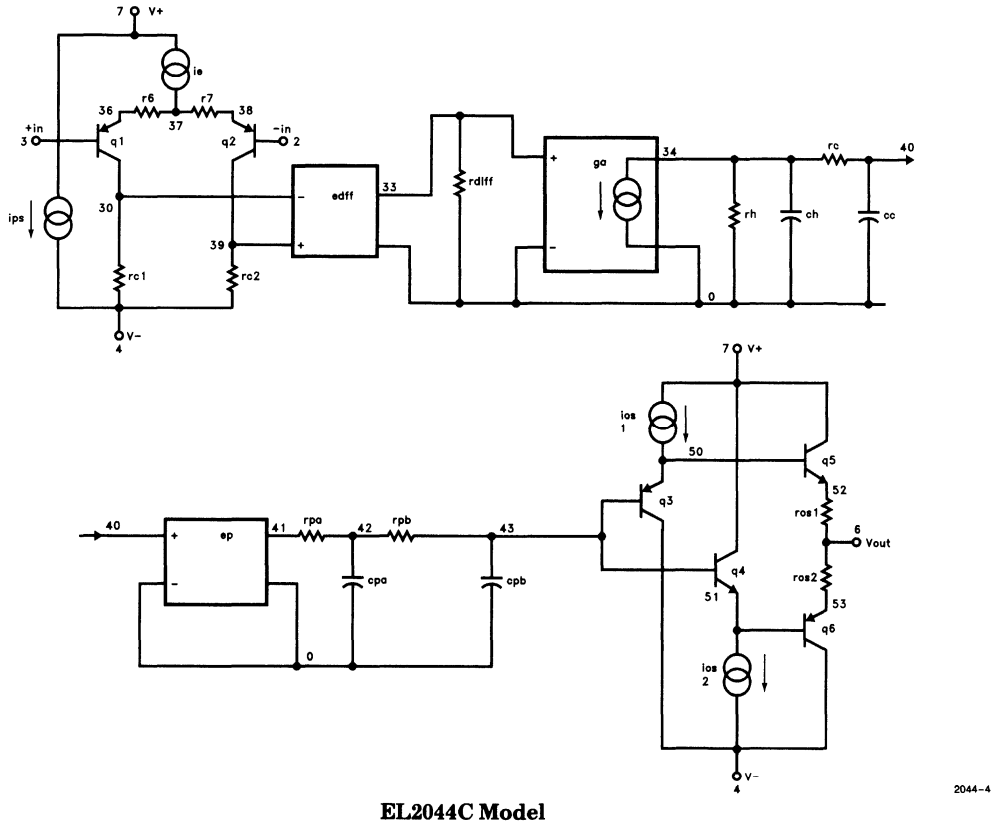
noise	non-linearities
settling-time	temperature effects
CMRR	manufacturing variations
PSRR	

EL2044C Macromodel — Contd.

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2044       3     2     7     4     6
*
* Input stage
*
ie 7 37 1mA
r6 36 37 800
r7 38 37 800
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.3pF
rc 34 40 1K
cc 40 0 1pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 200
cpa 42 0 1pF
rpb 42 43 200
cpb 43 0 1pF
*
* Output Stage
*
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
*
* Power Supply Current
*
ips 7 4 2.7mA
*
* Models
*
.model qn npn(is=800E-18 bf=200 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=100 tf=0.2nS)
.model qp pnp(is=800E-18 bf=125 tf=0.2nS)
.ends
```

EL2044C
Low-Power 60 MHz Unity-Gain Stable Operational Amplifier

EL2044C Macromodel — Contd.



EL2044C Model

EL2045C

Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

Features

- 100 MHz gain-bandwidth product
- Gain-of-2 stable
- Low supply current = 5.2 mA at $V_S = \pm 15V$
- Wide supply range = $\pm 2V$ to $\pm 18V$ dual-supply = 2.5V to 36V single-supply
- High slew rate = 275 V/μs
- Fast settling = 80 ns to 0.1% for a 10V step
- Low differential gain = 0.02% at $A_V = +2$, $R_L = 150\Omega$
- Low differential phase = 0.07° at $A_V = +2$, $R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing = $\pm 13.6V$ with $V_S = \pm 15V$, $R_L = 1000\Omega$ = 3.8V/0.3V with $V_S = +5V$, $R_L = 500\Omega$

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2045CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2045CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

The EL2045C is a high speed, low power, low cost monolithic operational amplifier built on Elantec's proprietary complementary bipolar process. The EL2045C is gain-of-2 stable and features a 275 V/μs slew rate and 100 MHz gain-bandwidth product while requiring only 5.2 mA of supply current.

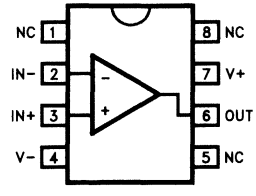
The power supply operating range of the EL2045C is from $\pm 18V$ down to as little as $\pm 2V$. For single-supply operation, the EL2045C operates from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2045C makes it an obvious choice for applications on a single +5V or +3V supply.

The EL2045C also features an extremely wide output voltage swing of $\pm 13.6V$ with $V_S = \pm 15V$ and $R_L = 1000\Omega$. At $\pm 5V$, output voltage swing is a wide $\pm 3.8V$ with $R_L = 500\Omega$ and $\pm 3.2V$ with $R_L = 150\Omega$. Furthermore, for single-supply operation at +5V, output voltage swing is an excellent 0.3V to 3.8V with $R_L = 500\Omega$.

At a gain of +2, the EL2045C has a −3 dB bandwidth of 100 MHz with a phase margin of 50°. It can drive unlimited load capacitance, and because of its conventional voltage-feedback topology, the EL2045C allows the use of reactive or non-linear elements in its feedback network. This versatility combined with low cost and 75 mA of output-current drive makes the EL2045C an ideal choice for price-sensitive applications requiring low power and high speed.

Connection Diagram

DIP and SO Package



2045-1

EL2045C

Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±18V or 36V
Peak Output Current (I_{OP})	Short-Circuit Protected
Output Short-Circuit Duration (Note 1)	Infinite
Input Voltage (V_{IN})	$\pm V_S$
Differential Input Voltage (dV_{IN})	±10V
Power Dissipation (P_D)	See Curves
Operating Temperature Range (T_A)	0°C to +75°C
Operating Junction Temperature (T_J)	150°C
Storage Temperature (T_{ST})	−65°C to +150°C
Lead Temperature	
DIP Package (Soldering: < 5 seconds)	300°C
SO Package Vapor Phase (60 seconds)	215°C
SO Package Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		0.5	7.0	I	mV
			T_{MIN}, T_{MAX}			9.0	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)	All		10.0		V	µV/°C
I_B	Input Bias Current	V_S = ± V	25°C		2.8	8.2	I	µA
			T_{MIN}, T_{MAX}			9.2	III	µA
		V_S = ±5	25°C		2.8		V	µA
I_{OS}	Input Offset Current	V_S = ±15	25°C		50	300	I	nA
			T_{MIN}, T_{MAX}			400	III	nA
		V_S = ±5V	25°C		50		V	nA
TCI_{OS}	Average Offset Current Drift	(Note 2)	All		0.3		V	nA/°C
A_{VOL}	Open-Loop Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1000Ω	25°C	1500	3000		I	V/V
			T_{MIN}, T_{MAX}	1500			III	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 500Ω	25°C		2500		V	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 150Ω	25°C		1750		V	V/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	25°C	70	85		I	dB
			T_{MIN}, T_{MAX}	65			III	dB

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1000\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$, $V_{OUT} = 0V$	25°C	70	95		I	dB
			T_{MIN}, T_{MAX}	70			III	dB
CMIR	Common-Mode Input Range	$V_S = \pm 15V$	25°C		±14.0		V	V
		$V_S = \pm 5V$	25°C		±4.2		V	V
		$V_S = +5V$	25°C		4.2/0.1		V	V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 1000\Omega$	25°C	±13.4	±13.6		I	V
			T_{MIN}, T_{MAX}	±13.1			III	V
		$V_S = \pm 15V$, $R_L = 500\Omega$	25°C	±12.0	±13.4		I	V
		$V_S = \pm 5V$, $R_L = 500\Omega$	25°C	±3.4	±3.8		IV	V
		$V_S = \pm 5V$, $R_L = 150\Omega$	25°C		±3.2		V	V
		$V_S = +5V$, $R_L = 500\Omega$	25°C	3.6/0.4	3.8/0.3		I	V
			T_{MIN}, T_{MAX}	3.5/0.5			III	V
I_{SC}	Output Short Circuit Current		25°C	50	75		I	mA
			T_{MIN}, T_{MAX}	35			III	mA
I_S	Supply Current	$V_S = \pm 15V$, No Load	25°C		5.2	6.3	I	mA
			T_{MIN}, T_{MAX}			7.6	III	mA
		$V_S = \pm 5V$, No Load	25°C		5.0		V	mA
R_{IN}	Input Resistance	Differential	25°C		150		V	kΩ
		Common-Mode	25°C		15		V	MΩ
C_{IN}	Input Capacitance	$A_V = +2$@ 10 MHz	25°C		1.0		V	pF
R_{OUT}	Output Resistance	$A_V = +2$	25°C		50		V	mΩ
PSOR	Power-Supply Operating Range	Dual-Supply	25°C	±2.0		±18.0	V	V
		Single-Supply	25°C	2.5		36.0	V	V

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +2$, $R_f = R_g = 1\ k\Omega$, $C_f = 3\ pF$, $R_L = 1000\Omega$ unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth ($V_{OUT} = 0.4\ V_{PP}$)	$V_S = \pm 15V$, $A_V = +2$	25°C		100		V	MHz
		$V_S = \pm 15V$, $A_V = -1$	25°C		75		V	MHz
		$V_S = \pm 15V$, $A_V = +5$	25°C		20		V	MHz
		$V_S = \pm 15V$, $A_V = +10$	25°C		10		V	MHz
		$V_S = \pm 15V$, $A_V = +20$	25°C		5		V	MHz
		$V_S = \pm 5V$, $A_V = +2$	25°C		75		V	MHz
GBWP	Gain-Bandwidth Product	$V_S = \pm 15V$	25°C		100		V	MHz
		$V_S = \pm 5V$	25°C		75		V	MHz
PM	Phase Margin	$R_L = 1\ k\Omega$, $C_L = 10\ pF$	25°C		50		V	°

EL2045C
Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

Closed-Loop AC Electrical Characteristics

V_S = ±15V, A_V = +2, R_f = R_g = 1 kΩ, C_f = 3 pF, R_L = 1000Ω, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 3)	V_S = ±15V, R_L = 1000Ω	25°C	200	275		I	V/μs
		V_S = ±5V, R_L = 500Ω	25°C		200		V	V/μs
FPBW	Full-Power Bandwidth (Note 4)	V_S = ±15V	25°C	3.2	4.4		I	MHz
		V_S = ±5V	25°C		12.7		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Output Step	25°C		3.0		V	ns
OS	Overshoot	0.1V Output Step	25°C		20		V	%
t_{PD}	Propagation Delay		25°C		2.5		V	ns
t_s	Settling to +0.1% (A_V = +2)	V_S = ±15V, 10V Step	25°C		80		V	ns
		V_S = ±5V, 5V Step	25°C		60		V	ns
dG	Differential Gain (Note 5)	NTSC/PAL	25°C		0.02		V	%
dP	Differential Phase (Note 5)	NTSC/PAL	25°C		0.07		V	°
eN	Input Noise Voltage	10 kHz	25°C		15.0		V	nV/√Hz
iN	Input Noise Current	10 kHz	25°C		1.50		V	pA/√Hz
CI STAB	Load Capacitance Stability	A_V = +2	25°C		Infinite		V	pF

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

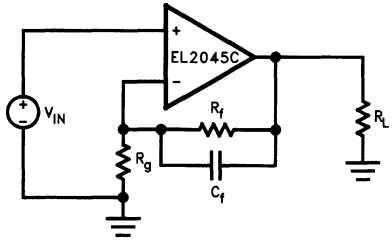
Note 2: Measured from T_{MIN} to T_{MAX}.

Note 3: Slew rate is measured on rising edge.

Note 4: For V_S = ±15V, V_{OUT} = 20 V_{PP}. For V_S = ±5V, V_{OUT} = 5 V_{PP}. Full-power bandwidth is based on slew rate measurement using: FPBW = SR/(2π * Vpeak).

Note 5: Video Performance measured at V_S = ±15V, A_V = +2 with 2 times normal video level across R_L = 150Ω. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L, see curves.

EL2045C Test Circuit



2045-2

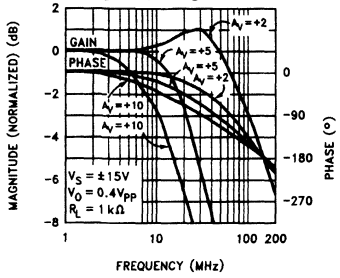
EL2045C

Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

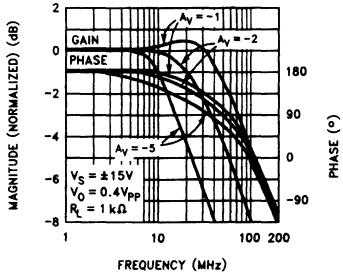
Typical Performance Curves

(T_A = 25°C, R_f = 1 kΩ, C_f = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified)

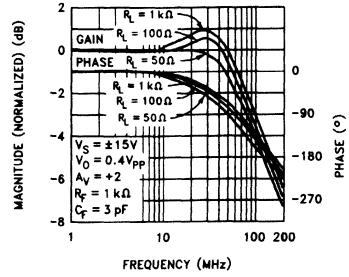
Non-Inverting Frequency Response



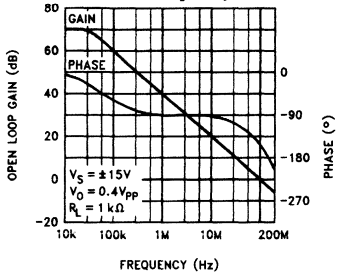
Inverting Frequency Response



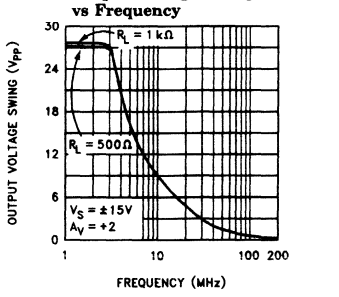
Frequency Response for Various Load Resistances



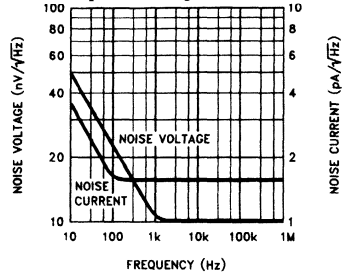
Open-Loop Gain and Phase vs Frequency



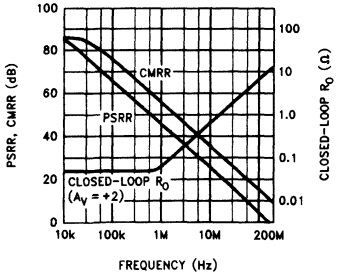
Output Voltage Swing vs Frequency



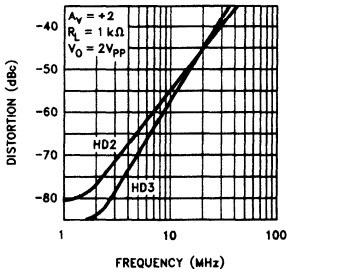
Equivalent Input Noise



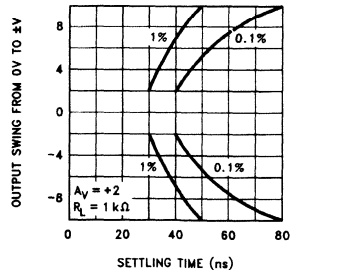
CMRR, PSRR and Closed-Loop Output Resistance vs Frequency



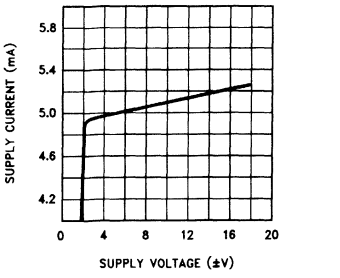
2nd and 3rd Harmonic Distortion vs Frequency



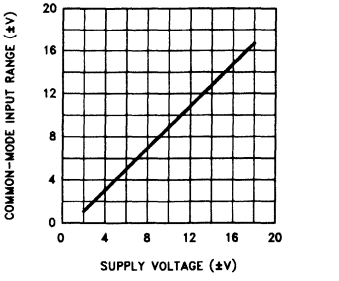
Settling Time vs Output Voltage Change



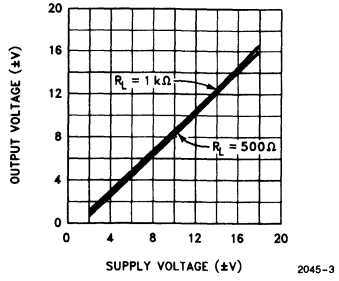
Supply Current vs Supply Voltage



Common-Mode Input Range vs Supply Voltage



Output Voltage Range vs Supply Voltage



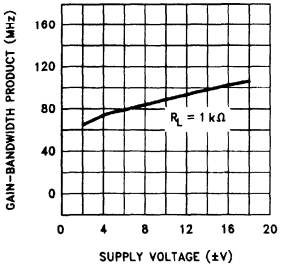
2045-3

EL2045C
Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

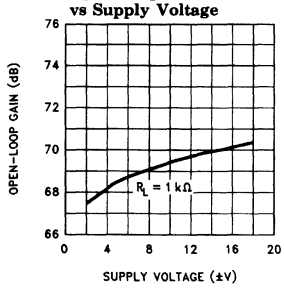
Typical Performance Curves

(T_A = 25°C, R_f = 1 kΩ, C_f = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified) — Contd.

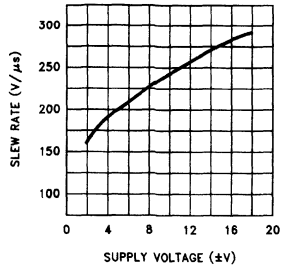
Gain-Bandwidth Product vs Supply Voltage



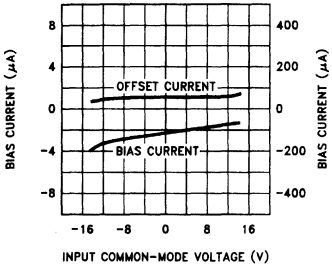
Open-Loop Gain vs Supply Voltage



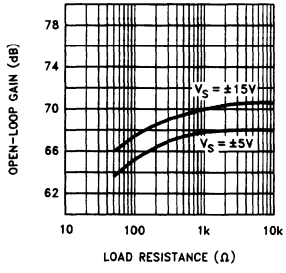
Slew-Rate vs Supply Voltage



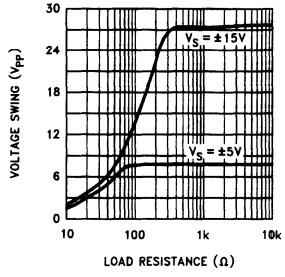
Bias and Offset Current vs Input Common-Mode Voltage



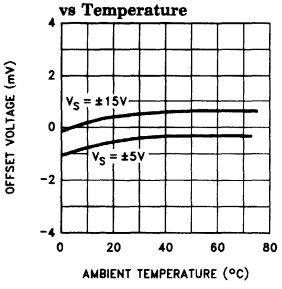
Open-Loop Gain vs Load Resistance



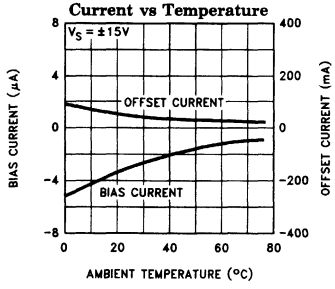
Voltage Swing vs Load Resistance



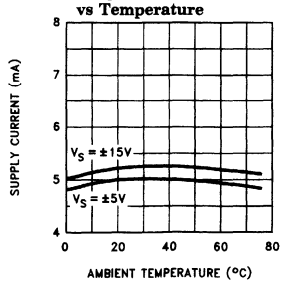
Offset Voltage vs Temperature



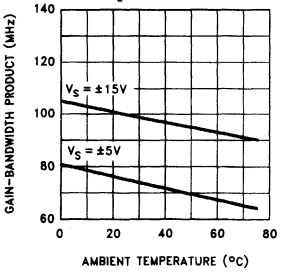
Bias and Offset Current vs Temperature



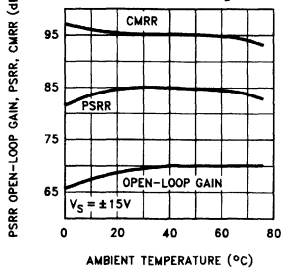
Supply Current vs Temperature



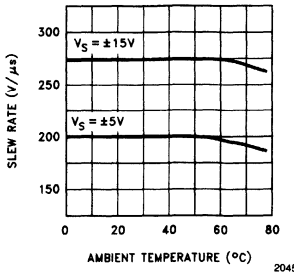
Gain-Bandwidth Product vs Temperature



Open-Loop Gain PSRR and CMRR vs Temperature



Slew Rate vs Temperature

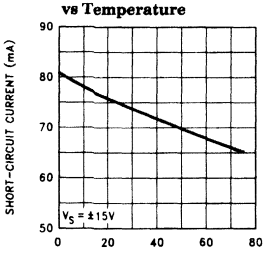


2045-4

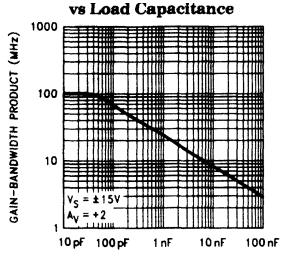
Typical Performance Curves

(T_A = 25°C, R_f = 1 kΩ, C_f = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified) — Contd.

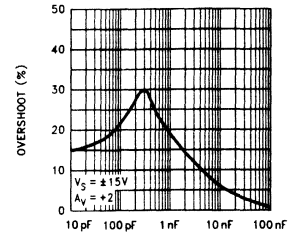
Short-Circuit Current vs Temperature



Gain-Bandwidth Product vs Load Capacitance

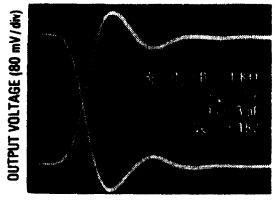


Overshoot vs Load Capacitance



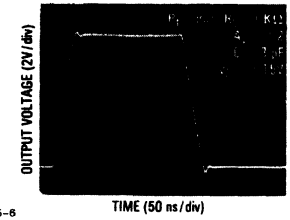
2045-5

Small-Signal Step Response



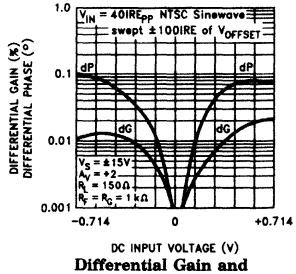
2045-6

Large-Signal Step Response

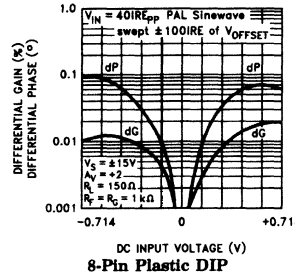


2045-7

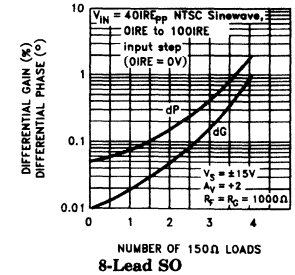
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



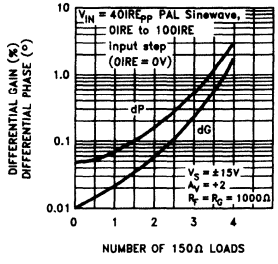
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



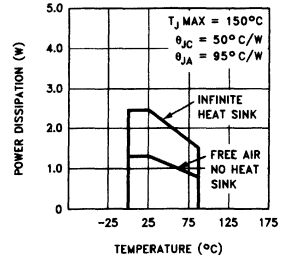
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



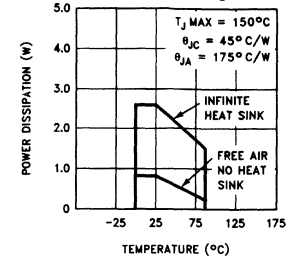
Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature

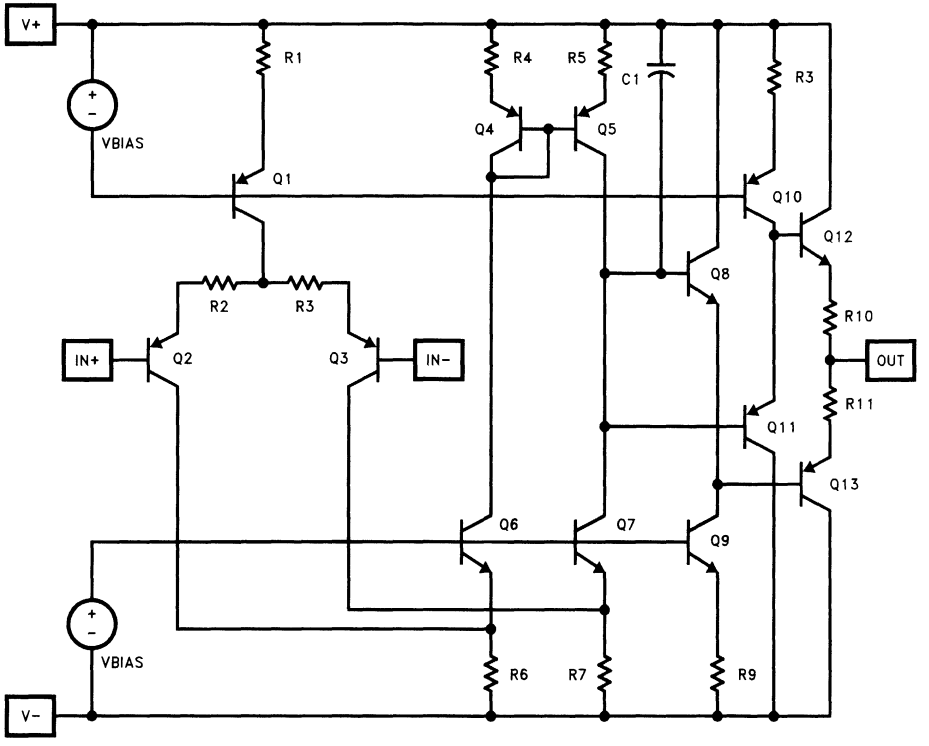


2045-8

EL2045C

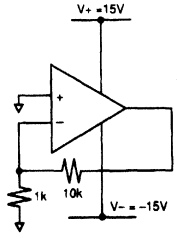
Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

Simplified Schematic



2045-9

Burn-In Circuit



All Packages Use the Same Schematic

Applications Information

Product Description

The EL2045C is a low-power wideband, gain-of-2 stable monolithic operational amplifier built on Elantec's proprietary high-speed complementary bipolar process. The EL2045C uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2045C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2045C is an excellent choice for applications such as fast log amplifiers.

Single-Supply Operation

The EL2045C has been designed to have a wide input and output voltage range. This design also makes the EL2045C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (R_L = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2045C still has 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth

The EL2045C has a gain-bandwidth product of 100 MHz while using only 5.2 mA of supply current. For gains greater than 4, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2045C has a −3 dB bandwidth of 100 MHz at a gain of +2, dropping to 20 MHz at a gain of +5. It is important to note that the EL2045C has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2045C in a gain of +2 only exhibits 1.0 dB of peaking with a 1000Ω load.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2045C is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2045C has been designed as an economical solution for applications requiring low video distortion. It has been thoroughly characterized

EL2045C
Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

Applications Information — Contd.

for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2045C exhibits dG and dP of only 0.02% and 0.07° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2045C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The output drive capability of the EL2045C allows it to drive up to 2 back-terminated loads with good video performance. For more demanding applications such as greater output drive or better video distortion, a number of alternatives such as the EL2120, EL400, or EL2074 should be considered.

Output Drive Capability

The EL2045C has been designed to drive low impedance loads. It can easily drive 6 V_{PP} into a 150Ω load. This high output drive capability makes the EL2045C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2045C remains a minimum of 35 mA at low temperatures. The EL2045C is current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2045C has been designed to drive any capacitive load. However, the EL2045C remains stable by automatically reducing its gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2045C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2045C is well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2045C Macromodel

This macromodel has been developed to assist the user in simulating the EL2045C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

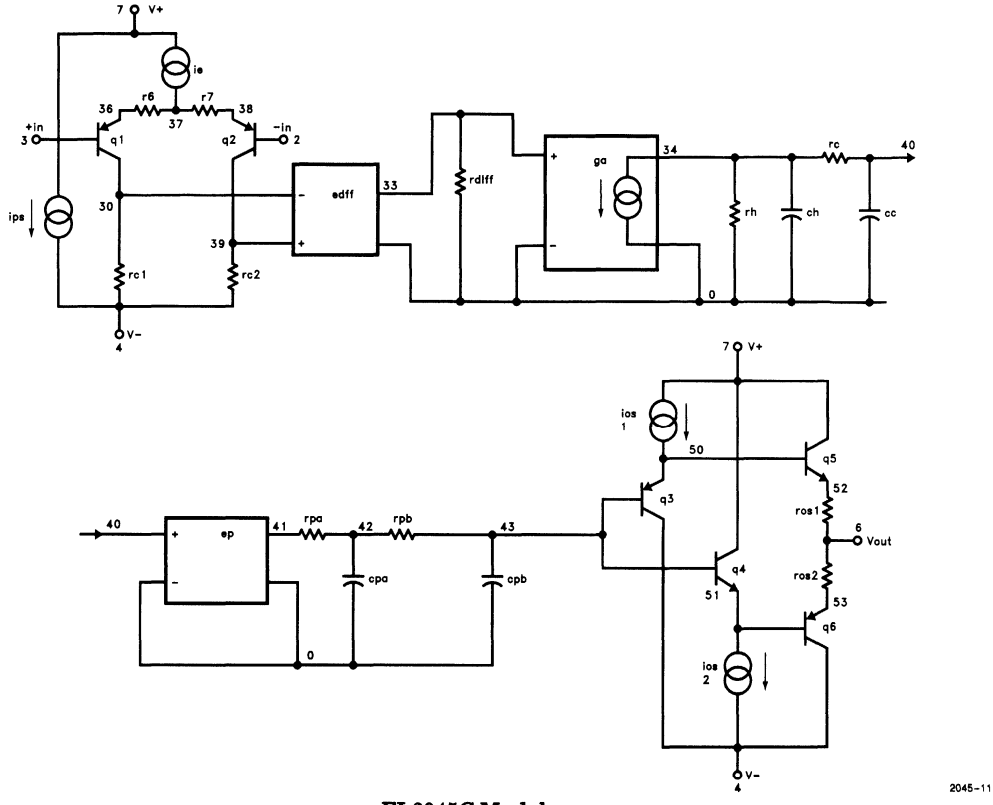
noise	non-linearities
settling-time	temperature effects
CMRR	manufacturing variations
PSRR	

EL2045C Macromodel — Contd.

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2045       3     2     7     4     6
*
* Input stage
*
ie 7 37 0.9mA
r6 36 37 400
r7 38 37 400
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.5pF
rc 34 40 1K
cc 40 0 1pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 200
cpa 42 0 2pF
rpb 42 43 200
cpb 43 0 2pF
*
* Output Stage
*
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
*
* Power Supply Current
*
ips 7 4 2.7mA
*
* Models
*
.model qn npn(is=800E-18 bf=200 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=100 tf=0.2nS)
.model qp pnp(is=800E-18 bf=125 tf=0.2nS)
.ends
```

EL2045C
Low-Power 100 MHz Gain-of-2 Stable Operational Amplifier

EL2045C Macromodel — Contd.



EL2045C Model

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2070C
200 MHz Current Feedback Amplifier

Features

- 200 MHz −3 dB bandwidth, $A_V = 2$
- Disable/enable
- 12 ns settling to 0.05%
- $V_S = \pm 5V$ @ 15 mA
- Low distortion: HD2, HD3 @ −60 dBc at 20 MHz
- Differential gain 0.02% at NTSC, PAL
- Differential phase 0.01° at NTSC, PAL
- Overload/short-circuit protected
- ±1 to ±8 closed-loop gain range
- Low cost

Applications

- Video gain block
- Video distribution
- HDTV amplifier
- Analog multiplexing (using disable)
- Power-down mode (using disable)
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2070CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2070CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL2070 is a wide bandwidth, fast settling monolithic amplifier incorporating a disable/enable feature. Built using an advanced complementary bipolar process, this amplifier uses current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±1 to ±8, the EL2070 has a 200 MHz −3 dB bandwidth ($A_V = +2$), and 12 ns settling to 0.05% while consuming only 15 mA of supply current. Furthermore, the fast disable/enable times of 200 ns/100 ns allow rapid analog multiplexing.

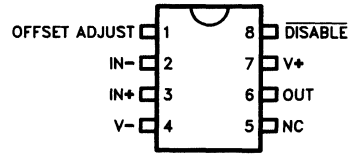
The EL2070 is an obvious high-performance solution for video distribution and line-driving applications, especially when its disable feature can be used for fast analog multiplexing. Furthermore, the low 15 mA supply current, and the very low 5 mA of supply current when disabled suggest use in systems where power is critical. With differential gain/phase of 0.02%/0.01°, guaranteed video specifications, and a minimum 50 mA output drive, performance in these areas is assured.

The EL2070's settling to 0.05% in 12 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 200 MHz bandwidth and extremely linear phase allow unmatched signal fidelity. D/A systems can also benefit from the EL2070, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



2070-1

Top View

EL2070C
200 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V	Applied Output Voltage (Disabled)	±V_S
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.	Power Dissipation	See Curves
Common-Mode Input Voltage	±V_S	Operating Temperature EL2070C	−40C to +85C
Differential Input Voltage	5V	Lead Temperature (Soldering, 5 Seconds)	300°C
Disable Input Voltage	+V_S, −1V	Junction Temperature	175°C
Thermal Resistance θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8		Storage Temperature	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±5V, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		2	5.0	I	mV
			T_{MIN}			8.2	III	mV
			T_{MAX}			9.0	III	mV
$d(V_{OS})/dT$	Average Offset Voltage Drift	(Note 1)	All		10.0	40.0	IV	µV/°C
$+I_{IN}$	+Input Current		25°C, T_{MAX}		10	20.0	II	µA
			T_{MIN}			36.0	III	µA
$d(+I_{IN})/dT$	Average +Input Current Drift	(Note 1)	All		50.0	200.0	IV	nA/°C
$-I_{IN}$	−Input Current		25.0°C		10	20	I	µA
			T_{MIN}, T_{MAX}			36.0	III	µA
$d(-I_{IN})/dT$	Average −Input Current Drift	(Note 1)	All		50.0	200.0	IV	nA/°C

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
PSRR	Power Supply Rejection Ratio		All	45.0	50.0		II	dB
CMRR	Common-Mode Rejection Ratio		All	40.0	50.0		II	dB
I_S	Supply Current—Quiescent	No Load	All		16.0	20.0	II	mA
IS_{OFF}	Supply Current—Disabled	(Note 2)	All		4.0	7.0	II	mA
$+R_{IN}$	+Input Resistance		25°C, T_{MAX}	100.0	200.0		II	kΩ
			T_{MIN}	50.0			III	kΩ
C_{IN}	Input Capacitance		All		0.5	2.0	IV	pF
R_{OUT}	Output Impedance (DC)		All		0.1	0.2	IV	Ω
$R_{OUT}D$	Output Resistance (DC)	Disabled	All	100.0	200.0		IV	kΩ
$C_{OUT}D$	Output Capacitance (DC)	Disabled	All		0.5	2.0	IV	pF
CMIR	Common-Mode Input Range	(Note 3)	25°C, T_{MAX}	2.0	2.1		IV	V
			T_{MIN}	1.2			IV	V
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		II	mA
			T_{MIN}	35.0			III	mA
V_{OUT}	Output Voltage Swing	No Load	All	3.3	3.5		II	V
$V_{OUT}L$	Output Voltage Swing	100Ω	25°C	3.0	3.4		I	V
−ICMR	Input Current Common Mode Rejection		25°C		8.0	33.0	I	μA/V
+IPSR	+Input Current Power Supply Rejection		25°C		1.0	3.6	I	μA/V
−IPSR	−Input Current Power Supply Rejection		25°C		20	24	I	μA/V
R_{OL}	Transimpedance		25°C	30.0	125.0		II	V/mA
			T_{MIN}		80.0		V	V/mA
			T_{MAX}		140.0		V	V/mA
I_{LOGIC}	Pin 8 Current @ 0V		All		0.8	1.2	II	mA
V_{DIS}	Maximum Pin 8 V to Disable		All			0.5	II	V
V_{EN}	Minimum Pin 8 V to Enable		All	3.5			II	V
I_{DIS}	Minimum Pin 8 I to Disable		All	350.0			II	μA
I_{EN}	Maximum Pin 8 I to Enable		All			60.0	II	μA

EL2070C
200 MHz Current Feedback Amplifier

Closed-Loop AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = 250\Omega$, $A_V = +2$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth ($V_{OUT} < 0.5\ V_{PP}$)		25°C	150.0	200.0		III	MHz
			T_{MIN}	150.0			IV	MHz
			T_{MAX}	120.0			IV	MHz
LSBW	−3 dB Bandwidth ($V_{OUT} < 5.0\ V_{PP}$)	$A_V = +5$	All	35.0	50.0		IV	MHz
GAIN FLATNESS								
GFPL	Peaking $V_{OUT} < 0.5\ V_{PP}$	<40 MHz	25°C		0.0	0.3	III	dB
			T_{MIN}, T_{MAX}			0.4	IV	dB
GFPH	Peaking $V_{OUT} < 0.5\ V_{PP}$	>40 MHz	25°C		0.0	0.5	III	dB
			T_{MIN}, T_{MAX}			0.7	IV	dB
GFR	Rolloff $V_{OUT} < 0.5\ V_{PP}$	<75 MHz	25°C		0.6	1.0	III	dB
			T_{MIN}			1.0	IV	dB
			T_{MAX}			1.3	IV	dB
LPD	Linear Phase Deviation $V_{OUT} < 0.5\ V_{PP}$	<75 MHz	25°C, T_{MIN}		0.2	1.0	IV	°
			T_{MAX}			1.2	IV	°
TIME-DOMAIN RESPONSE								
t_{r1}, t_{f1}	Rise Time, Fall Time	0.5V Step	All		1.6	2.4	IV	ns
t_{r2}, t_{f2}	Rise Time, Fall Time	5.0V Step	All		6.5	10.0	IV	ns
t_{s1}	Settling Time to 0.1%	2.0V Step	All		10.0	13.0	IV	ns
t_{s2}	Settling Time to 0.05%	2.0V Step	All		12.0	15.0	IV	ns
OS	Overshoot	0.5V Step	25°C, T_{MAX}		0.0	10.0	IV	%
			T_{MIN}			15.0	IV	%
SR	Slew Rate	$A_V = +2$	All	430.0	700.0		IV	V/µs
		$A_V = -2$	All		1600.0		V	V/µs
DISTORTION								
HD2	2nd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−60.0	−45.0	III	dBc
			T_{MIN}			−40.0	IV	dBc
			T_{MAX}			−45.0	IV	dBc
HD3	3rd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−60.0	−50.0	III	dBc
			T_{MIN}, T_{MAX}			−50.0	IV	dBc

Closed-Loop AC Electrical Characteristics — Contd.

$V_S = \pm 5V$, $R_F = 250\Omega$, $A_V = +2$, $R_L = 100\Omega$ unless otherwise specified

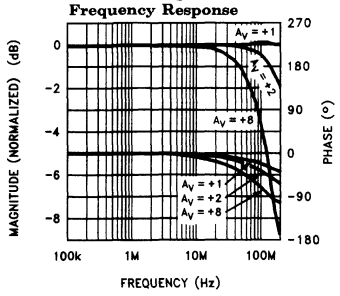
Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz	(Note 4)	25°C		−157.0	−154.0	IV	dBm (1 Hz)
			T_{MIN}			−154.0	IV	dBm (1Hz)
			T_{MAX}			−153.0IV	IV	dBm (1Hz)
INV	Integrated Noise 100 kHz to 200 MHz	(Note 4)	25°C		40.0	57.0	IV	μV
			T_{MIN}			57.0	IV	μV
			T_{MAX}			63.0	IV	μV
DISABLE/ENABLE PERFORMANCE								
T_{OFF}	Disable Time to >50 dB	10 MHz	All		1000.0	IV	V	ns
T_{ON}	Enable Time		All		200.0		V	ns
OFFIso	Off Isolation	10 MHz	All	55.0	59.0		IV	dB
VIDEO PERFORMANCE								
d_G	Differential Gain (Note 5)	NTSC/PAL	25°C		0.02	0.08	III	% pp
d_P	Differential Phase (Note 5)	NTSC/PAL	25°C		0.01	0.08	III	° pp
d_G	Differential Gain (Note 5)	30 MHz	25°C		0.05	0.18	IV	% pp
d_P	Differential Phase (Note 5)	30 MHz	25°C		0.05	0.18	IV	° pp
VBW	−0.1 dB Bandwidth (Note 5)		25°C	30.0	60.0		III	MHz

Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: Supply current when disabled is measured at the negative supply.
Note 3: Common-mode input range for rated performance.
Note 4: Noise Tests are performed from 5 MHz to 200 MHz.
Note 5: Differential gain/phase tests are with $R_L = 100\Omega$. For other values of R_L, see curves.

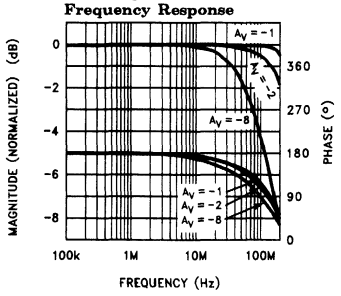
EL2070C
200 MHz Current Feedback Amplifier

Typical Performance Curves

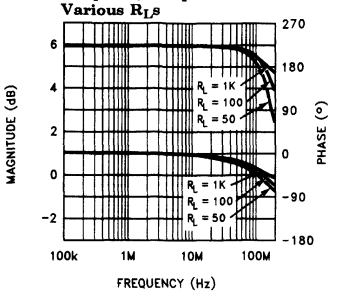
Non-Inverting Frequency Response



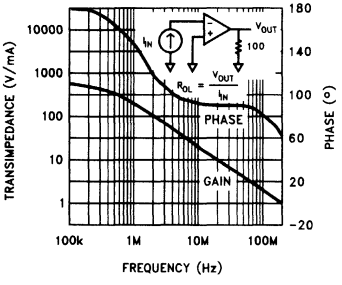
Inverting Frequency Response



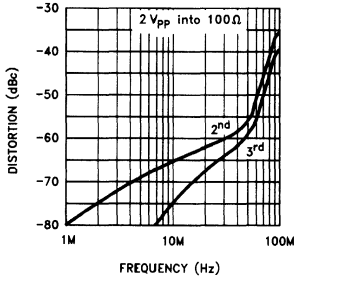
Frequency Response for Various R_Ls



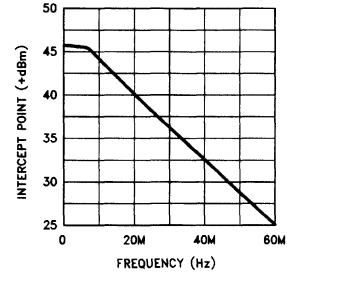
Open-Loop Transimpedance Gain and Phase



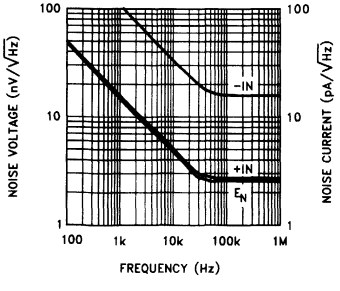
2nd and 3rd Harmonic Distortion



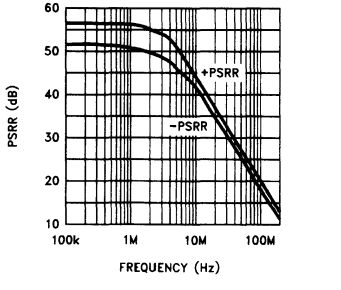
2-Tone 3rd Order Intermodulation Intercept



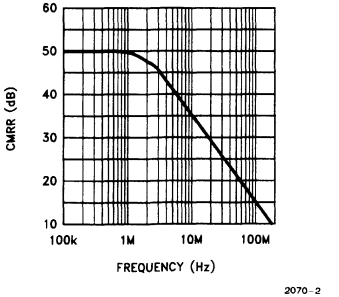
Equivalent Input Noise



Power-Supply Rejection Ratio



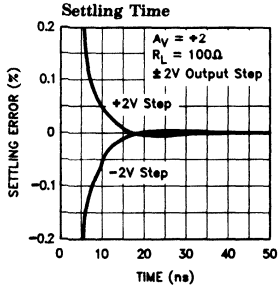
Common-Mode Rejection Ratio



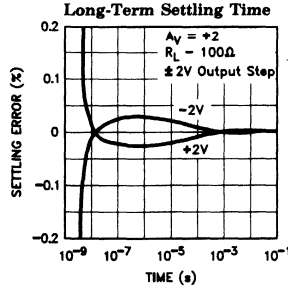
2070-2

Typical Performance Curves — Contd.

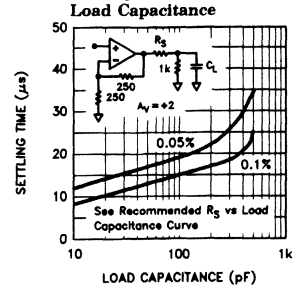
Settling Time



Long-Term Settling Time

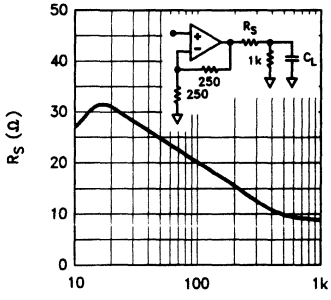


Settling Time vs Load Capacitance



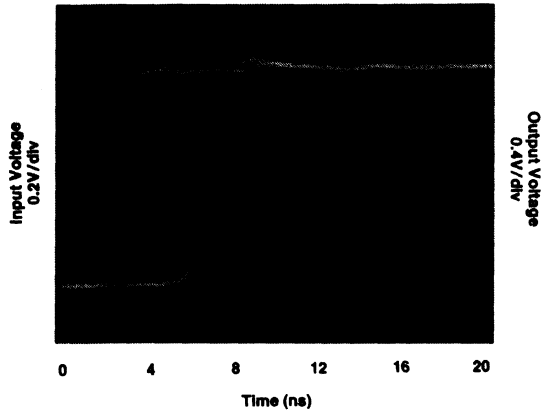
2070-3

Recommended R_S vs Load Capacitance



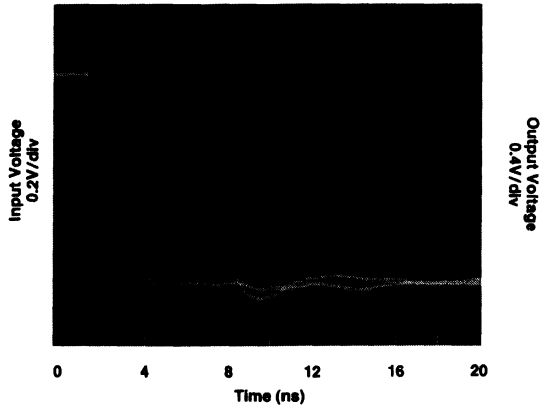
2070-4

Pulse Response A_V = +2



2070-5

Pulse Response A_V = +2

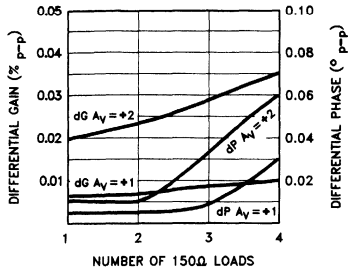


2070-6

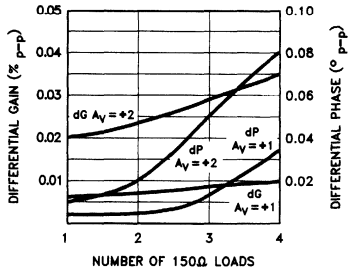
EL2070C
200 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

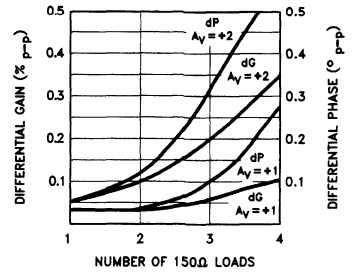
Differential Gain and Phase (3.58 MHz)



Differential Gain and Phase (4.43 MHz)

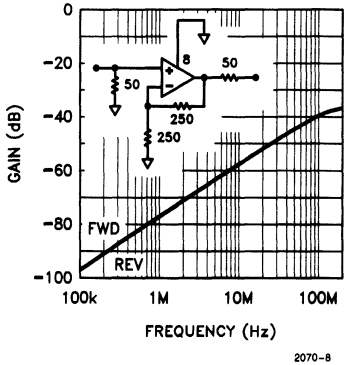


Differential Gain and Phase (30 MHz)



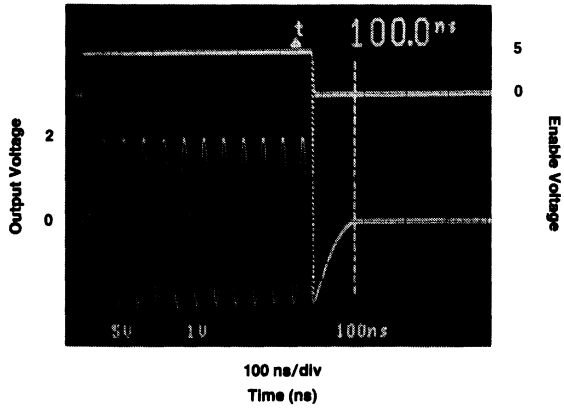
2070-7

Forward and Reverse Gain during Disable



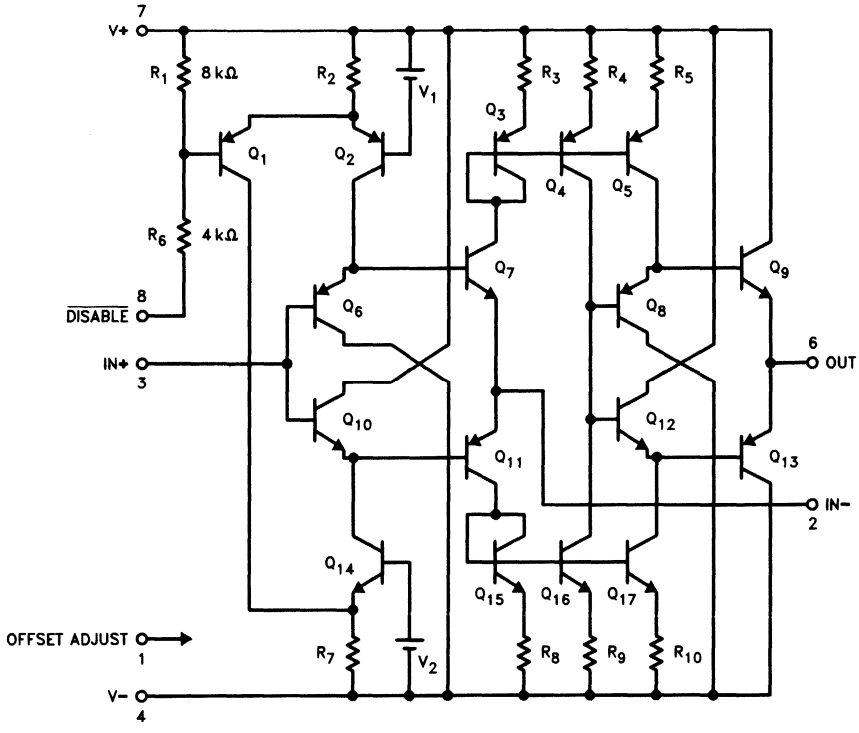
2070-8

Enable/Disable Response



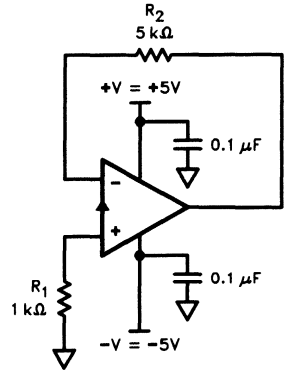
2070-9

Equivalent Circuit



2070-10

Burn-In Circuit



2070-11

ALL PACKAGES USE THE SAME SCHEMATIC.

EL2070C
200 MHz Current Feedback Amplifier

Applications Information

Theory of Operation

The EL2070 has a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL2070 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (R_{OL}) of the EL2070 [V_{OUT} = (R_{OL}) * ($-I_{IN}$)]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2070. The nominal value for the feedback resistor is 250Ω, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Differential Gain/Phase

An industry-standard method of measuring the distortion of a video component is to measure the amount of differential gain and phase error it introduces. To measure these, a 40 IRE_{PP} reference signal is applied to the device with 0V DC offset (0 IRE) at 3.58 MHz for NTSC, 4.43 MHz for PAL, and 30 MHz for HDTV. A second measurement is then made with a 0.714V DC offset (100 IRE). Differential Gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential Phase is a measure of the change in phase, and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak values.

In general, a back terminated cable (75Ω in series at the drive end and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double-termination is used, the received signal is reduced by half; therefore a gain of 2 configuration is typically used to compensate for the attenuation. In a gain of 2 configuration, with output swing of 2 V_{PP}, with each back-terminated load at 150Ω. The EL2070 is capable of driving up to 4 back-terminated loads with excellent video performance. Please refer to the typical curves for more information on video performance with respect to frequency, gain, and loading.

Capacitive Feedback

The EL2070 relies on its feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Applications Information — Contd.

Offset Adjustment Pin

Output offset voltage of the EL2070 can be nulled by tying a 10k potentiometer between $+V_S$ and $-V_S$ with the slider attached to pin 1. A full-range variation of the voltage at pin 1 to ±5V results in an offset voltage adjustment of at least ±10 mV. For best settling performance pin 1 should be bypassed to ground with a ceramic capacitor located near to the package, even if the offset voltage adjustment feature is not being used.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply and Offset Adjust bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling to the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL2070 allows a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

Disable/Enable Operation

The EL2070 has a disable/enable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or tied to pin 7. When more than 350 μA is pulled from pin 8, the EL2070 is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is reduced by ⅔. To make it easy to use this feature, there is an internal resistor to limit the current to a safe level (0.8 mA) if pin 8 is grounded.

To draw current out of pin 8 an open-collector TTL output, a 5V CMOS output, or an NPN transistor can be used.

EL2070C
200 MHz Current Feedback Amplifier

EL2070 Macromodel

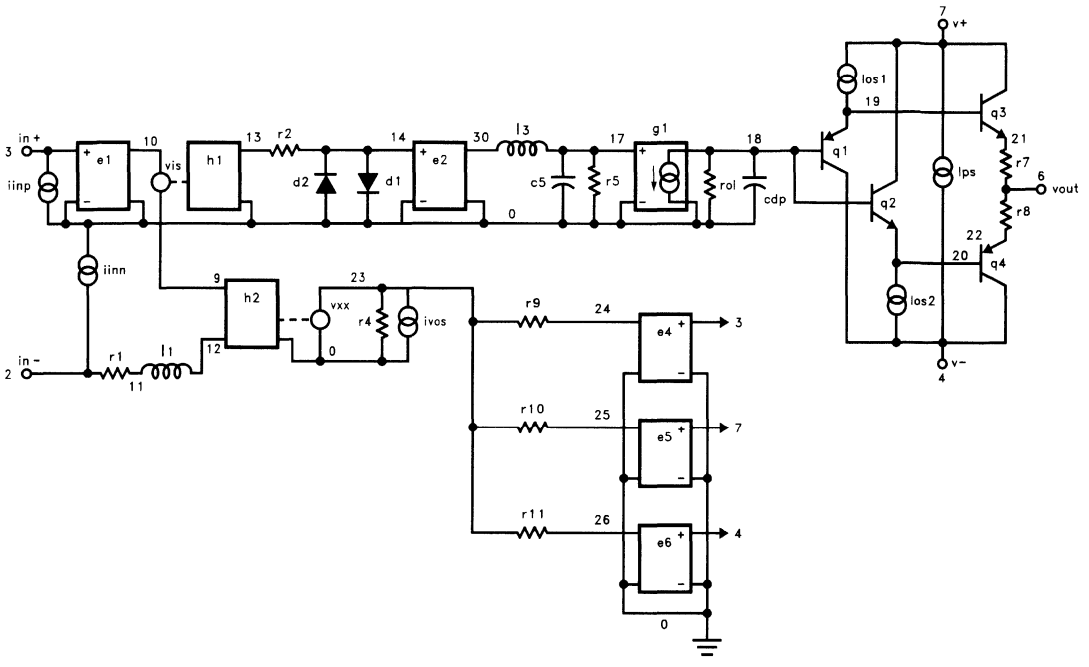
```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2070       3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 8µA
iinm 2 0 8µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l3 30 17 0.1µH
c5 17 0 0.1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 2
r8 22 6 2
```

EL2070 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is = 5e - 15 bf = 200 tf = 0.05nS)
.model qp pnp (is = 5e - 15 bf = 200 tf = 0.05nS)
.model dclamp d(is = 1e - 30 ibv = 0.266 bv = 1.3 n = 4)
.ends
```

EL2070C
200 MHz Current Feedback Amplifier

EL2070 Macromodel — Contd.



2070-12

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL400C
200 MHz Current Feedback Amplifier

Features

- 200 MHz −3 dB bandwidth, $A_V = 2$
- 12 ns settling to 0.05%
- $V_S = \pm 5V$ @ 15 mA
- Low distortion: HD2, HD3 @ −60 dBc at 20 MHz
- Differential gain 0.02% at NTSC, PAL
- Differential phase 0.01° at NTSC, PAL
- Overload/short-circuit protected
- ±1 to ±8 closed-loop gain range
- Low cost
- Direct replacement for CLC400

Applications

- Video gain block
- Video distribution
- HDTV amplifier
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL400CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL400CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL400 is a wide bandwidth, fast settling monolithic amplifier built using an advanced complementary bipolar process. This amplifier uses current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±1 to ±8, the EL400 has a 200 MHz −3 dB bandwidth ($A_V = +2$), and 12 ns settling to 0.05% while consuming only 15 mA of supply current.

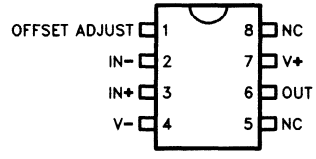
The EL400 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current, differential gain/phase of 0.02%/0.01°, and a minimum 50 mA output drive, performance in these areas is assured.

The EL400's settling to 0.05% in 12 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 200 MHz bandwidth and extremely linear phase allow unmatched signal fidelity. D/A systems can also benefit from the EL400, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, *QRA-1: Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



Top View

EL400C
200 MHz Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V	Lead Temperature (Soldering, 5 Seconds)	300°C
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.	Junction Temperature	175°C
		Storage Temperature	−60°C to +150°C
		Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8
Common-Mode Input Voltage	$\pm V_S$		
Differential Input Voltage	5V		
Power Dissipation	See Curves		
Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±5V, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL400C	Units
V_{OS}	Input Offset Voltage		25°C		2.0	5.5	I	mV
			T_{MIN}			8.7	III	mV
			T_{MAX}			9.5	III	mV
$d(V_{OS})/dT$	Average Offset Voltage Drift	(Note 1)	All		10.0	40.0	IV	µV/°C
$+I_{IN}$	+Input Current		25°C, T_{MAX}		10.0	25.0	II	µA
			T_{MIN}			41.0	III	µA
$d(+I_{IN})/dT$	Average +Input Current Drift	(Note 1)	All		50.0	200.0	IV	nA/°C
$-I_{IN}$	−Input Current		25°C		10.0	25.0	I	µA
			T_{MIN}			41.0	III	µA
			T_{MAX}			35.0	III	µA
$d(-I_{IN})/dT$	Average −Input Current Drift	(Note 1)	All		100.0	200.0	IV	nA/°C
PSRR	Power Supply Rejection Ratio		All	40.0	50.0		II	dB
CMRR	Common-Mode Rejection Ratio		All	40.0	50.0		II	dB
I_S	Supply Current—Quiescent	No Load	All		15.0	23.0	II	mA

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL400C	Units
$+R_{IN}$	+Input Resistance		25°C, T_{MAX}	100.0	200.0		II	kΩ
			T_{MIN}	50.0			III	kΩ
C_{IN}	Input Capacitance		All		0.5	2.0	IV	pF
R_{OUT}	Output Impedance (DC)		All		0.1	0.2	IV	Ω
CMIR	Common-Mode Input Range	(Note 2)	25°C, T_{MAX}	2.0	2.1		IV	V
			T_{MIN}	1.2			IV	V
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		II	mA
			T_{MIN}	35.0			III	mA
V_{OUT}	Output Voltage Swing	No Load	All	3.2	3.5		II	V
$V_{OUT}L$	Output Voltage Swing	100Ω	25°C	3.0	3.4		I	V
R_{OL}	Transimpedance		25°C	30.0	125.0		II	V/mA
			T_{MIN}		80.0		V	V/mA
			T_{MAX}		140.0		V	V/mA

Closed-Loop AC Electrical Characteristics

V_S = ±5V, R_F = 250Ω, A_V = +2, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL400C	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth (V_{OUT} < 0.5 V_{PP})		25°C	150.0	200.0		III	MHz
			T_{MIN}	150.0			IV	MHz
			T_{MAX}	120.0			IV	MHz
LSBW	−3 dB Bandwidth (V_{OUT} < 5.0 V_{PP})	A_V = +5	All	35.0	50.0		IV	MHz
GAIN FLATNESS								
GFPL	Peaking V_{OUT} < 0.5 V_{PP}	<40 MHz	25°C		0.0	0.3	III	dB
			T_{MIN}, T_{MAX}			0.4	IV	dB
GFPH	Peaking V_{OUT} < 0.5 V_{PP}	>40 MHz	25°C		0.0	0.5	III	dB
			T_{MIN}, T_{MAX}			0.7	IV	dB
GFR	Rolloff V_{OUT} < 0.5 V_{PP}	<75 MHz	25°C		0.6	1.0	III	dB
			T_{MIN}			1.0	IV	dB
			T_{MAX}			1.3	IV	dB
LPD	Linear Phase Deviation V_{OUT} < 0.5 V_{PP}	<75 MHz	25°C, T_{MIN}		0.2	1.0	IV	°
			T_{MAX}			1.2	IV	°

EL400C
200 MHz Current Feedback Amplifier

Closed-Loop AC Electrical Characteristics — Contd.

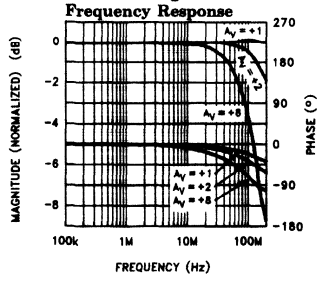
$V_S = \pm 5V$, $R_F = 250\Omega$, $A_V = +2$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL400C	Units
TIME-DOMAIN RESPONSE								
t_{r1}, t_{f1}	Rise Time, Fall Time	0.5V Step	25°C, T_{MIN}		1.6	2.4	IV	ns
			T_{MAX}			2.9	IV	ns
t_{r2}, t_{f2}	Rise Time, Fall Time	5.0V Step	All		6.5	10.0	IV	ns
t_{s1}	Settling Time to 0.1%	2.0V Step	All		10.0	13.0	IV	ns
t_{s2}	Settling Time to 0.05%	2.0V Step	All		12.0	15.0	IV	ns
OS	Overshoot	0.5V Step	25°C		0.0	10.0	IV	%
			T_{MIN}, T_{MAX}			15.0	IV	%
SR	Slew Rate	$A_V = +2$	All	430.0	700.0		IV	V/µs
		$A_V = -2$	All		1600.0		V	V/µs
DISTORTION								
HD2	2nd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−60.0	−45.0	III	dBc
			T_{MIN}			−40.0	IV	dBc
			T_{MAX}			−45.0	IV	dBc
HD3	3rd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−60.0	−50.0	III	dBc
			T_{MIN}, T_{MAX}			−50.0	IV	dBc
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz	(Note 3)	25°C		−157.0	−154.0	IV	dBm (1 Hz)
			T_{MIN}			−154.0	IV	dBm (1Hz)
			T_{MAX}			−153.0	IV	dBm (1Hz)
INV	Integrated Noise 100 kHz to 200 MHz	(Note 3)	25°C		40.0	57.0	IV	µV
			T_{MIN}			57.0	IV	µV
			T_{MAX}			63.0	IV	µV
VIDEO PERFORMANCE								
d_G	Differential Gain (Note 4)	NTSC/PAL	25°C		0.02		V	% pp
d_P	Differential Phase (Note 4)	NTSC/PAL	25°C		0.01		V	° pp
d_G	Differential Gain (Note 4)	30 MHz	25°C		0.05		V	% pp
d_P	Differential Phase (Note 4)	30 MHz	25°C		0.05		V	° pp
VBW	−0.1 dB Bandwidth (Note 4)		25°C		60.0		V	MHz

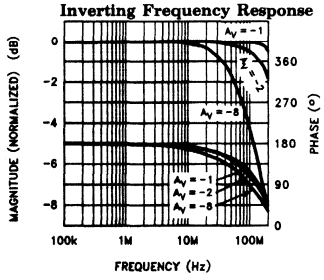
Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: Common-Mode Input Range for Rated Performance.
Note 3: Noise Tests are Performed from 5 MHz to 200 MHz.
Note 4: Differential Gain/Phase Tests are $R_L = 100\Omega$. For other values of R_L, see curves.

Typical Performance Curves

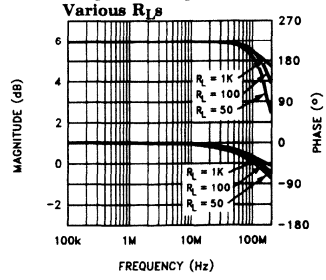
Non-Inverting Frequency Response



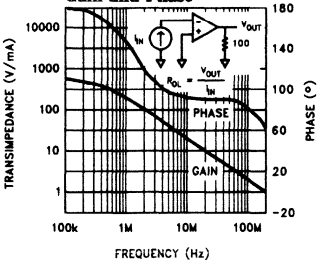
Inverting Frequency Response



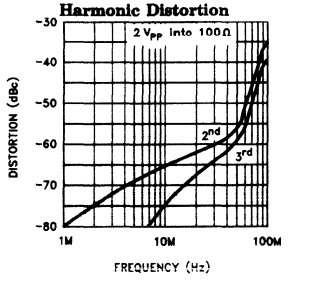
Frequency Response for Various R_Ls



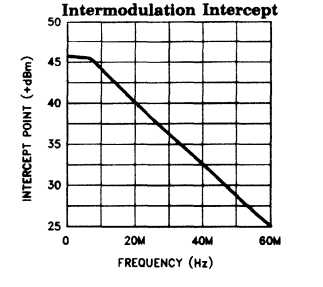
Open-Loop Transimpedance Gain and Phase



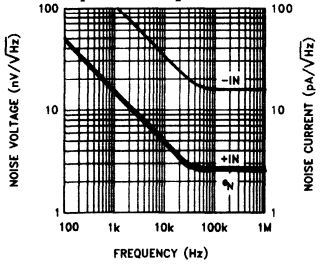
2nd and 3rd Harmonic Distortion



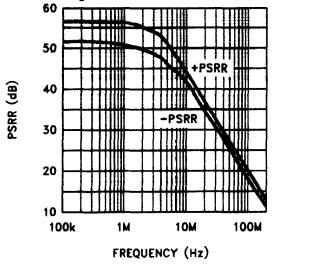
2-Tone 3rd Order Intermodulation Intercept



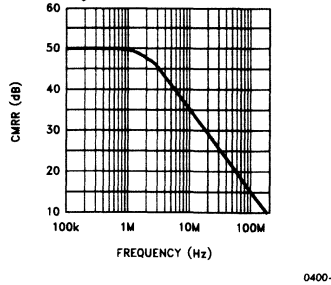
Equivalent Input Noise



Power-Supply Rejection Ratio

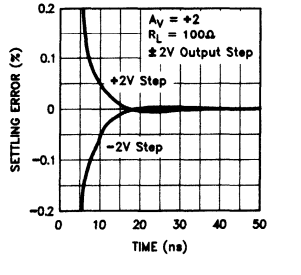


Common-Mode Rejection Ratio

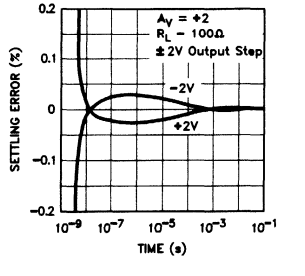


0400-2

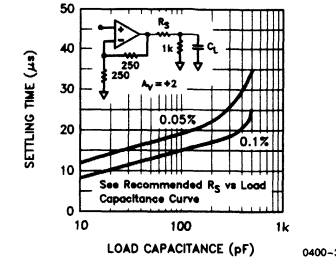
Settling Time



Long-Term Settling Time



Settling Time vs Load Capacitance

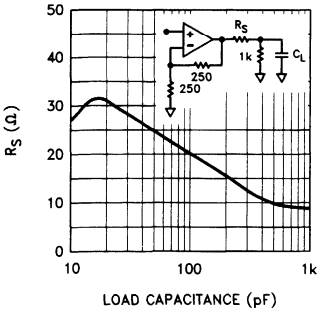


0400-3

EL400C
200 MHz Current Feedback Amplifier

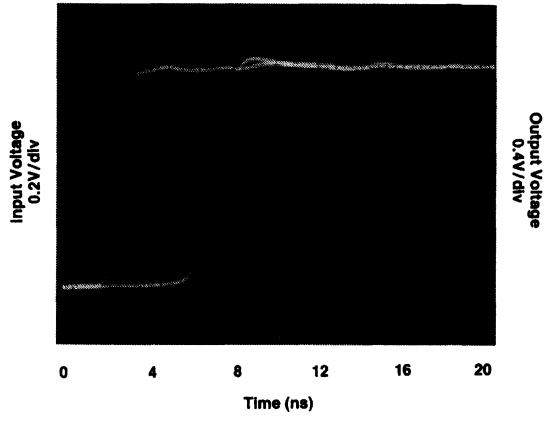
Typical Performance Curves — Contd.

Recommended R_S vs Load Capacitance



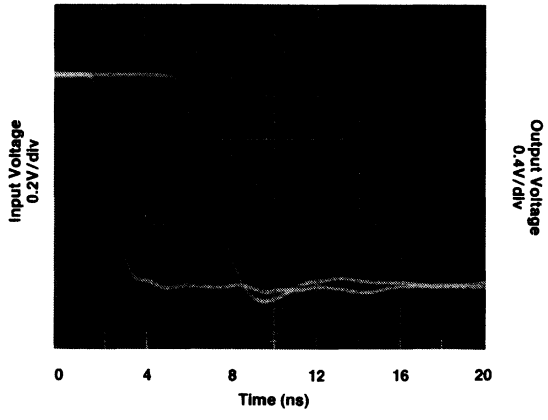
0400-4

Pulse Response A_V = +2



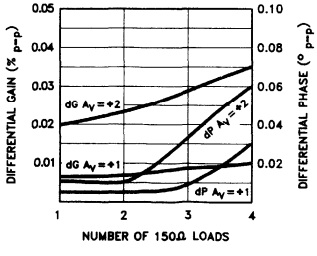
0400-5

Pulse Response A_V = +2

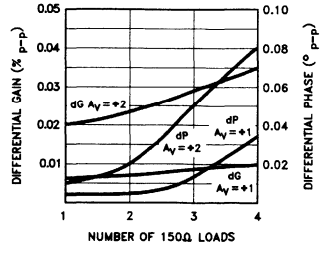


0400-6

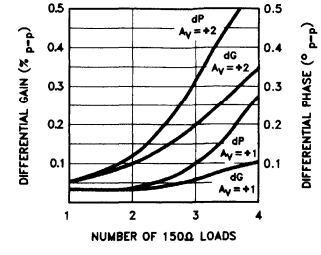
Differential Gain and Phase (3.58 MHz)



Differential Gain and Phase (4.43 MHz)

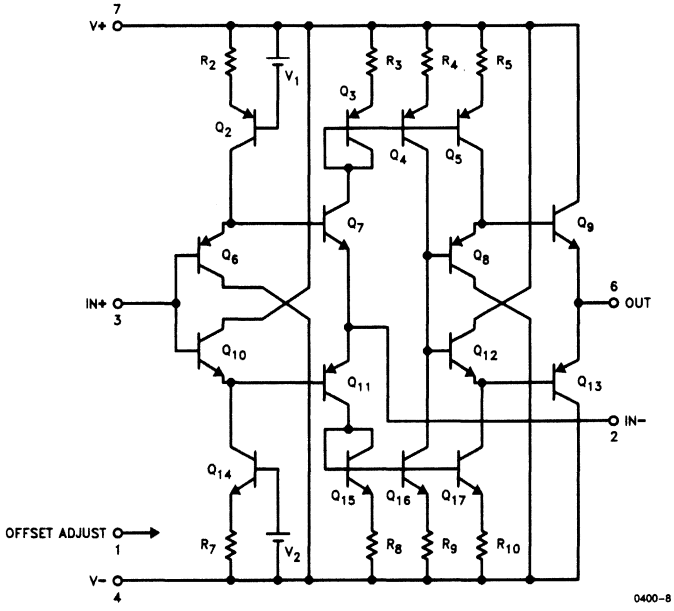


Differential Gain and Phase (30 MHz)

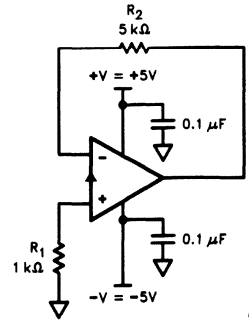


0400-7

Equivalent Circuit



Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC.

Applications Information

Theory of Operation

The EL400 has a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL400 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (R_{OL}) of the EL400 [$V_{OUT} = (R_{OL}) * (-I_{IN})$]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL400. The nominal value for the feedback resistor is 250Ω, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Differential Gain/Phase

An industry-standard method of measuring the distortion of a video component is to measure the amount of differential gain and phase error it introduces. To measure these, a 40 IRE_{PP} reference signal is applied to the device with 0V DC offset (0IRE) at 3.58 MHz for NTSC, 4.43 MHz for

EL400C
200 MHz Current Feedback Amplifier

Applications Information — Contd.

PAL, and 30 MHz for HDTV. A second measurement is then made with a 0.714V DC offset (100IRE). Differential Gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential Phase is a measure of the change in phase, and is measured in degrees. Typically, the maximum positive and negative deviations are summed to give peak values.

In general, a back terminated cable (75Ω in series at the drive end and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double-termination is used, the received signal is reduced by half; therefore a gain of 2 configuration is typically used to compensate for the attenuation. In a gain of 2 configuration, with output swing of 2 V_{PP}, with each back-terminated load at 150Ω. The EL400 is capable of driving up to 4 back-terminated loads with excellent video performance. Please refer to the typical curves for more information on video performance with respect to frequency, gain, and loading.

Capacitive Feedback

The EL400 relies on its feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

Offset Adjustment Pin

Output offset voltage of the EL400 can be nulled by tying a 10k potentiometer between $+V_S$ and $-V_S$ with the slider attached to pin 1. A full-range variation of the voltage at pin 1 to ±5V results in an offset voltage adjustment of at least ±10 mV. For best settling performance pin 1 should be bypassed to ground with a ceramic capacitor located near to the package, even if the offset voltage adjustment feature is not being used.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply and Offset Adjust bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling the ground plane as possible.

Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL400 allows a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

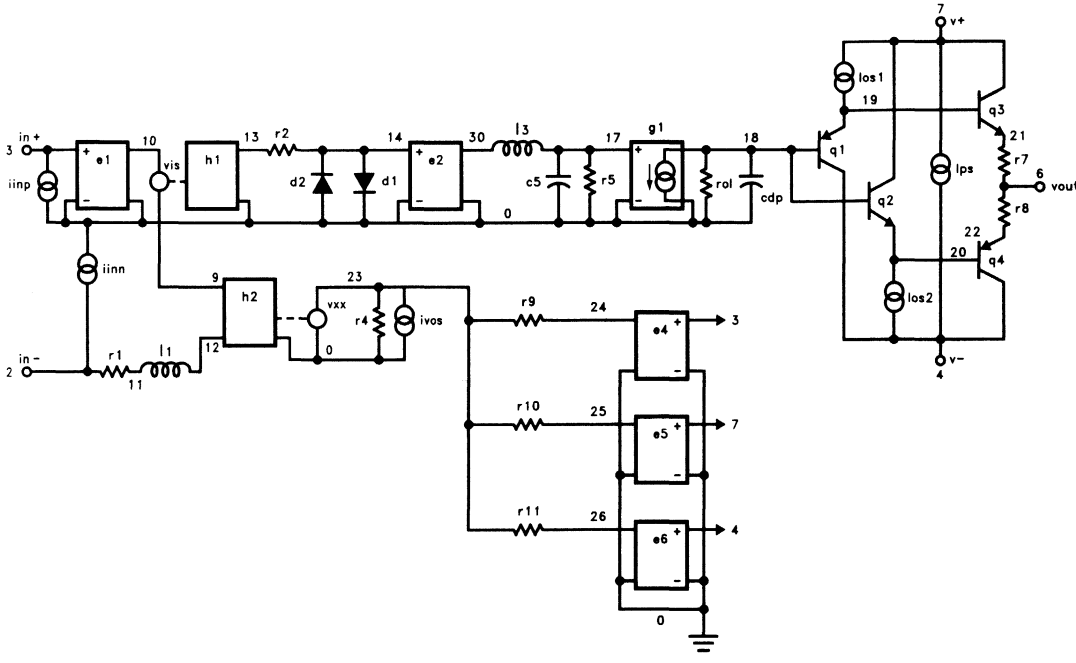
EL400 Macromodel

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M400        3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 48nH
iinp 3 0 8µA
iinm 2 0 8µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.1µH
c5 17 0 0.1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 150K
cdp 18 0 2.8pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 2
r8 22 6 2
```

EL400 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is = 5e-15 bf = 200 tf = 0.5nS)
.model qp pnp (is = 5e-15 bf = 200 tf = 0.5nS)
.model dclamp d(is = 1e-30 ibv = 0.266 bv = 1.3 n = 4)
.ends
```

EL400 Macromodel — Contd.



0400-10

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2071C/EL2171C
150 MHz Current Feedback Amplifier

Features

- 150 MHz − 3 dB bandwidth, $A_V = 20$
- 10 ns settling to 0.1%
- $V_S = \pm 5V$ @ 15 mA
- 2.5 ns rise/fall times (2V step)
- Overload/short-circuit protected
- ±7 to ±50 closed-loop gain range
- Low cost
- EL2171 is direct replacement for CLC401
- Disable capability on EL2071

Applications

- Line drivers
- DC-coupled log amplifiers
- High-speed modems, radios
- High-speed A/D conversion
- D/A I-V conversion
- Photodiode, CCD preamps
- IF processors
- High-speed communications
- Analog multiplexing (using disable—EL2071)
- Power down mode (using disable—EL2071)

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2171CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2171CS	−40°C to +85°C	8-Lead SO	MDP0027
EL2071CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2071CS	−40°C to +85°C	8-Lead SO	MDP0027

General Description

The EL2071 and EL2171 are wide bandwidth, fast settling monolithic amplifiers built using an advanced complementary bipolar process. The EL2071 has a disable/enable feature which allows power down and analog multiplexing. These amplifiers use current-mode feedback to achieve more bandwidth at a given gain than conventional operational amplifiers. Designed for closed-loop gains of ±7 to ±50, the EL2071 and EL2171 have a 150 MHz − 3 dB bandwidth ($A_V = +20$), and 2.5 ns rise/fall time, while consuming only 15 mA of supply current. The EL2071 consumes only 1.5 mA when disabled.

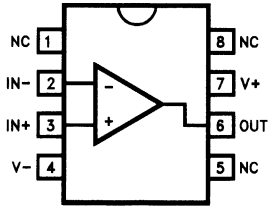
The wide 150 MHz bandwidth and extremely linear phase (0.2 dB deviation from linear at 50 MHz) allow superior signal fidelity. These features make the EL2071 and EL2171 especially suited for many digital communication system applications.

The EL2071's and EL2171's settling to 0.1% in 10 ns and ability to drive capacitive loads make them ideal in flash A/D applications. D/A systems can also benefit from the EL2071 and EL2171, especially if linearity and drive levels are important.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, *QRA-1: Elantec's Processing, Monolithic Integrated Circuits.*

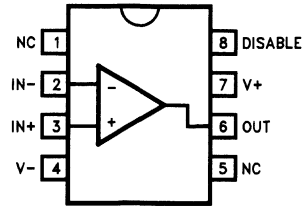
Connection Diagrams

EL2171
DIP and SO Package



Top View

EL2071
DIP and SO Package



Top View

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common Mode Input Voltage	±V_S
Differential Input Voltage	5V
Power Dissipation	See Curves
Operating Temperature	−40°C to +85°C

Lead Temperature	
DIP Package	300°C
(Soldering: <5 Seconds-CN; <10 Seconds-J)	
SO Package	
Vapor Phase (60 Seconds)	215°C
Infrared (15 seconds)	220°C
Operating Junction Temperature	
Ceramic Packages	175°C
Plastic Packages	150°C
Storage Temperature	−60°C to +150°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		3	6	I	mV
			T_{MIN}, T_{MAX}			10	III	mV
TC V_{OS}	Average Offset Voltage Drift	(Note 1)	All		20	50	IV	µV/°C
$+I_{IN}$	+Input Current		25°C, T_{MAX}		10	20	II	µA
			T_{MIN}			36	III	µA
TC ($+I_{IN}$)	Average +Input Current Drift	(Note 1)	All		100	200	IV	nA/°C
$-I_{IN}$	−Input Current		25°C		10	30	I	µA
			T_{MIN}			46	III	µA
			T_{MAX}			40	III	µA
TC ($-I_{IN}$)	Average −Input Current Drift	(Note 1)	All		100	200	IV	nA/°C

EL2071C/EL2171C
150 MHz Current Feedback Amplifier

Open Loop DC Electrical Characteristics
V_S = ±5V, R_L = 100Ω, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
PSRR	Power Supply Rejection Ratio	(Note 2)	All	50	55		II	dB
CMRR	Common-Mode Rejection Ratio		All	40	50		II	dB
I_S	Supply Current—Quiescent	No Load	All		15	21	II	mA
$I_{S_{OFF}}$	Supply Current—Disabled	EL2071C (Note 3)	All		1.5	3.0	II	mA
$+R_{IN}$	+Input Resistance		25°C, T_{MAX}	100	200		II	kΩ
			T_{MIN}	50			III	kΩ
C_{IN}	Input Capacitance		All		0.5	2.5	IV	pF
R_{OUT}	Output Resistance (DC)		All		0.2	0.3	IV	Ω
R_{OUT_D}	Output Resistance (DC)	EL2071C Disabled	All	100	200		IV	kΩ
C_{OUT_D}	Output Capacitance (DC)	EL2071C Disabled	All		0.5	2.0	IV	pF
CMIR	Common-Mode Input Range	(Note 4)	25°C, T_{MAX}	±2.5	±2.8		IV	V
			T_{MIN}	±2			IV	V
I_{OUT}	Output Current		25°C, T_{MAX}	50	70		II	mA
			T_{MIN}	35			III	mA
V_{OUT}	Output Voltage Swing	No Load	25°C, T_{MAX}	3.2	3.5		II	V
			T_{MIN}	3			II	V
V_{OUT_L}	Output Voltage Swing	R_L = 100Ω	25°C	3.2	3.4		I	V
R_{OL}	Transimpedance		25°C	250	1000		I	V/mA
I_{LOGIC}	Pin 8 Current @ +5V	EL2071C	All		500	750	II	μA
V_{DIS}	Minimum Pin 8 V to Disable	EL2071C	25°C	4.3			II	V
			T_{MIN}	4.0				
			T_{MAX}	4.6				
V_{EN}	Maximum Pin 8 V to Enable	EL2071C	All			0.7	II	V
I_{DIS}	Minimum Pin 8 I to Disable	EL2071C	All	750			II	μA
I_{EN}	Maximum Pin 8 I to Enable	EL2071C	All			35	II	μA

Closed Loop AC Electrical Characteristics

$V_S = \pm 5V$, $R_F = 1.5\ k\Omega$, $A_V = +20$, $R_L = 100\Omega$ unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth (V_{OUT} <2.0 V_{PP})		25°C	100	150		III	MHz
			T_{MIN}	100			IV	MHZ
			T_{MAX}	70			IV	MHz
LSBW	−3 dB Bandwidth (V_{OUT} < 5.0 V_{PP})		25°C, T_{MIN}	65	100		IV	MHz
			T_{MAX}	55			IV	MHz
GAIN FLATNESS								
GFPL	Peaking V_{OUT} < 2.0 V_{PP}	<25 MHz	25°C		0.0	0.1	III	dB
			T_{MIN}, T_{MAX}			0.1	IV	dB
GFPH	Peaking V_{OUT} < 2.0 V_{PP}	>25 MHz	25°C		0.0	0.2	III	dB
			T_{MIN}, T_{MAX}			0.2	IV	dB
GFR	Rolloff V_{OUT} < 2.0 V_{PP}	<50 MHz	25°C		0.2	1.0	III	dB
			T_{MIN}			1.0	IV	dB
			T_{MAX}			1.3	IV	dB
LPD	Linear Phase Deviation V_{OUT} < 2.0 V_{PP}	<50 MHz	25°C, T_{MIN}		0.2	1.0	IV	°
			T_{MAX}			1.5	IV	°
TIME-DOMAIN RESPONSE								
t_{r1}, t_{f1}	Rise Time, Fall Time	2.0V Step	25°C, T_{MIN}		2.5	3.5	IV	ns
			T_{MAX}			5	IV	ns
t_{r2}, t_{f2}	Rise Time, Fall Time	5.0V Step	25°C, T_{MIN}		5	7	IV	ns
			T_{MAX}			8	IV	ns
t_s	Settling Time to 0.1%	2.0V Step	All		10	15	IV	ns
OS	Overshoot	2.0V Step	All		0	10	IV	%
SR	Slew Rate		25°C, T_{MIN}	800	1200		IV	V/μs
			T_{MAX}	700			IV	V/μs
DISTORTION								
HD2	2nd Harmonic Distortion @20 MHz	2 V_{PP}	25°C		−45	−35	III	dBc
			T_{MIN}, T_{MAX}			−35	IV	dBc
HD3	3rd Harmonic Distortion @20 MHz	2 V_{PP}	25°C		−60	−50	III	dBc
			T_{MIN}			−50	IV	dBc
			T_{MAX}			−45	IV	dBc

EL2071C/EL2171C
150 MHz Current Feedback Amplifier

Closed Loop AC Electrical Characteristics

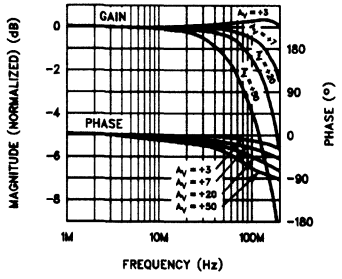
$V_S = \pm 5V$, $R_F = 1.5\ k\Omega$, $A_V = +20$, $R_L = 100\Omega$ unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz		25°C		−158	−155	IV	dBm (1 Hz)
			T_{MIN}			−155	IV	dBm (1 Hz)
			T_{MAX}			−154	IV	dBm (1 Hz)
INV	Integrated Noise 100 kHz to 200 MHz		25°C		35	50	IV	μV
			T_{MIN}			50	IV	μV
			T_{MAX}			55	IV	μV
DISABLE/ENABLE PERFORMANCE—EL2071C								
T_{OFF}	$V_{OUT} = 2\ V_{PP}$ Disable Time to >40 dB	20 MHz	All		70	200	IV	ns
T_{ON}	Enable Time		All		40	100	IV	ns
ISO	Off Isolation	20 MHz	All	50	55		IV	dB

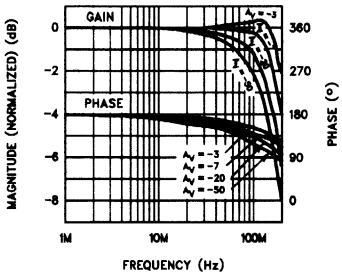
Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: PSRR is measured at $V_S = \pm 4.5V$ and $V_S = \pm 5.5V$. Both supplies are changed simultaneously.
Note 3: Supply current when disabled is measured at the negative supply.
Note 4: Common-Mode Input Range for Rated Performance.

Typical Performance Curves

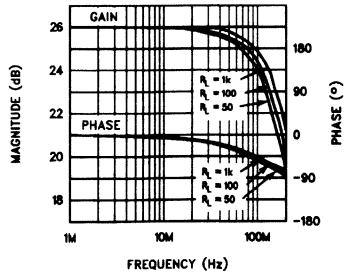
Non-Inverting Frequency Response



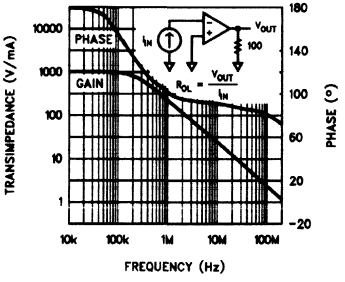
Inverting Frequency Response



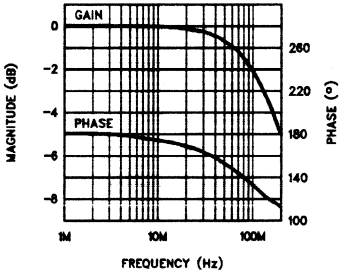
Frequency Response for Various R_Ls



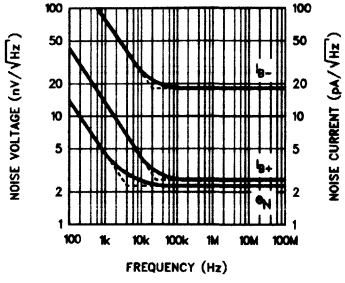
Open-Loop Transimpedance Gain and Phase



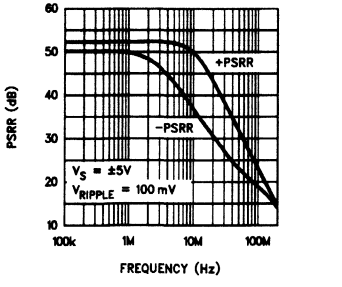
Frequency Response, $A_V = -1$, $R_F = 2.5\ k\Omega$



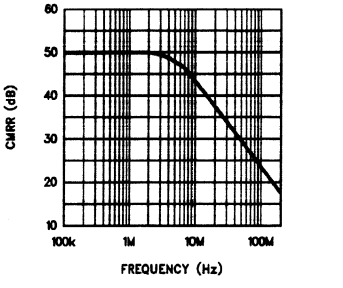
Equivalent Input Noise



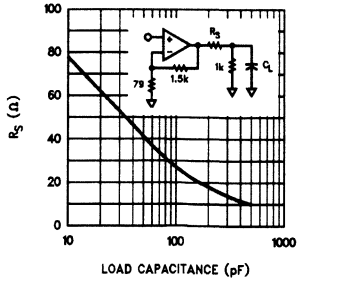
Single Power Supply Rejection Ratio



Common Mode Rejection Ratio ($A_V = +20$)



Recommended R_S vs Load Capacitance

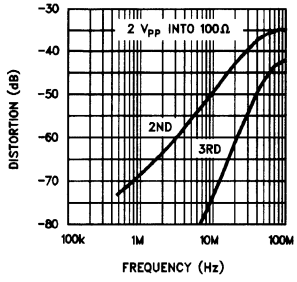


2071-3

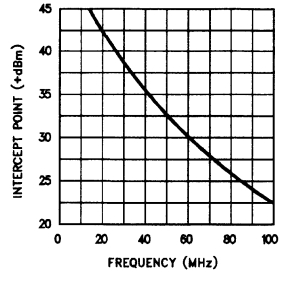
EL2071C/EL2171C
150 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

2nd and 3rd Harmonic Distortion

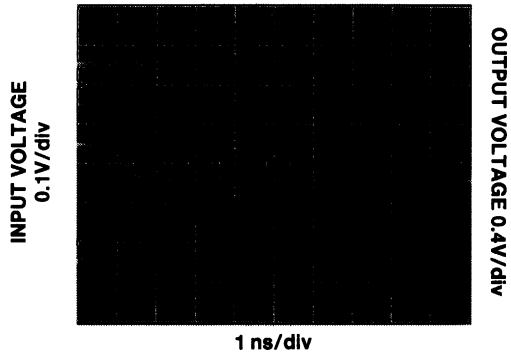


2-Tone 3rd Order Intermodulation Intercept



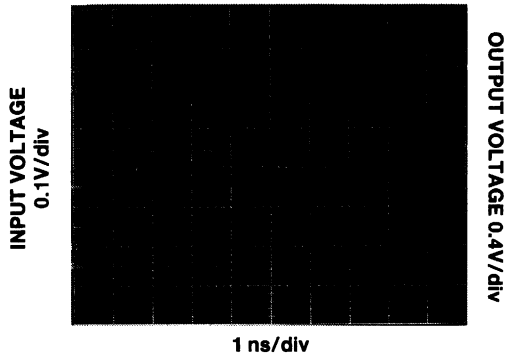
2071-4

Pulse Response A_V = +20



2071-5

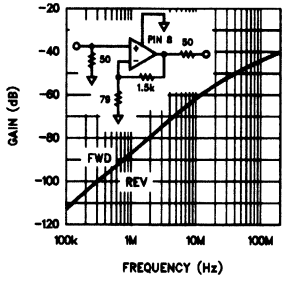
Pulse Response A_V = +20



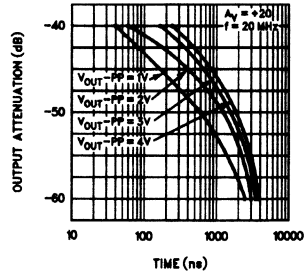
2071-6

Typical Performance Curves — Contd.

Forward and Reverse Gain during Disable—EL2071C

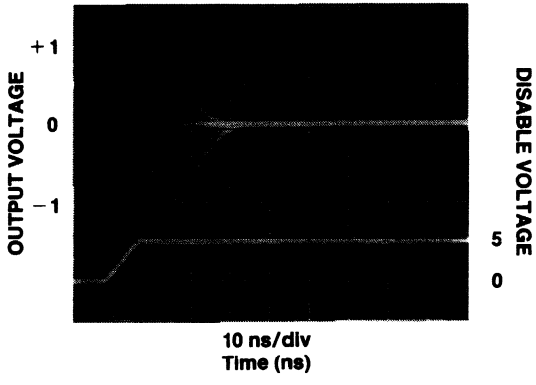


Disabled Attenuation vs Time for Various Output Levels—EL2071C



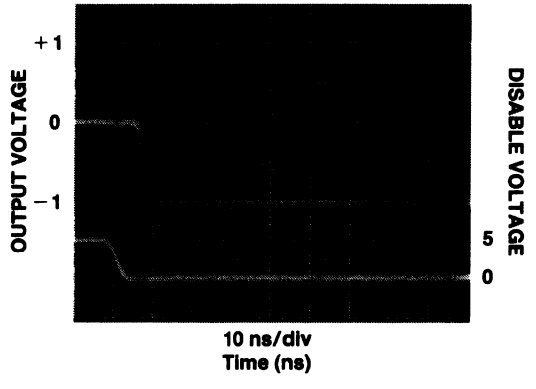
2071-7

Disable Response—EL2071C



2071-8

Enable Response—EL2071C

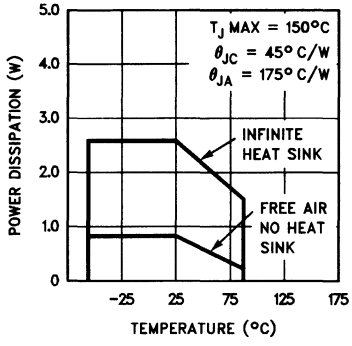


2071-9

EL2071C/EL2171C
150 MHz Current Feedback Amplifier

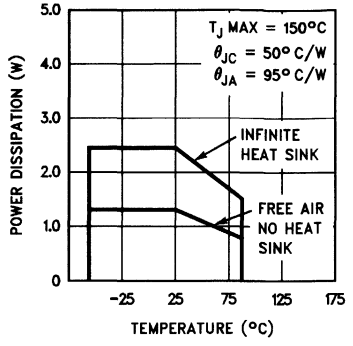
Typical Performance Curves — Contd.

8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



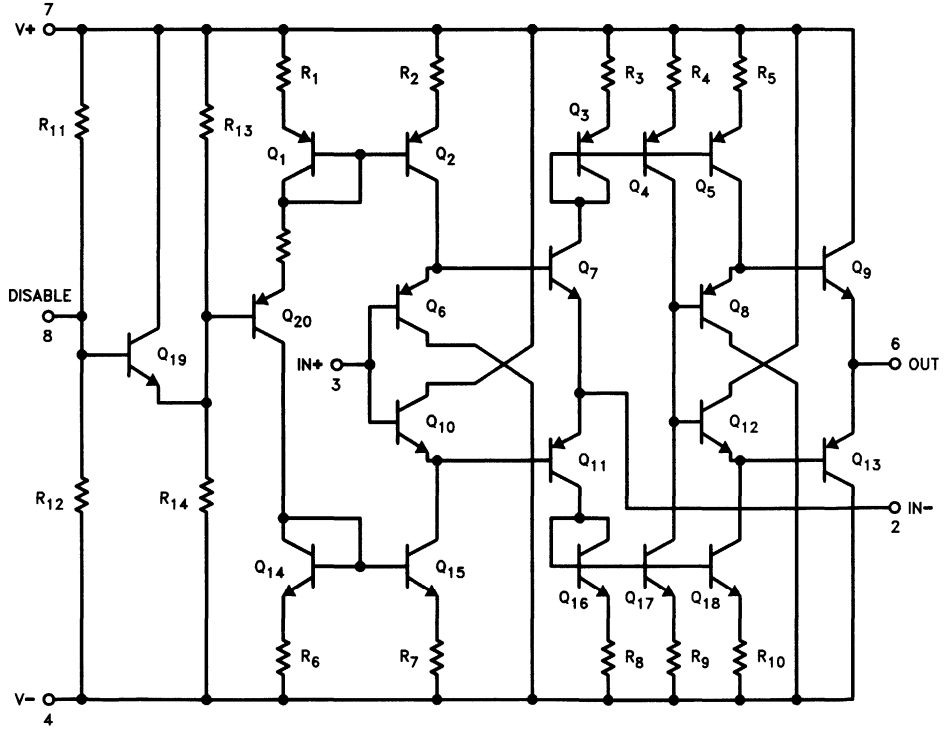
2071-10

8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



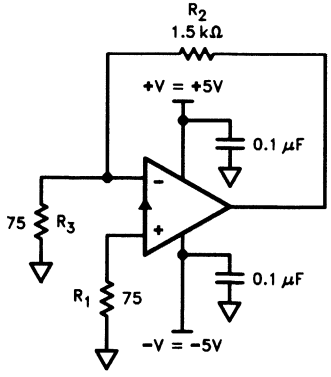
2071-11

Equivalent Circuit



2071-13

Burn-In Circuit



ALL PACKAGES USE THE SAME SCHEMATIC.

Applications Information

Theory of Operation

The EL2071/EL2171 have a unity gain buffer from the non-inverting input to the inverting input. The error signal of the EL2071/EL2171 is a current flowing into (or out of) the inverting input. A very small change in current flowing through the inverting input will cause a large change in the output voltage. This current amplification is called the transimpedance (R_{OL}) of the EL2071/EL2171 [$V_{OUT} = (R_{OL}) * (-I_{IN})$]. Since R_{OL} is very large, the current flowing into the inverting input in the steady-state (non-slewing) condition is very small.

Therefore we can still use op-amp assumptions as a first-order approximation for circuit analysis, namely that:

1. The voltage across the inputs is approximately 0V.
2. The current into the inputs is approximately 0 mA.

Resistor Value Selection and Optimization

The value of the feedback resistor (and an internal capacitor) sets the AC dynamics of the EL2071/EL2171. The nominal value for the feedback resistor is 1.5 kΩ, which is the value used for production testing. This value guarantees stability. For a given closed-loop gain the bandwidth may be increased by decreasing the feedback resistor and, conversely, the bandwidth may be decreased by increasing the feedback resistor.

Reducing the feedback resistor too much will result in overshoot and ringing, and eventually oscillations. Increasing the feedback resistor results in a lower −3 dB frequency. Attenuation at high frequency is limited by a zero in the closed-loop transfer function which results from stray capacitance between the inverting input and ground. Consequently, it is very important to keep stray capacitance to a minimum at the inverting input.

Capacitive Feedback

The EL2071/EL2171 rely on their feedback resistor for proper compensation. A reduction of the impedance of the feedback element results in less stability, eventually resulting in oscillation. Therefore, circuit implementations which have capacitive feedback should not be used because of the capacitor's impedance reduction with frequency. Similarly, oscillations can occur when using the technique of placing a capacitor in parallel with the feedback resistor to compensate for shunt capacitances from the inverting input to ground.

EL2071C/EL2171C
150 MHz Current Feedback Amplifier

Applications Information — Contd.

Printed Circuit Layout

As with any high frequency device, good PCB layout is necessary for optimum performance. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. The inverting input is sensitive to stray capacitance, therefore connections at the inverting input should be minimal, close to the package, and constructed with as little coupling to the ground plane as possible.

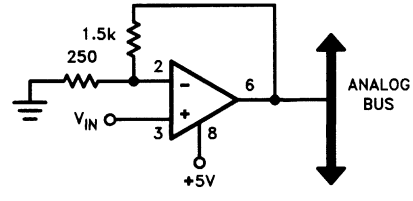
Capacitance at the output node will reduce stability, eventually resulting in peaking, and finally oscillation if the capacitance is large enough. The design of the EL2071/EL2171 allow a larger capacitive load than comparable products, yet there are occasions when a series resistor before the capacitance may be needed. Please refer to the graphs to determine the proper resistor value needed.

Disable/Enable Operation for EL2071C

The EL2071C has a disable/enable control input at pin 8. The device is enabled and operates normally when pin 8 is left open or returned to ground. When the voltage at pin 8 is brought to within 0.4V of pin 7 (V_S+), the EL2071C is disabled. The output becomes a high impedance, the inverting input is no longer driven to the positive input voltage, and the supply current is reduced to less than 2.2. mA. There are internal resistors which limit the current at pin 8 to a safe level ($\sim \pm 500\ \mu A$) if pin 8 is shorted to either supply.

Typically, analog and digital circuits should have separate power supplies. This usually leads to slight differences between the power supply voltages. The EL2071C's disable feature is dependent on the voltage at pins 8 and 7. Therefore, to operate the disable feature of the EL2071C dependably over temperature, it is recommended that the logic circuitry which drives pin 8 of the EL2071C operate from the same +5V supply as the EL2071C to avoid voltage differences between the digital and analog power supplies. Since V_{DIS} is temperature dependent, it is recommended that 5V CMOS logic (with a $V_{OH} > 4.6V$ sourcing $> 750\ \mu A$ over temperature) be used to drive the disable pin of the EL2071C.

When disabled, (as well as in enabled mode), care must be taken to prevent a differential voltage between the + and − inputs greater than 5.0V. For example, in the figure below, the EL2071C is connected in a gain of +7 configuration and is disabled while the analog bus is driven externally to +5V. Pin 2 is consequently at +0.71V, and if V_{IN} is driven to −5V, then 5.71V appears between pins 3 and 2. Internally, this voltage appears across a forward biased V_{BE} in series with a reverse biased V_{BE} and is past the threshold for zenering the reverse biased V_{BE}. In a typical application, a 50Ω or 75Ω terminating resistor from pin 3 to ground will prevent pin 3 from approaching −5V.



2071-15

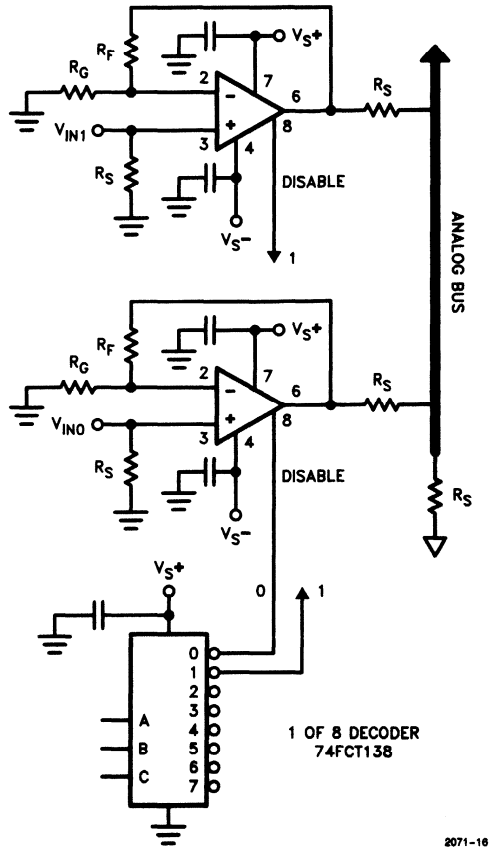
Applications Information — Contd.

Using the EL2071C as a Multiplexer

An interesting use of the enable feature is to combine several amplifiers in parallel with their outputs in common. This combination then acts similar to a MUX in front of an amplifier. A typical circuit is shown. The series resistance at each output helps to further increase isolation between amplifiers.

When the EL2071C is disabled, the DC output impedance is >100 kΩ in parallel with 2 pF capacitance.

To operate properly, the decoder that is used must have a $V_{OH} > (V_S+) - 0.4V$ with $I_{OH} = 750\ \mu A$, and should be connected to the same power supply as the EL2071C.



2071-16

EL2071C/EL2171C
150 MHz Current Feedback Amplifier

EL2071 Macromodel

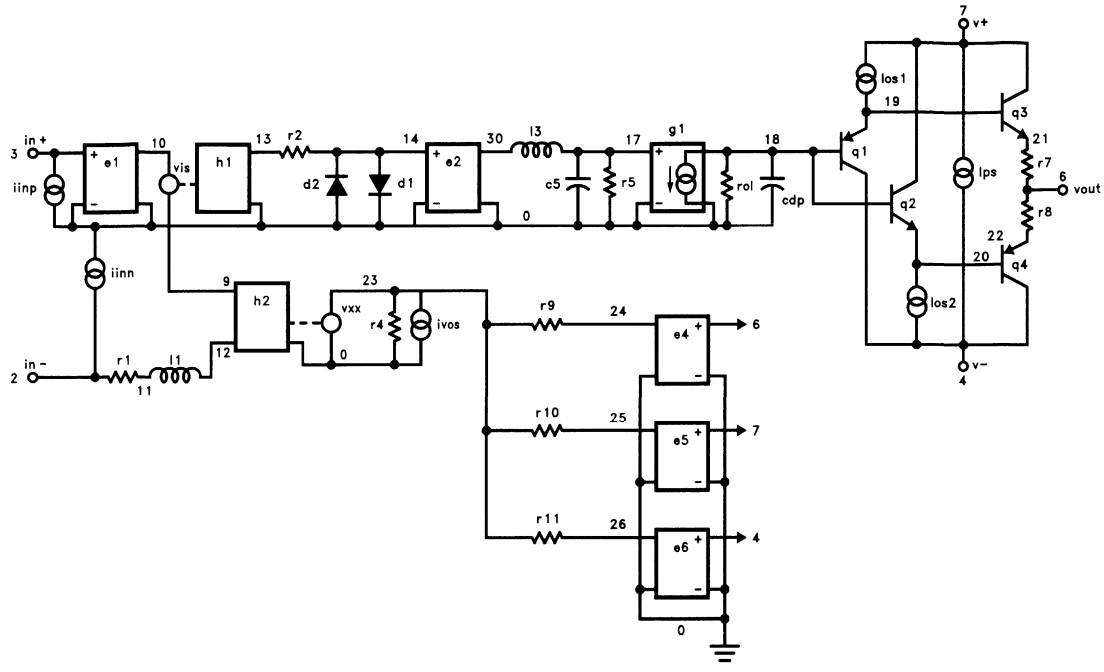
```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2071       3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 2
l1 11 12 1nH
iinp 3 0 10µA
iinm 2 0 10µA
*
* Slew Rate Limiting
*
*h1 13 0 vis 1K
h1 13 0 vis 600
r2 13 14 100
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
e2 30 0 14 0 0.001
13 30 17 1.0µH
c5 17 0 0.1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 1Meg
cdp 18 0 0.88pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 2
r8 22 6 2
```

EL2071 Macromodel — Contd.

```
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply Current
*
ips 7 4 9mA
*
* Error Terms
*
ivos 0 23 3mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 316
r10 25 23 562
r11 26 23 562
*
* Models
*
.model qn npn (is = 5e-15 bf = 500 tf = 0.05nS)
.model qp pnp (is = 5e-15 bf = 500 tf = 0.05nS)
.model dclamp d(is = 1e-30 ibv = 1pA bv = 3.5 n = 4)
.ends
```

EL2071C/EL2171C
150 MHz Current Feedback Amplifier

EL2071 Macromodel



2071-17

EL2073C

200 MHz Unity-Gain Stable Operational Amplifier

Features

- 200 MHz gain-bandwidth product
- Unity-gain stable
- Ultra low video distortion = 0.01%/0.015° @ NTSC/PAL
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%
- Low distortion = −60 dB HD2, −70 dB HD3 @ 20 MHz, 2 V_{PP}, A_V = +1

Applications

- High resolution video
- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2073CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2073CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

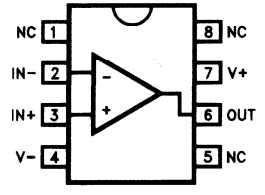
The EL2073 is a precision voltage-feedback amplifier featuring a 200 MHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2073 is unity-gain stable with a −3 dB bandwidth of 400 MHz. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2073 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2073 the ideal choice for all op-amp applications requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2073 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



2073-1

EL2073C

200 MHz Unity-Gain Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common-Mode Input	$\pm V_S$
Differential Input Voltage	5V
Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8
Operating Temperature	0°C to +75°C

Lead Temperature	
DIP Package	300°C
(Soldering: <5 seconds −CN <10 seconds −J)	
SO Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1.5	I	mV
			T_{MIN}, T_{MAX}			3	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)	All		8		V	µV/°C
I_B	Input Bias Current	V_{CM} = 0V	All		2	6	II	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	I	µA
			T_{MIN}, T_{MAX}			2	III	µA
PSRR	Power Supply Rejection Ratio	(Note 2)	All	60	80		II	dB
CMRR	Common Mode Rejection Ratio	(Note 3)	All	65	90		II	dB
I_S	Supply Current—Quiescent	No Load	25°C		21	23	I	mA
			T_{MIN}, T_{MAX}			25	III	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		V	kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		V	pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		V	MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		V	pF

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
R_{OUT}	Output Resistance		25°C		20		V	mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		IV	V
			T_{MIN}, T_{MAX}	±2.5			IV	V
I_{OUT}	Output Current		All	50	70		II	mA
V_{OUT}	Output Voltage Swing	No Load	All	±3.5	±4		II	V
V_{OUT} 100	Output Voltage Swing	100Ω	All	±3	±3.6		II	V
V_{OUT} 50	Output Voltage Swing	50Ω	All	±2.5	±3.4		II	V
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	500	1000		I	V/V
			T_{MIN}, T_{MAX}	400			III	V/V
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	400	800		I	V/V
			T_{MIN}, T_{MAX}	300			III	V/V
eN@ > 1 MHz	Noise Voltage 1–100 MHz		25°C		2.3		V	nV/√Hz
iN@ > 100 kHz	Noise Current 100k–100 MHz		25°C		3.2		V	pA/√Hz

Closed Loop AC Electrical Characteristics

V_S = ±5V, A_V = +1, Rf = 0Ω, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
SSBW	−3 dB Bandwidth (V_{OUT} = 0.4V_{PP})	A_V = +1	25°C	150	300		V	MHz
		A_V = −1	25°C		200		V	MHz
		A_V = +2	25°C	150	200		III	MHz
			T_{MIN}, T_{MAX}	125			IV	MHz
		A_V = +5	25°C		40		V	MHz
		A_V = +10	25°C		20		V	MHz
GBWP	Gain-Bandwidth Product	A_V = +10	25°C		200		V	MHz
LSBWa	−3 dB Bandwidth	V_{OUT} = 2 V_{PP} (Note 4)	All	50	85		IV	MHz
LSBWb	−3 dB Bandwidth	V_{OUT} = 5 V_{PP} (Note 4)	All	11	16		IV	MHz
GFPL	Peaking (<50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	0.5	III	dB
			T_{MIN}, T_{MAX}			0.5	IV	dB
GFPH	Peaking (>50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		1	3	III	dB
			T_{MIN}, T_{MAX}			3	IV	dB
GFR	Rolloff (<100 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0.1	0.5	III	dB
			T_{MIN}, T_{MAX}			0.5	IV	dB

EL2073C

200 MHz Unity-Gain Stable Operational Amplifier

Closed Loop AC Electrical Characteristics

$V_S = \pm 5V$, $A_V = +1$, Rf = 0Ω, R_L = 100Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
LPD	Linear Phase Deviation (<100 MHz)	V_{OUT} = 0.4 V_{PP}	All		1	1.8	IV	°
PM	Phase Margin	$A_V = +1$	25°C		60		V	°
tr1, tf1	Rise Time, Fall Time	0.4V Step, $A_V = +2$	25°C		2		V	ns
tr2, tf2	Rise Time, Fall Time	5V Step, $A_V = +2$	25°C		15		V	ns
ts1	Settling to 0.1% ($A_V = -1$)	2V Step	25°C		13		V	ns
ts2	Settling to 0.01% ($A_V = -1$)	2V Step	25°C		25		V	ns
OS	Overshoot	2V Step	25°C		5		V	%
SR	Slew Rate	2V Step	All	175	250		IV	V/μs
DISTORTION (Note 5)								
HD2a	2nd Harmonic Distortion	@ 10 MHz, $A_V = +2$	25°C		−65	−55	IV	dBc
HD2b	2nd Harmonic Distortion	@ 20 MHz, $A_V = +1$	25°C		−60	−50	IV	dBc
HD2c	2nd Harmonic Distortion	@ 20 MHz, $A_V = +2$	25°C		−55	−50	III	dBc
			T_{MIN}, T_{MAX}			−45	IV	dBc
HD3a	3rd Harmonic Distortion	@ 10 MHz, $A_V = +2$	25°C		−72	−60	IV	dBc
HD3b	3rd Harmonic Distortion	@ 20 MHz, $A_V = +1$	25°C		−70	−55	IV	dBc
HD3c	3rd Harmonic Distortion	@ 20 MHz, $A_V = +2$	25°C		−70	−60	III	dBc
			T_{MIN}, T_{MAX}			−60	IV	dBc
VIDEO PERFORMANCE (Note 6)								
dG	Differential Gain	NTSC	25°C		0.01	0.05	III	$\%_{pp}$
dP	Differential Phase	NTSC	25°C		0.015	0.05	III	$°_{pp}$
dG	Differential Gain	30 MHz	25°C		0.1		V	$\%_{pp}$
dP	Differential Phase	30 MHz	25°C		0.1		V	$°_{pp}$
VBW	±0.1 dB Bandwidth Flatness		25°C	25	50		III	MHz

Note 1: Measured from T_{MIN}, T_{MAX}.

Note 2: $\pm V_{CC} = \pm 4.5V$ to 5.5V.

Note 3: $\pm V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$

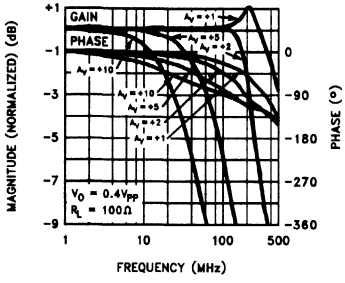
Note 4: Large-signal bandwidth calculated using $LSBW = \frac{\text{Slew Rate}}{2\pi\ V_{PEAK}}$.

Note 5: All distortion measurements are made with V_{OUT} = 2 V_{PP}, R_L = 100Ω.

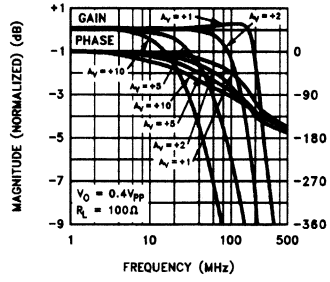
Note 6: Video performance measured at $A_V = +1$ with 2 times normal video level across R_L = 100Ω. This corresponds to standard video levels across a back-terminated 50Ω load, i.e., 0–100 IRE, 40IREpp giving a 1 V_{PP} video signal across the 50Ω load. For other values of R_L, see curves.

Typical Performance Curves (T_A = 25°C)

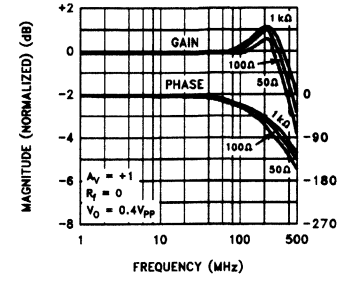
Non-Inverting Frequency Response



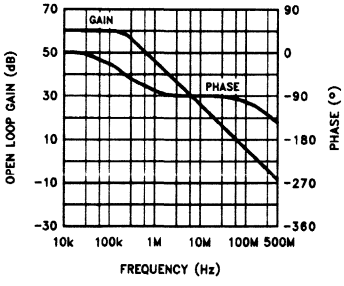
Inverting Frequency Response



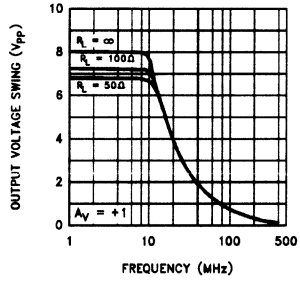
Frequency Response for Various R_Ls



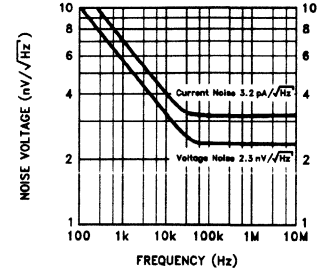
Open Loop Gain and Phase



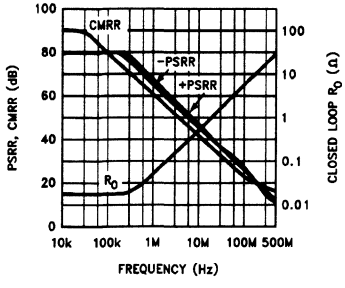
Output Voltage Swing vs Frequency



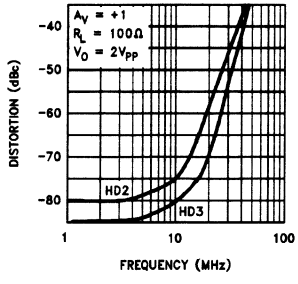
Equivalent Input Noise



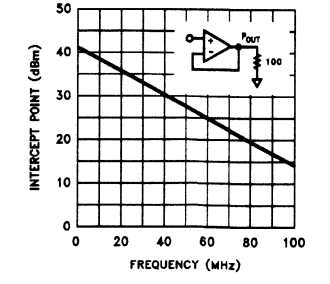
PSRR, CMRR, and Closed-Loop R_O vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency



2-Tone, 3rd Order Intermodulation Intercept

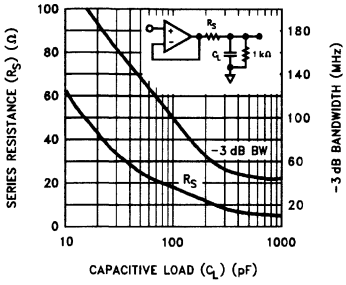


2073-2

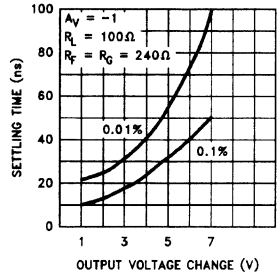
EL2073C
200 MHz Unity-Gain Stable Operational Amplifier

Typical Performance Curves (T_A = 25°C unless otherwise specified) — Contd.

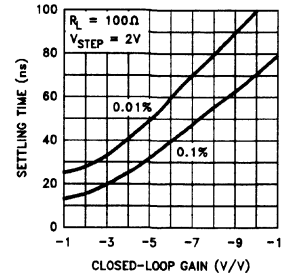
Series Resistor and Resulting Bandwidth vs Capacitive Load



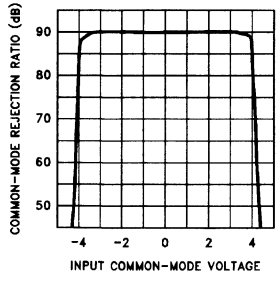
Settling Time vs Output Voltage Change



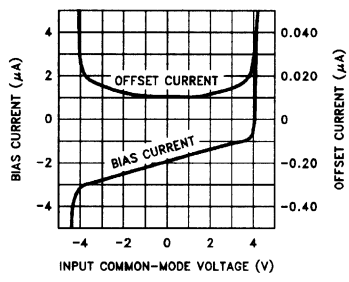
Settling Time vs Closed-Loop Gain



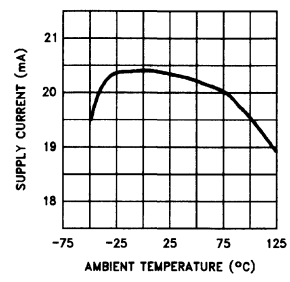
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



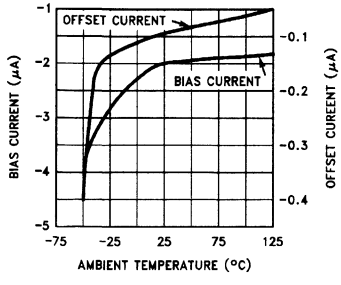
Bias and Offset Current vs Input Common-Mode Voltage



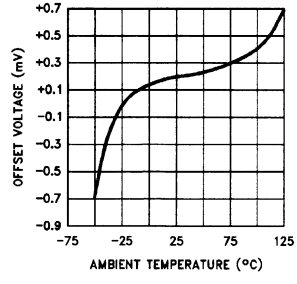
Supply Current vs Temperature



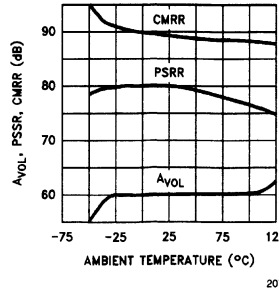
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature



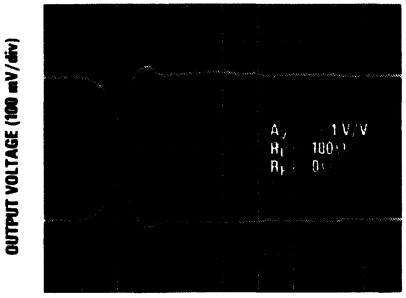
A_{VOL}, PSRR, and CMRR vs Temperature



2073-3

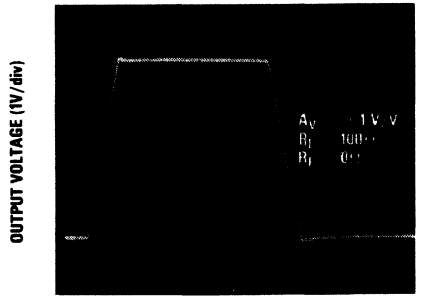
Typical Performance Curves (T_A = 25°C) — Contd.

Small Signal Transient Response



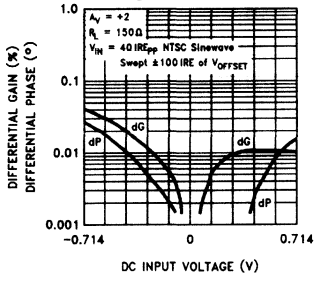
2072-4

Large Signal Transient Response

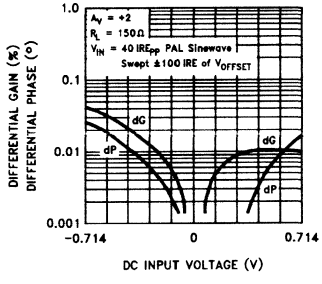


2072-5

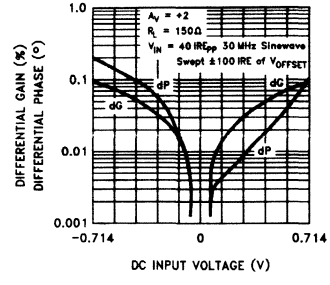
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



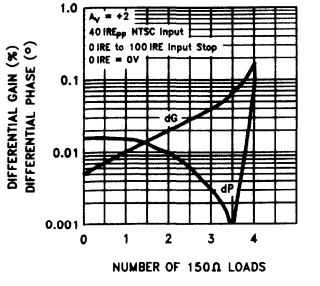
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



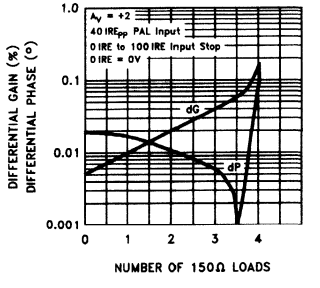
Differential Gain and Phase vs DC Input Offset at 30 MHz



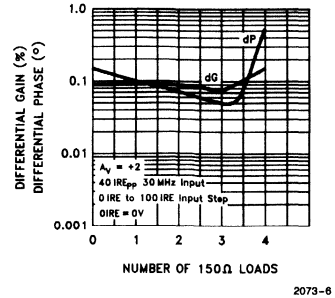
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



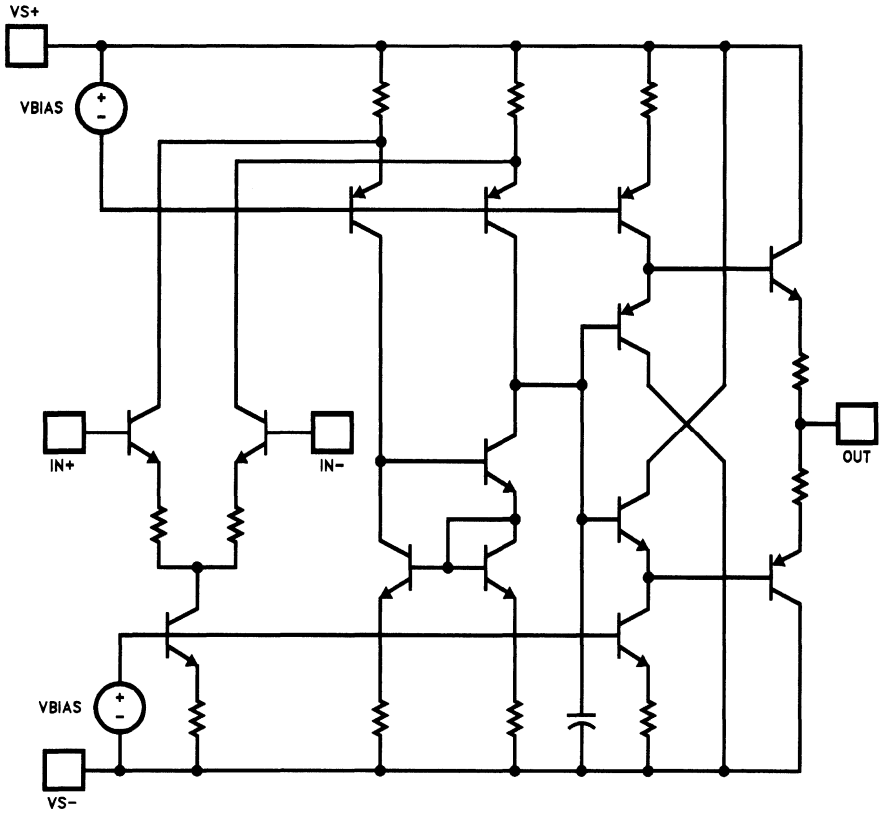
Differential Gain and Phase vs Number of 150Ω Loads at 30 MHz



2073-6

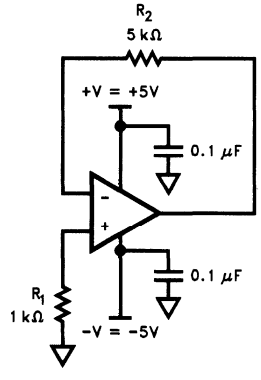
EL2073C
200 MHz Unity-Gain Stable Operational Amplifier

Equivalent Circuit



2073-7

Burn-In Circuit



2073-8

All Packages Use The Same Schematic

Applications Information

Product Description

The EL2073 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2073 uses a classical voltage-feedback topology which allows it to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2073 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2073 is an excellent choice for applications such as log amplifiers.

The EL2073 also has excellent DC specifications: 200 μV, V_{OS}, 2 μA I_B, 0.1 μA I_{OS}, and 90 dB of CMRR. These specifications allow the EL2073 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2073 is only 3.2 pA/$\sqrt{\text{Hz}}$, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2073 has a gain-bandwidth product of 200 MHz. For gains greater than 4, its closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2073 has a −3 dB bandwidth of 400 MHz at a gain of +1, dropping to 200 MHz at a gain of +2. It is important to note that the EL2073 has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2073 in a gain of +1 only exhibits 1 dB of peaking with a 100Ω load.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2073 is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC, 4.43 MHz for PAL, or 30 MHz for HDTV. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2073 has been designed to be among the best video amplifiers in the marketplace today. It has been thoroughly characterized for video performance in the topology described above, and the results have been included as minimum dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2073 exhibits dG and dP of only 0.01% and 0.015° at NTSC and PAL. Because dG and dP vary with different DC offsets, the superior video performance of the EL2073 has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The excellent output drive capability of the EL2073 allows it to drive up to 4 back-terminated loads with excellent video performance. With 4 150Ω loads, dG and dP are only 0.15% and 0.08° at NTSC and PAL. For more information, refer to the curves for Video Performance vs Number of 150Ω Loads.

Output Drive Capability

The EL2073 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 V_{PP} into a 50Ω load. This high output drive capability makes the EL2073 an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2073 remains a minimum of 50 mA at low temperatures. The EL2073 is current-limited at

Applications Information

the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2073 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without peaking.

Printed-Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 μF–10 μF tantalum capacitor is recommended in parallel with a 0.01 μF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2073 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2073 Macromodel

```
*
* Connections:                    +input
*                                 | -input
*                                 |  |  +Vsupply
*                                 |  |  |  -Vsupply
*                                 |  |  |  |  output
*                                 |  |  |  |  |
.subckt M2073                     3  2  7  4  6
*
*Input Stage
*
ie 37 4 1mA
r6 36 37 125
r7 38 37 125
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 1.2pF
rc 34 40 400
cc 40 0 0.3pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 0.5pF
rpb 42 43 50
cpb 43 0 0.5pF
*
* Output Stage
*
iosl 7 50 3.0mA
ios2 51 4 3.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
rosl 52 6 2
ros2 6 53 2
*
Power Supply Current
*
ips 7 4 11.4mA
*
Models
*
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.ends
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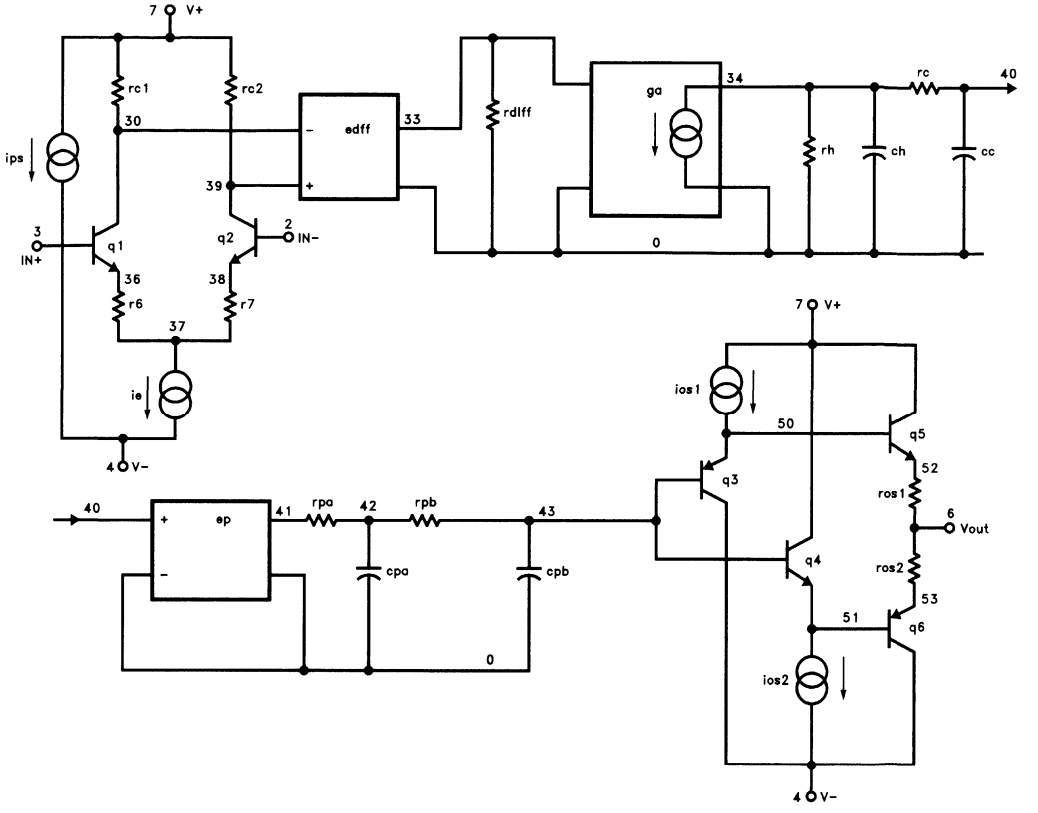
EL2073C
200 MHz Unity-Gain Stable Operational Amplifier

EL2073 Macromodel — Contd.



EL2074C

400 MHz GBWP Gain-of-2 Stable Operational Amplifier

Features

- 400 MHz gain-bandwidth product
- Gain-of-2 stable
- Ultra low video distortion = 0.01%/0.015° @ NTSC/PAL
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%
- Low distortion = −55 dB HD2, −70 dB HD3 @ 20 MHz, 2 Vpp, A_V = +2

Applications

- High resolution video
- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2074CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2074CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

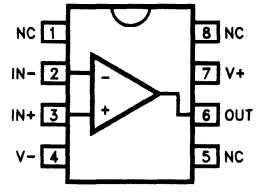
The EL2074 is a precision voltage-feedback amplifier featuring a 400 MHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2074 is gain-of-2 stable with a −3 dB bandwidth of 400 MHz at A_V = +2. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2074 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2074 the ideal choice for all op-amp applications at a noise gain of 2 or greater requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2074 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



2074-1

EL2074C

400 MHz GBWP Gain-of-2 Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common-Mode Input	$\pm V_S$
Differential Input Voltage	5V
Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8
Operating Temperature	0°C to +75°C

Lead Temperature	
DIP Package	300°C
(Soldering: <5 seconds −CN <10 seconds −J)	
SO Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1.5	I	mV
			T_{MIN}, T_{MAX}			3	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)	All		8		V	µV/°C
I_B	Input Bias Current	V_{CM} = 0V	All		2	6	II	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	I	µA
			T_{MIN}, T_{MAX}			2	III	µA
PSRR	Power Supply Rejection Ratio	(Note 2)	All	60	80		II	dB
CMRR	Common Mode Rejection Ratio	(Note 3)	All	65	90		II	dB
I_S	Supply Current—Quiescent	No Load	25°C		21	23	I	mA
			T_{MIN}, T_{MAX}			25	III	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		V	kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		V	pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		V	MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		V	pF

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
R_{OUT}	Output Resistance		25°C		20		V	mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		IV	V
			T_{MIN}, T_{MAX}	±2.5			IV	V
I_{OUT}	Output Current		All	50	70		II	mA
V_{OUT}	Output Voltage Swing	No Load	All	±3.5	±4		II	V
V_{OUT} 100	Output Voltage Swing	100Ω	All	±3	±3.6		II	V
V_{OUT} 50	Output Voltage Swing	50Ω	All	±2.5	±3.4		II	V
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	500	1000		I	V/V
			T_{MIN}, T_{MAX}	400			III	V/V
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	400	800		I	V/V
			T_{MIN}, T_{MAX}	300			III	V/V
eN@ > 1 MHz	Noise Voltage 1–100 MHz		25°C		2.3		V	nV/√Hz
iN@ > 100 kHz	Noise Current 100k–100 MHz		25°C		3.2		V	pA/√Hz

Closed Loop AC Electrical Characteristics

V_S = ±5V, A_V = +2, Rf = Rg = 250Ω, Cf = 3pF, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
SSBW	−3 dB Bandwidth (V_{OUT} = 0.4V_{PP})	A_V = −1	25°C		400		V	MHz
		A_V = +2	25°C	250	400		III	MHz
			T_{MIN}, T_{MAX}	250			IV	MHz
		A_V = +5	25°C		100		V	MHz
		A_V = +10	25°C		40		V	MHz
GBWP	Gain-Bandwidth Product	A_V = +10	25°C		400		V	MHz
LSBWa	−3 dB Bandwidth	V_{OUT} = 2 V_{PP} (Note 4)	All	43	63		IV	MHz
LSBWb	−3 dB Bandwidth	V_{OUT} = 5 V_{PP} (Note 4)	All	17	25		IV	MHz
GFPL	Peaking (<50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	1	III	dB
			T_{MIN}, T_{MAX}			1	IV	dB
GFPH	Peaking (>50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	2	III	dB
			T_{MIN}, T_{MAX}			2	IV	dB
GFR	Rolloff (<100 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0.1	0.5	III	dB
			T_{MIN}, T_{MAX}			0.5	IV	dB

EL2074C
400 MHz GBWP Gain-of-2 Stable Operational Amplifier

Closed Loop AC Electrical Characteristics

$V_S = \pm 5V$, $A_V = +2$, Rf = Rg = 250Ω, Cf = 3pF, R_L = 100Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
LPD	Linear Phase Deviation (<100 MHz)	V_{OUT} = 0.4 V_{PP}	All		1	1.8	IV	°
PM	Phase Margin	$A_V = +2$	25°C		50		V	°
tr1, tf1	Rise Time, Fall Time	0.4V Step, $A_V = +2$	25°C		1.8		V	ns
tr2, tf2	Rise Time, Fall Time	5V Step, $A_V = +2$	25°C		8		V	ns
ts1	Settling to 0.1% ($A_V = -1$)	2V Step	25°C		13		V	ns
ts2	Settling to 0.01% ($A_V = -1$)	2V Step	25°C		25		V	ns
OS	Overshoot	2V Step	25°C		5		V	%
SR	Slew Rate	2V Step	All	275	400		IV	V/μs
DISTORTION (Note 5)								
HD2a	2nd Harmonic Distortion	@ 10 MHz, $A_V = +2$	25°C		−65	−55	IV	dBc
HD2c	2nd Harmonic Distortion	@ 20 MHz, $A_V = +2$	25°C		−55	−45	III	dBc
			T_{MIN}, T_{MAX}			−45	IV	dBc
HD3a	3rd Harmonic Distortion	@ 10 MHz, $A_V = +2$	25°C		−72	−60	IV	dBc
HD3c	3rd Harmonic Distortion	@ 20 MHz, $A_V = +2$	25°C		−70	−60	III	dBc
			T_{MIN}, T_{MAX}			−60	IV	dBc
VIDEO PERFORMANCE (Note 6)								
dG	Differential Gain	NTSC	25°C		0.01	0.05	III	$\%_{pp}$
dP	Differential Phase	NTSC	25°C		0.015	0.05	III	$°_{pp}$
dG	Differential Gain	30 MHz	25°C		0.1		V	$\%_{pp}$
dP	Differential Phase	30 MHz	25°C		0.1		V	$°_{pp}$
VBW	±0.1 dB Bandwidth Flatness		25°C	25	50		III	MHz

Note 1: Measured from T_{MIN}, T_{MAX}.

Note 2: $\pm V_{CC} = \pm 4.5V$ to 5.5V.

Note 3: $\pm V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$

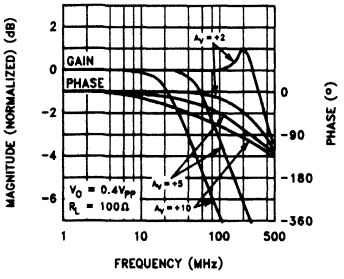
Note 4: Large-signal bandwidth calculated using $LSBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.

Note 5: All distortion measurements are made with $V_{OUT} = 2\ V_{PP}$, $R_L = 100\Omega$.

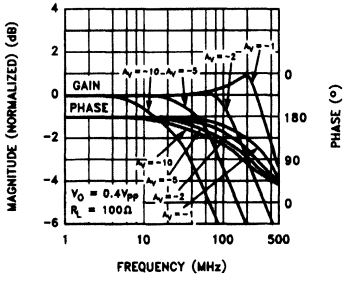
Note 6: Video performance measured at $A_V = +2$ with 2 times normal video level across $R_L = 100\Omega$. This corresponds to standard video levels across a back-terminated 50Ω load, i.e., 0–100 IRE, 40IREpp giving a 1 V_{PP} video signal across the 50Ω load. For other values of R_L, see curves.

Typical Performance Curves (T_A = 25°C)

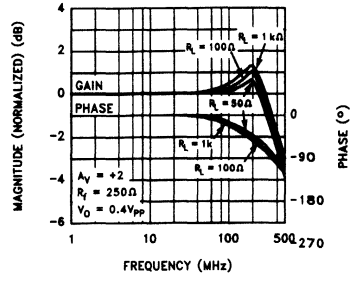
Non-Inverting Frequency Response



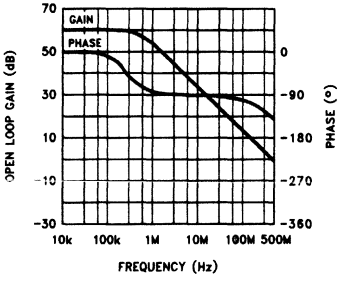
Inverting Frequency Response



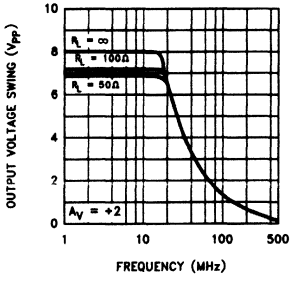
Frequency Response for Various R_Ls



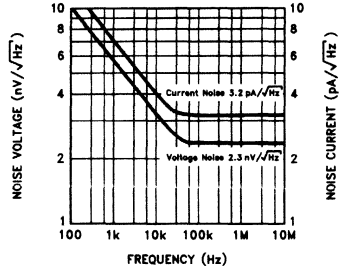
Open Loop Gain and Phase



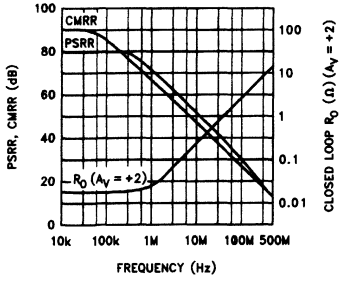
Output Voltage Swing vs Frequency



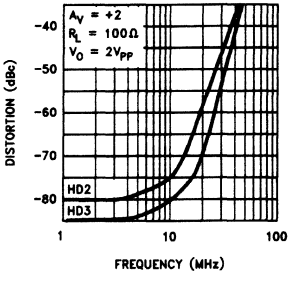
Equivalent Input Noise



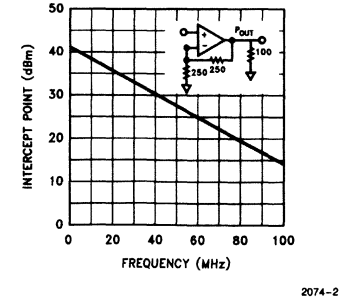
PSRR, CMRR, and Closed-Loop R_O vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency



2-Tone, 3rd Order Intermodulation Intercept

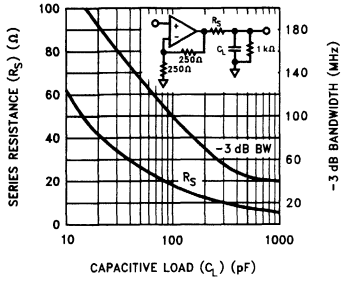


2074-2

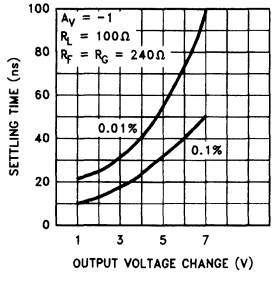
EL2074C
400 MHz GBWP Gain-of-2 Stable Operational Amplifier

Typical Performance Curves (T_A = 25°C unless otherwise specified) — Contd.

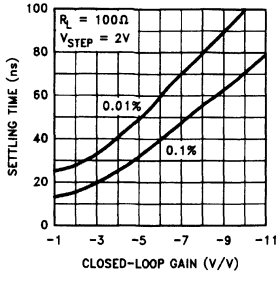
Series Resistor and Resulting Bandwidth vs Capacitive Load



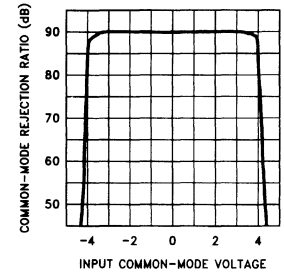
Settling Time vs Output Voltage Change



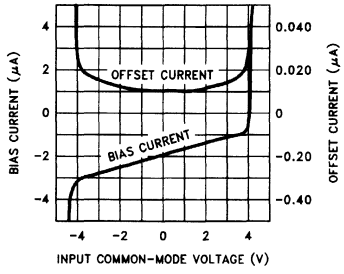
Settling Time vs Closed-Loop Gain



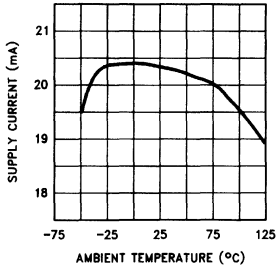
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



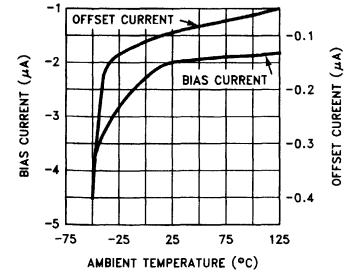
Bias and Offset Current vs Input Common-Mode Voltage



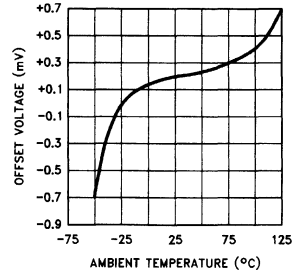
Supply Current vs Temperature



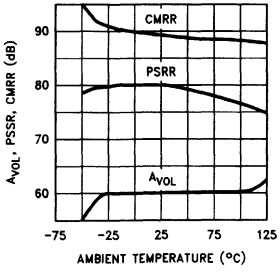
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature



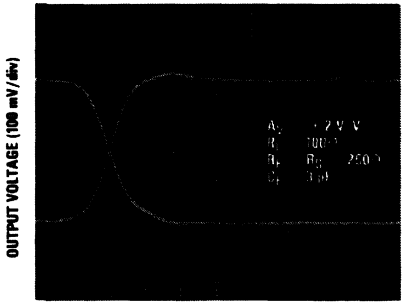
A_{VOL}, PSRR, and CMRR vs Temperature



2074-3

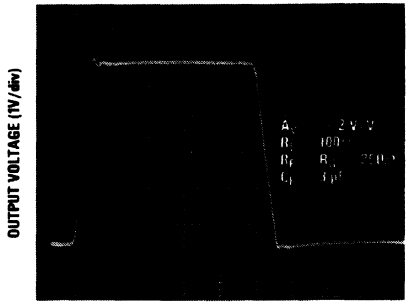
Typical Performance Curves (T_A = 25°C) — Contd.

Small Signal Transient Response



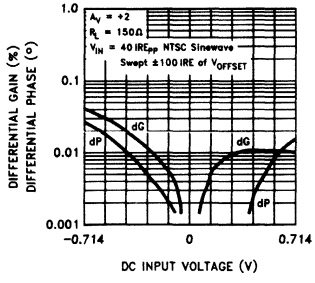
2074-4

Large Signal Transient Response

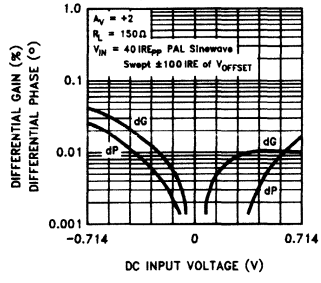


2074-5

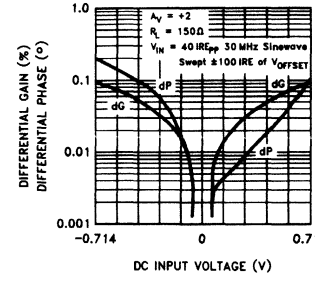
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



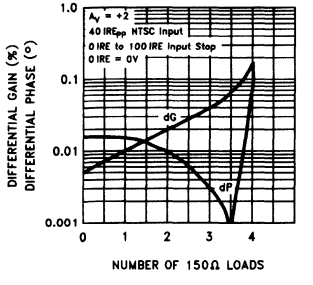
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



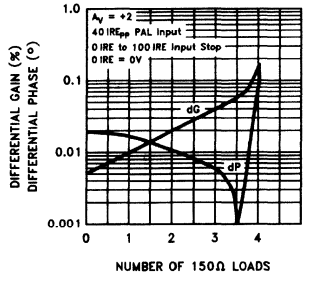
Differential Gain and Phase vs DC Input Offset at 30 MHz



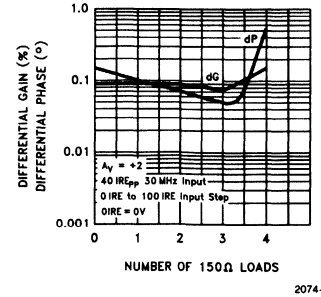
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



Differential Gain and Phase vs Number of 150Ω Loads at 30 MHz



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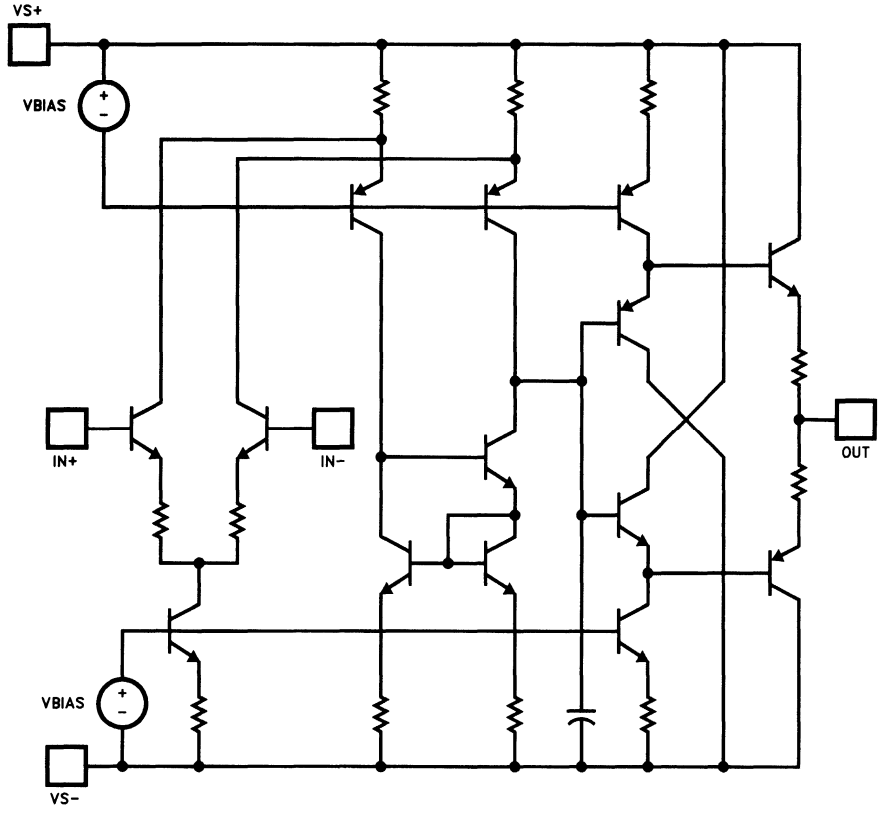
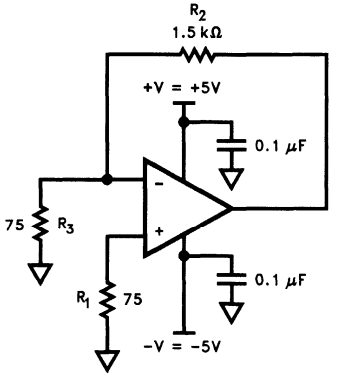
EL2074C
400 MHz GBWP Gain-of-2 Stable Operational Amplifier

Equivalent Circuit



2074-7

Burn-In Circuit



2074-8

All Packages Use The Same Schematic

Applications Information

Product Description

The EL2074 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2074 uses a classical voltage-feedback topology which allows it to be used in a variety of applications requiring a noise gain ≥ 2 where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2074 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2074 is an excellent choice for applications such as log amplifiers.

The EL2074 also has excellent DC specifications: 200 μV, V_{OS}, 2 μA I_B, 0.1 μA I_{OS}, and 90 dB of CMRR. These specifications allow the EL2074 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2074 is only 3.2 pA/$\sqrt{\text{Hz}}$, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2074 has a gain-bandwidth product of 400 MHz. For gains greater than 8, its closed-loop -3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 8, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2074 has a -3 dB bandwidth of 400 MHz at a gain of $+2$, dropping to 200 MHz at a gain of $+4$. It is important to note that the EL2074 has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2074 in a gain of $+2$ only exhibits 1 dB of peaking with a 100Ω load.

Parasitic Capacitances and Stability

When used in positive-gain configurations, the EL2074 can be quite sensitive to parasitic capacitances at the inverting input, especially with values $\geq 250\Omega$ for the gain resistor. The problem stems from the feedback and gain resistance in conjunction with the approximately 3pF of board-related parasitic capacitance from the inverting input to ground. Assuming a gain-of-2 configuration with $Rf = Rg = 250\Omega$, a feedback pole occurs at 424 MHz, which is equivalent to a zero in the forward path at the same frequency. This zero reduces stability by reducing the effective phase-margin from about 50° to about 30°.

A common solution to this problem is to add an additional capacitor from the inverting input to the output. This capacitor, in conjunction with the parasitic capacitance, maintains a constant voltage-divider between the output and the inverting input. This technique is used for AC testing of the EL2074. A 3pF capacitor is placed in parallel with the feedback resistor for all AC tests. When this capacitor is used, it is also possible to increase the resistance values of the feedback and gain resistors without loss of stability, resulting in less loading of the EL2074 from the feedback network.

Video Performance

An industry-standard method of measuring the video distortion of a component such as the EL2074 is to measure the amount of differential gain (dG) and differential phase (dP) that it introduces. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC, 4.43 MHz for PAL, or 30 MHz for HDTV. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

EL2074C
400 MHz GBWP Gain-of-2 Stable Operational Amplifier

Applications Information — Contd.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2074 has been designed to be among the best video amplifiers in the marketplace today. It has been thoroughly characterized for video performance in the topology described above, and the results have been included as minimum dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2074 exhibits dG and dP of only 0.01% and 0.015° at NTSC and PAL. Because dG and dP vary with different DC offsets, the superior video performance of the EL2074 has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

The excellent output drive capability of the EL2074 allows it to drive up to 4 back-terminated loads with excellent video performance. With 4 150Ω loads, dG and dP are only 0.15% and 0.08° at NTSC and PAL. For more information, refer to the curves for Video Performance vs Number of 150Ω Loads.

Output Drive Capability

The EL2074 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 V_{PP} into a 50Ω load. This high output drive capability makes the EL2074 an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2074 remains a minimum of 50 mA at low temperatures. The EL2074 is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2074 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without peaking.

Printed-Circuit Layout

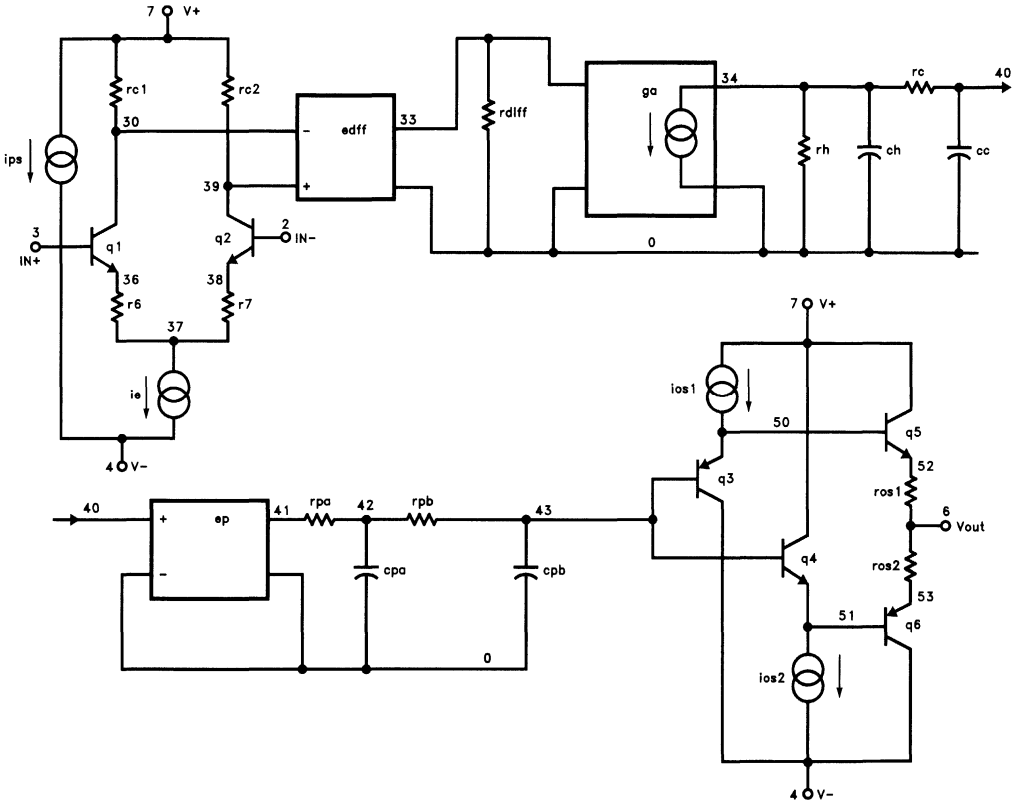
As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 μF–10 μF tantalum capacitor is recommended in parallel with a 0.01 μF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2074 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2074 Macromodel

```
*
* Connections:                    +input
*                                  | -input
*                                  |  |  +Vsupply
*                                  |  |  |  -Vsupply
*                                  |  |  |  |  output
*                                  |  |  |  |  |
.subckt M2074                      3  2  7  4  6
*
*Input Stage
*
ie 37 4 1 mA
r6 36 37 125
r7 38 37 125
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1 Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 0.8 pF
rc 34 40 50
cc 40 0 0.05 pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 150
cpa 42 0 0.5 pF
rpb 42 43 50
cpb 43 0 0.5 pF
*
* Output Stage
*
ios1 7 50 3.0 mA
ios2 51 4 3.0 mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
Power Supply Current
*
ips 7 4 11.4 mA
*
Models
*
.model qna npn(is=800e-18 bf=170 tf=0.2 ns)
.model qn  npn(is=810e-18 bf=200 tf=0.2 ns)
.model qp  pnp(is=800e-18 bf=200 tf=0.2 ns)
.ends
```

EL2074C
400 MHz GBWP Gain-of-2 Stable Operational Amplifier

EL2074 Macromodel — Contd.



EL2075C

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Features

- 2 GHz gain-bandwidth product
- Gain-of-10 stable
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%

Applications

- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2075CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2075CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

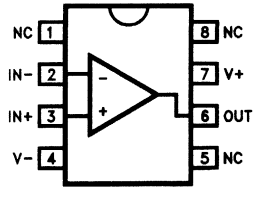
The EL2075 is a precision voltage-feedback amplifier featuring a 2 GHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2075 is gain-of-10 stable with a −3 dB bandwidth of 400 MHz at A_V = +10. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2075 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2075 the ideal choice for all op-amp applications at a gain of 10 or greater requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2075 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



2075-1

EL2075C
2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V	Lead Temperature	
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.	DIP Package (Soldering: <5 seconds −CN, <10 seconds −J)	300°C
		SO Package	
		Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
Common-Mode Input	$\pm V_S$	Junction Temperature	175°C
Differential Input Voltage	5V	Storage Temperature	−60°C to +150°C
Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO-8	Note: See EL2071/EL2171 for Thermal Impedance curves.	
Operating Temperature	0°C to +75°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075C	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1	I	mV
			T_{MIN}, T_{MAX}			2.5	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)	All		8		V	µV/°C
I_B	Input Bias Current	V_{CM} = 0V	All		2	6	II	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	I	µA
			T_{MIN}, T_{MAX}			2	III	µA
PSRR	Power Supply Rejection Ratio	(Note 2)	All	70	90		II	dB
CMRR	Common Mode Rejection Ratio	(Note 3)	All	70	90		II	dB
I_S	Supply Current—Quiescent	No Load	25°C		21	23	I	mA
			T_{MIN}, T_{MAX}			25	III	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		V	kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		V	pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		V	MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		V	pF

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075C	Units
R_{OUT}	Output Resistance		25°C		50		V	mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		IV	V
			T_{MIN}, T_{MAX}	±2.5			IV	V
I_{OUT}	Output Current		All	50	70		II	mA
V_{OUT}	Output Voltage Swing	No Load	All	±3.5	±4		II	V
V_{OUT} 100	Output Voltage Swing	100Ω	All	±3	±3.6		II	V
V_{OUT} 50	Output Voltage Swing	50Ω	All	±2.5	±3.4		II	V
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	1000	2800		I	V/V
			T_{MIN}, T_{MAX}	800			III	V/V
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	800	2300		I	V/V
			T_{MIN}, T_{MAX}	600			III	V/V
eN@ > 1 MHz	Noise Voltage 1–100 MHz		25°C		2.3		V	nV/√Hz
iN@ > 100 kHz	Noise Current 100k–100 MHz		25°C		3.2		V	pA/√Hz

Closed Loop AC Electrical Characteristics

V_S = ±5V, A_V = +20, Rf = 1500Ω, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075C	Units
SSBW	−3 dB Bandwidth (V_{OUT} = 0.4V_{PP})	A_V = +10	25°C		400		V	MHz
		A_V = +20	25°C	150	200		III	MHz
			T_{MIN}, T_{MAX}	125			IV	MHz
		A_V = +50	25°C		40		V	MHz
GBWP	Gain-Bandwidth Product	A_V = +100	25°C		2.0		V	GHz
LSBWa	−3 dB Bandwidth	V_{OUT} = 2 V_{PP} (Note 4)	All	80	128		IV	MHz
LSBWb	−3 dB Bandwidth	V_{OUT} = 5 V_{PP} (Note 4)	All	32	50		IV	MHz
GFPL	Peaking (<50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	0.5	III	dB
			T_{MIN}, T_{MAX}			0.5	IV	dB
GFPH	Peaking (>50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	1	III	dB
			T_{MIN}, T_{MAX}			1	IV	dB
GFR	Rolloff (<100 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0.1	0.5	III	dB
			T_{MIN}, T_{MAX}			0.5	IV	dB

EL2075C
2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Closed Loop AC Electrical Characteristics

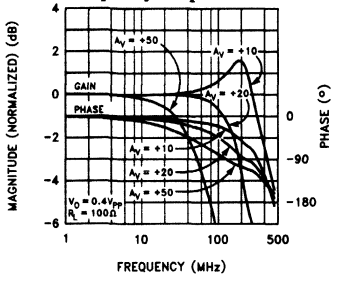
$V_S = \pm 5V$, $A_V = +20$, Rf = 1500Ω, R_L = 100Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075C	Units
LPD	Linear Phase Deviation (<100 MHz)	V_{OUT} = 0.4 V_{PP}	All		1	1.8	IV	°
PM	Phase Margin	$A_V = +10$	25°C		60		V	°
tr1, tf1	Rise Time, Fall Time	0.4V Step, $A_V = +10$	25°C		1.2		V	ns
tr2, tf2	Rise Time, Fall Time	5V Step, $A_V = +10$	25°C		6		V	ns
ts1	Settling to 0.1% ($A_V = -20$)	2V Step	25°C		13		V	ns
ts2	Settling to 0.01% ($A_V = -20$)	2V Step	25°C		25		V	ns
OS	Overshoot	2V Step, $A_V = +10$	25°C		10		V	%
SR	Slew Rate	2V Step, $A_V = +10$	All	500	800		IV	V/µs
DISTORTION (Note 5)								
HD2	2nd Harmonic Distortion	@ 20 MHz, $A_V = +20$	25°C		−40	−30	III	dBc
			T_{MIN}, T_{MAX}			−30	IV	dBc
HD3	3rd Harmonic Distortion	@ 20 MHz, $A_V = +20$	25°C		−65	−50	III	dBc
			T_{MIN}, T_{MAX}			−50	IV	dBc

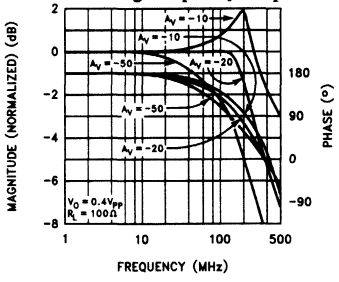
Note 1: Measured from T_{MIN}, T_{MAX}.
Note 2: $\pm V_{CC} = \pm 4.5V$ to 5.5V.
Note 3: $\pm V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$
Note 4: Large-signal bandwidth calculated using $LSBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
Note 5: All distortion measurements are made with V_{OUT} = 2 V_{PP}, R_L = 100Ω.

Typical Performance Curves (T_A = 25°C)

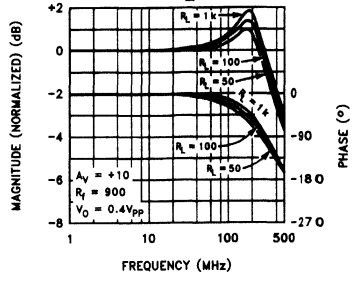
Non-Inverting Frequency Response



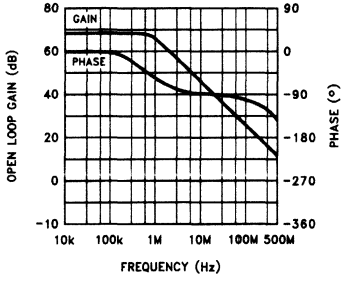
Inverting Frequency Response



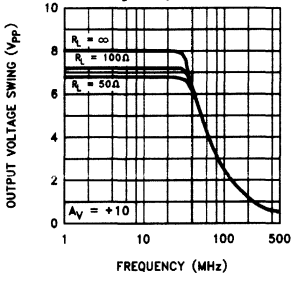
Frequency Response for Various R_Ls



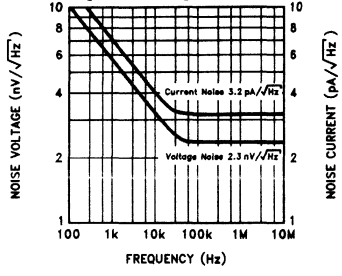
Open Loop Gain and Phase



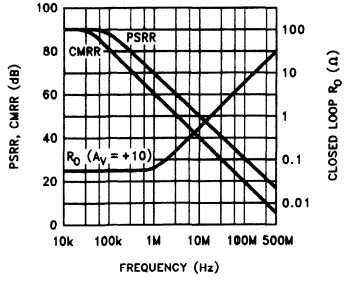
Output Voltage Swing vs Frequency



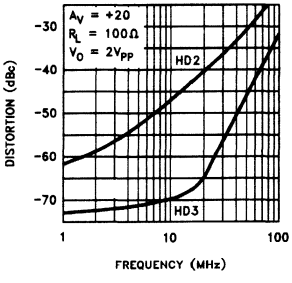
Equivalent Input Noise



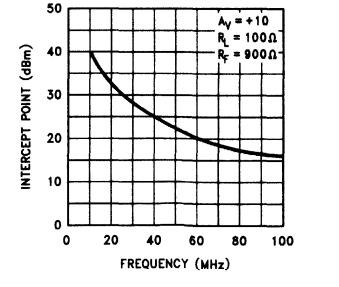
PSRR, CMRR, and Closed-Loop R_O Frequency



2nd and 3rd Harmonic Distortion vs Frequency



2-Tone, 3rd Order Intermodulation Intercept

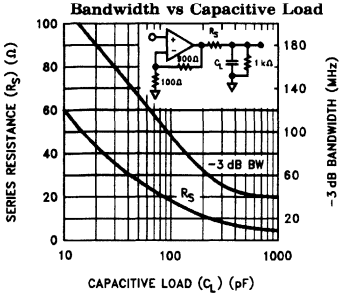


2075-2

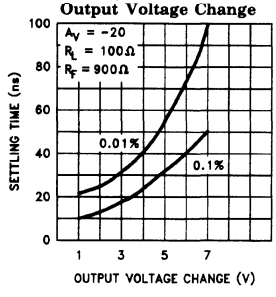
EL2075C
2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Typical Performance Curves (T_A = 25°C unless otherwise specified) — Contd.

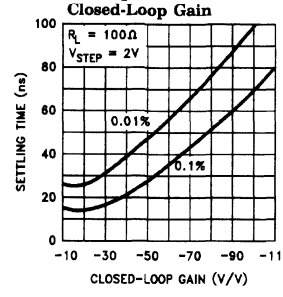
Series Resistor and Resulting Bandwidth vs Capacitive Load



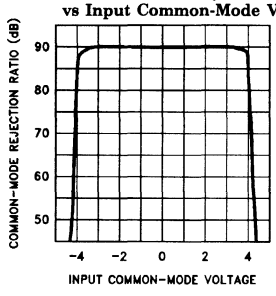
Settling Time vs Output Voltage Change



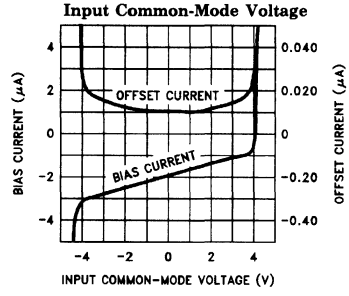
Settling Time vs Closed-Loop Gain



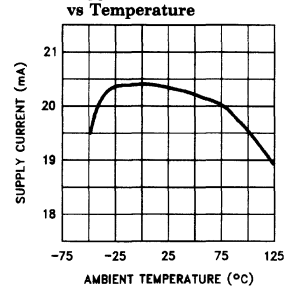
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



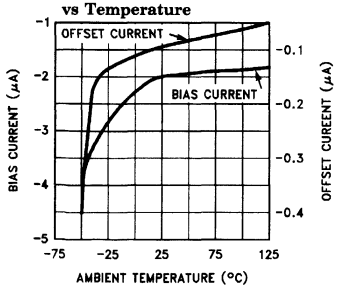
Bias and Offset Current vs Input Common-Mode Voltage



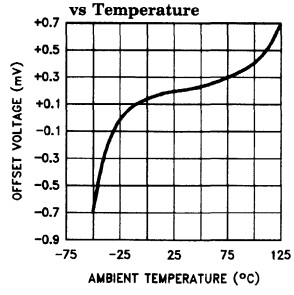
Supply Current vs Temperature



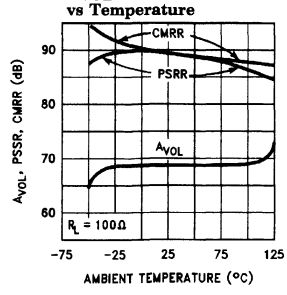
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature



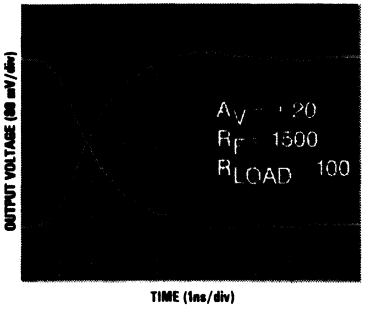
A_{VOL}, PSRR, and CMRR vs Temperature



2075-3

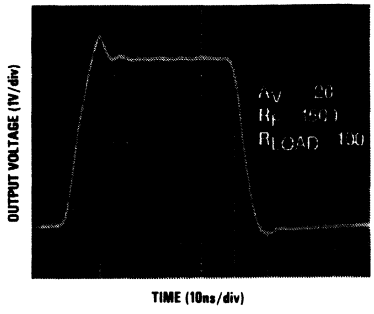
Typical Performance Curves (T_A = 25°C) — Contd.

Small Signal Transient Response



2075-4

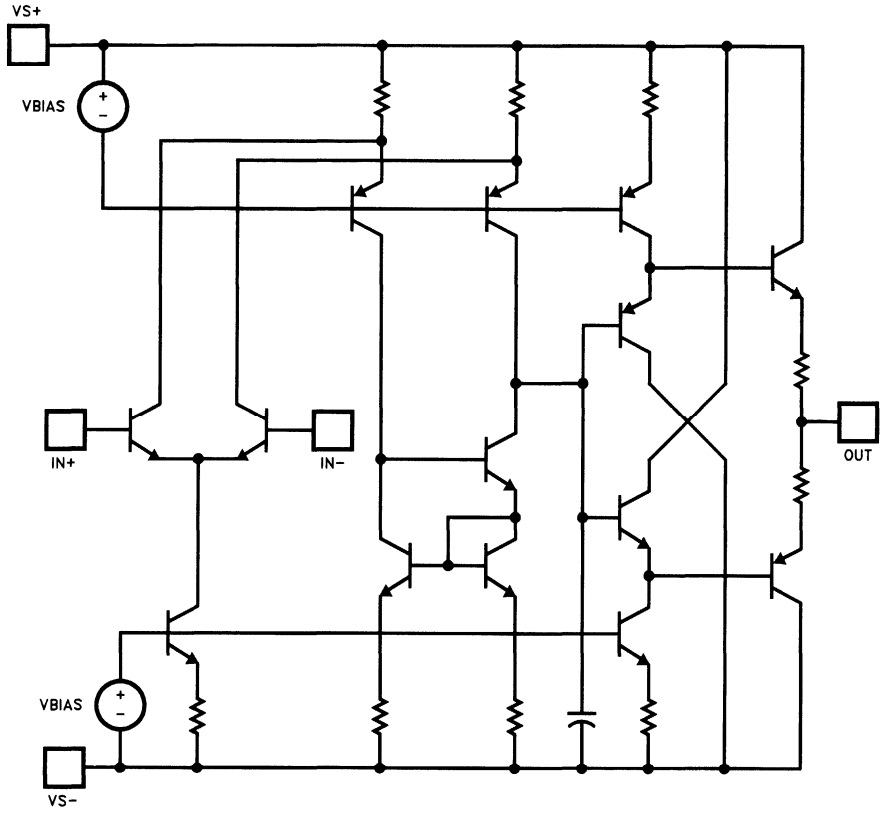
Large Signal Transient Response



2075-5

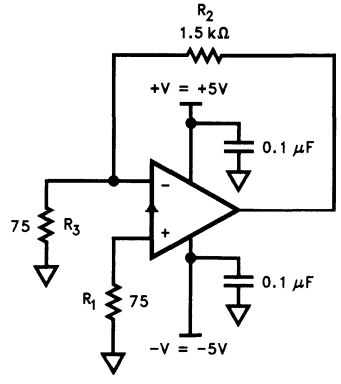
EL2075C
2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Equivalent Circuit



2075-6

Burn-In Circuit



2075-7

All Packages Use The Same Schematic

Applications Information

Product Description

The EL2075 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2075 uses a classical voltage-feedback topology which allows it to be used in a variety of applications requiring a noise gain $\geq$ 10 where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2075 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2075 is an excellent choice for applications such as log amplifiers.

The EL2075 also has excellent DC specifications: 200 μV, V_{OS}, 2 μA I_B, 0.1 μA I_{OS}, and 90 dB of CMRR. These specifications allow the EL2075 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2075 is only 3.2 pA/$\sqrt{\text{Hz}}$, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2075 has a gain-bandwidth product of 2 GHz. For gains greater than 40, its closed-loop -3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 40, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2075 has a -3 dB bandwidth of 400 MHz at a gain of $+10$, dropping to 200 MHz at a gain of $+20$. It is important to note that the EL2075 has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2075 in a gain of $+10$ only exhibits 1.5 dB of peaking with a 100Ω load.

Output Drive Capability

The EL2075 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 V_{PP} into a 50Ω load. This high output drive capability makes the EL2075 an ideal choice for RF and IF applications. Furthermore, the current drive of the EL2075 remains a minimum of 50 mA at low temperatures. The EL2075 is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2075 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without additionl peaking.

Printed-Circuit Layout

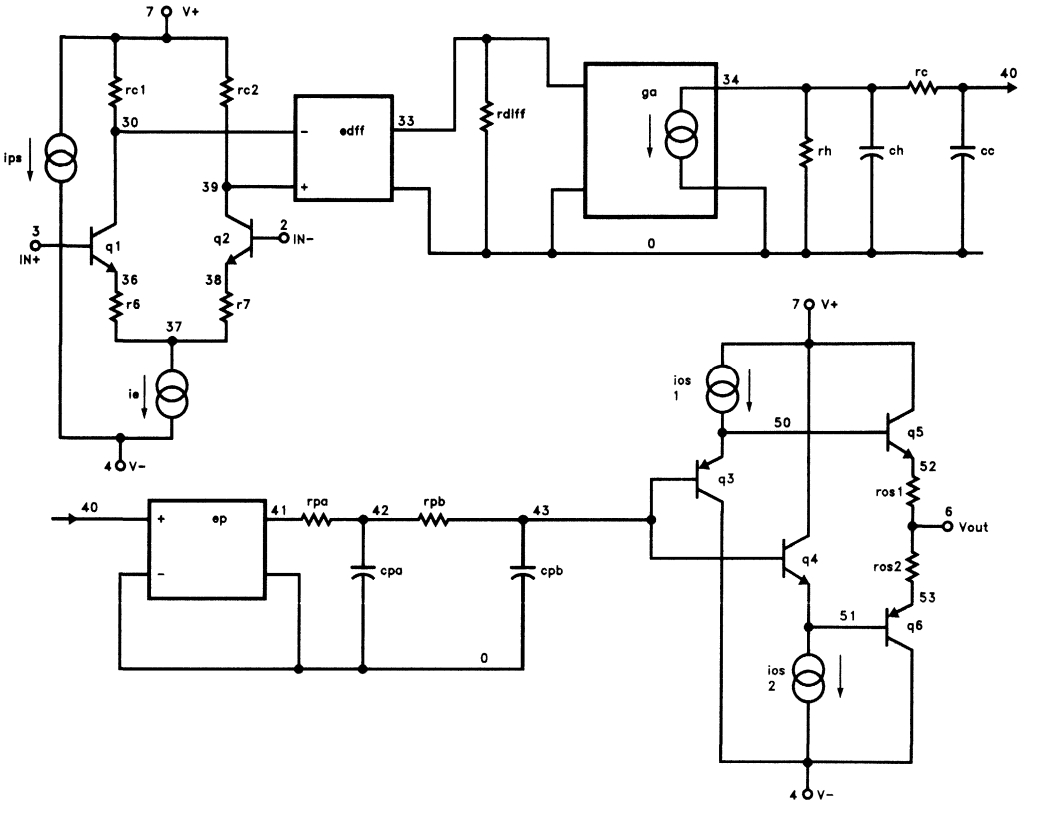
As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 μF–10 μF tantalum capacitor is recommended in parallel with a 0.01 μF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2075 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2075C
2 GHz GBWP Gain-of-10 Stable Operational Amplifier

EL2075 Macromodel

```
*
* Connections:                    +input
*                                 | -input
*                                 |  |  +Vsupply
*                                 |  |  |  -Vsupply
*                                 |  |  |  |  output
*                                 |  |  |  |  |
.subckt M2075                     3  2  7  4  6
*
*Input Stage
*
ie 37 4 1 mA
r6 36 37 15
r7 38 37 15
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1 Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 0.4 pF
rc 34 40 50
cc 40 0 0.05 pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 250
cpa 42 0 0.8 pF
rpb 42 43 50
cpb 43 0 0.5 pF
*
* Output Stage
*
ios1 7 50 3.0 mA
ios2 51 4 3.0 mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
* Power Supply Current
*
ips 7 4 11.4 mA
*
* Models
*
.model qna npn(is=800e-18 bf=170 tf=0.2 ns)
.model qn  npn(is=810e-18 bf=200 tf=0.2 ns)
.model qp  pnp(is=800e-18 bf=200 tf=0.2 ns)
.ends
```

EL2075 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2120C
100 MHz Current Feedback Amplifier

Features

- Excellent differential gain and phase on ±5V to ±15V supplies
- 100 MHz −3 dB bandwidth from gains of ±1 to ±10
- 700 V/μs slew rate
- 0.1 dB flatness to 20 MHz
- Output disable in 50 ns - remains high impedance even when driven with large slew rates
- Single +5V supply operation
- AC characteristics are lot and temperature stable
- Available in small SO-8 package

Applications

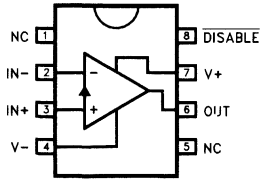
- Video gain block
- Residue amplifier
- Multiplexer
- Current to voltage converter
- Coax cable driver with gain of 2
- ADC driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2120CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2120CS	0°C to +75°C	8-Lead SO	MDP0027

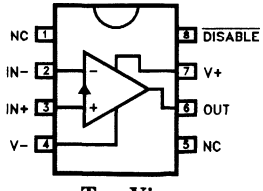
Connection Diagrams

P-DIP



2120-1

SO



2120-2

Top View

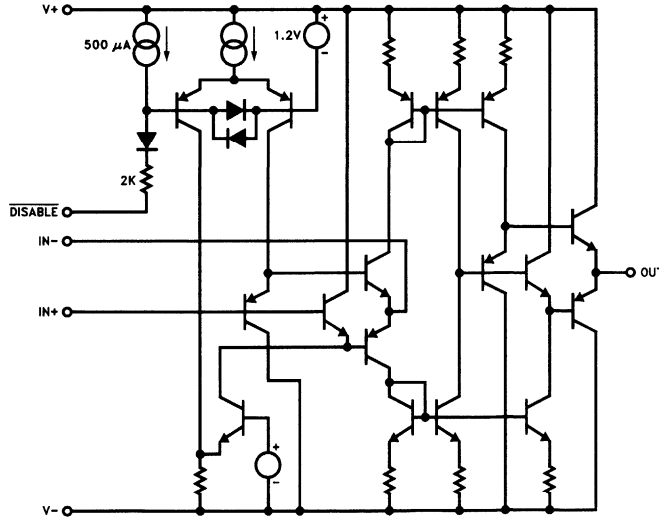
General Description

The EL2120C is a wideband current feedback amplifier optimized for video performance. Its 0.01% differential gain and 0.03 degree differential phase performance when at ±5V supplies exceeds the performance of other amplifiers running on ±15V supplies. Operating on ±8 to ±15V supplies reduces distortions to 0.01% and 0.01 degrees and below. The EL2120C can operate with supplies as low as ±2.5V or a single +5V supply.

Being a current feedback design, bandwidth is a relatively constant 100 MHz over the ±1 to ±10 gain range. The EL2120C has been optimized for flat gain over frequency and all characteristics are maintained at positive unity gain. Because the input slew rate is similar to the 700 V/μs output slew rate the part makes an excellent high-speed buffer.

The EL2120C has a superior output disable function. Time to enable or disable is 50 ns and does not change markedly with temperature. Furthermore, in disable mode the output does not draw excessive currents when driven with 1000 V/μs slew rates. The output appears as a 3 pF load when disabled.

Simplified Schematic



2120-21

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	33V	Operating Ambient Temperature Range	0° to 75°C
Voltage at +IN, −IN, V_{OUT}	(V−) − 0.5V to (V+) + 0.5V	Operating Junction Temperature P-DIP or SO	150°C
Voltage between +IN and − IN	±5V	Storage Temperature Range	−65°C to + 150°C
Voltage at /Disable	(V+) − 10V to (V+) + 0.5V	Lead Temperature P-DIP Package (Soldering, <10 Seconds)	300°C
Current into +IN, −IN, and /Disable	±5 mA	SO Package (Vapor Phase, <60 Seconds)	215°C
Output Current	±50 mA	(Infrared, <15 Seconds)	220°C
Internal Power Dissipation	See Curves		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V; R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage V_S = ±15V	Full Full		4 2	20 25	II II	mV mV
$\Delta V_{OS}/\Delta T$	Input Offset Drift	Full		20		V	µV/°C
I_{B+}	+V_{IN} Input Bias Current	Full		5	15	II	µA
I_{B-}	−V_{IN} Input Bias Current	Full		10	40	II	µA
CMRR	Common-Mode Rejection (Note 1)	Full	50	55		II	dB
−ICMR	−Input Current Common-Mode Rejection (Note 1)	Full		8	20	II	µA/V
PSRR	Power Supply Rejection (Note 2)	Full	65	80		II	dB
+IPSR	+Input Current Power Supply Rejection (Note 2)	25°C		0.03		V	µA/V
−IPSR	−Input Current Power Supply Rejection (Note 2)	Full		0.6	5	II	µA/V
R_{OL}	Transimpedance	Full	70	140		II	kΩ
A_{VOL}	Voltage Gain	Full	58	66		II	dB
+R_{IN}	+V_{IN} Input Impedance	25°C		2		V	MΩ

EL2120C
100 MHz Current Feedback Amplifier

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 5V$; $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{IN}	$+V_{IN}$ Range	Full	±3.0	±3.5		II	V
V_O	Output Voltage Swing	Full	±3.0	±3.5		II	V
I_{SC}	Output Short-Circuit Current	25°C		100		II	mA
$I_{O,DIS}$	Output Current, Disabled	Full		5	50	II	μA
$V_{DIS,ON}$	Disable Pin Voltage for Output Enabled	Full	(V+) − 1			II	V
$V_{DIS,OFF}$	Disable Pin Voltage for Output Disabled	Full			(V+) − 4	II	V
$I_{DIS,ON}$	Disable Pin Current for Output Enabled	Full			5	II	μA
$I_{DIS,OFF}$	Disable Pin Current for Output Disabled	Full	1.0			II	mA
I_S	Supply Current ($V_S = \pm 15V$)	Full		17	20	II	mA

Note 1: The input is moved from −3V to +3V.
Note 2: The supplies are moved from ±5V to ±15V.

Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$; $A_V = +2$ ($R_F = R_G = 270\Omega$); $R_L = 150\Omega$; $C_L = 7$ pF; $C_{IN-} = 2$ pF; $T_A = 25°C$

Parameter	Description		Min	Typ	Max	Test Level	Units
SR	Slew Rate; V_{OUT} from −3V to +3V Measured at −2V and +2V						
		$V_S = \pm 15V$		750		V	V/μs
		$V_S = \pm 5V$		550		V	V/μs
t_S	Settling Time to 0.25% of a 0 to +10V Swing; $A_V = +1$ with $R_F = 270\Omega$, $R_G = \infty$, and $R_L = 400\Omega$			50		V	ns
BW	Bandwidth	−3 dB		95		V	MHz
		±1 dB		50		V	MHz
		±0.1 dB		16		V	MHz
BW@2.5V	Bandwidth at $V_S = \pm 2.5V$	−3 dB		75		V	MHz
		±1 dB		35		V	MHz
		±0.1 dB		11		V	MHz
Peaking				0.5		V	dB

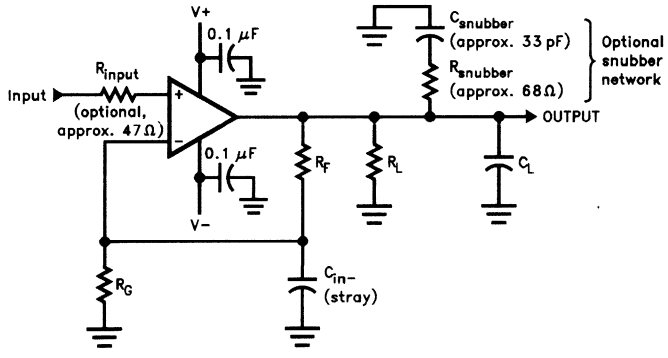
Closed Loop AC Electrical Characteristics — Contd.

$V_S = \pm 15V$; $A_V = +2$ ($R_F = R_G = 270\Omega$); $R_L = 150\Omega$; $C_L = 7$ pF; $C_{IN-} = 2$ pF; $T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
dG	Differential Gain; DC Offset from −0.7V through +0.7V, AC Amplitude 286 mVp-p					
	$V_S = \pm 15V$, f = 3.58 MHz		<0.01		V	%
	$V_S = \pm 15V$, f = 30 MHz		0.1		V	%
	$V_S = \pm 5V$, f = 3.58 MHz		0.01		V	%
dθ	Differential Phase; DC Offset from −0.7V through +0.7V, AC Amplitude 286 mVp-p					
	$V_S = \pm 15V$, f = 3.58 MHz		0.01		V	°
	$V_S = \pm 15V$, f = 30 MHz		0.1		V	°
	$V_S = \pm 5V$, f = 3.58 MHz		0.06		V	°

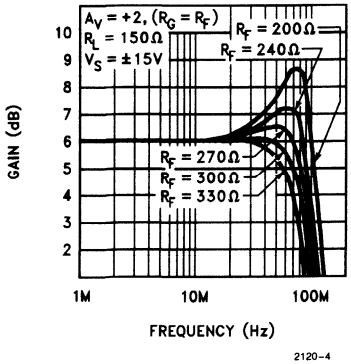
Typical Performance Curves

AC Test Circuit



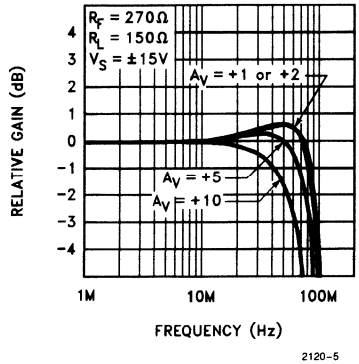
2120-3

Frequency Response vs R_F



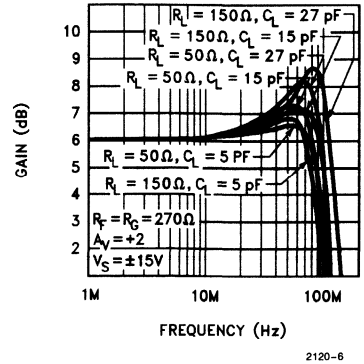
2120-4

Frequency Response vs Gain



2120-5

Frequency Response vs Load

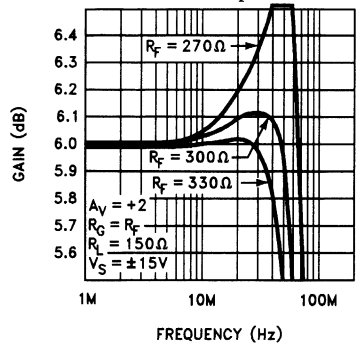


2120-6

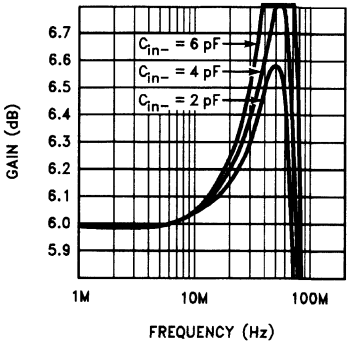
EL2120C
100 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

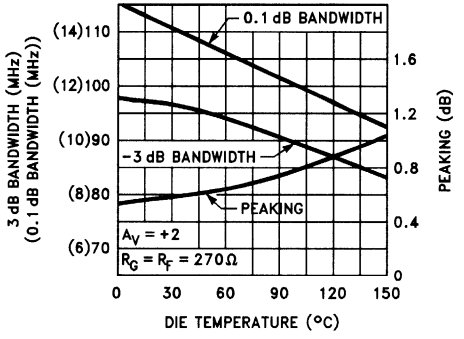
Gain Flatness vs R_F



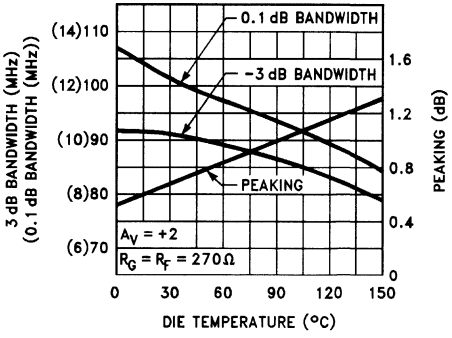
Gain Flatness vs C_{IN-}



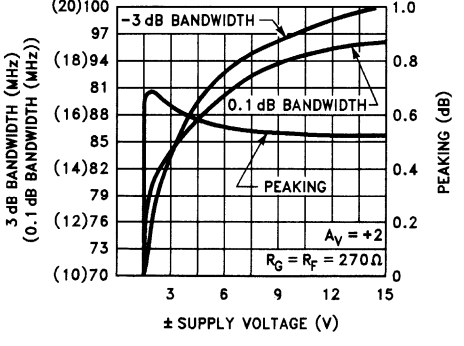
−3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Temperature at V_S ±15V



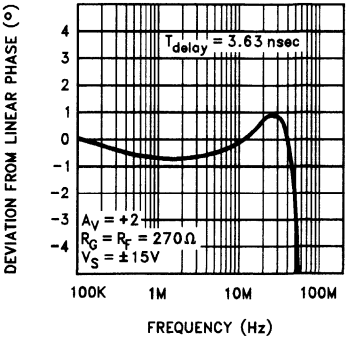
−3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Temperature at V_S ±5V



−3 dB Bandwidth, 0.1 dB Bandwidth, and Peaking vs Supply Voltage



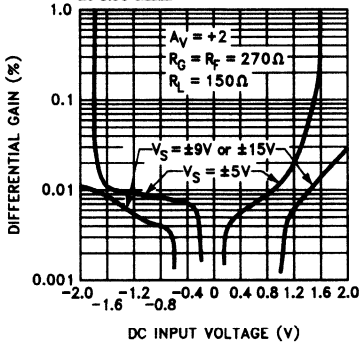
Deviation From Linear Phase vs Frequency



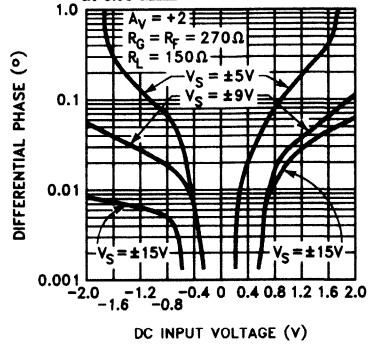
2120-7

Typical Performance Curves — Contd.

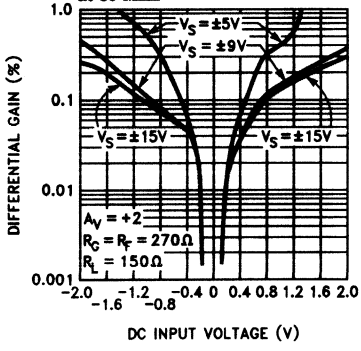
Differential Gain vs DC Input Offset at 3.58 MHz



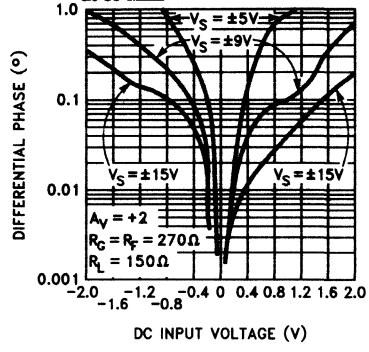
Differential Phase vs DC Input Offset at 3.58 MHz



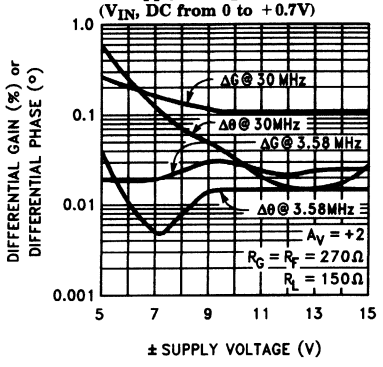
Differential Gain vs DC Input Offset at 30 MHz



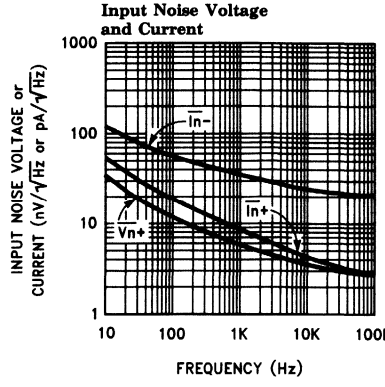
Differential Phase vs DC Input Offset at 30 MHz



Differential Gain and Phase vs Supply Voltage (V_{IN}, DC from 0 to +0.7V)



Input Noise Voltage and Current

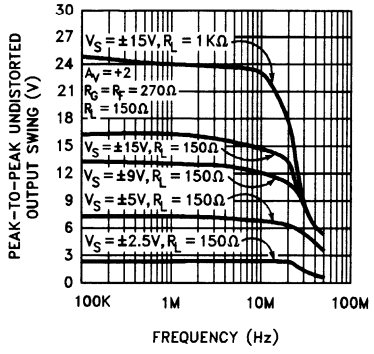


2120-8

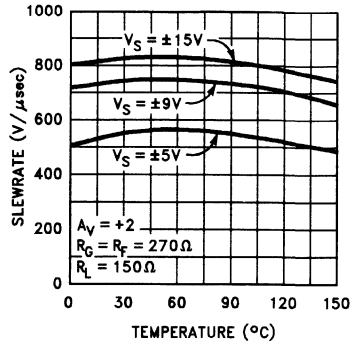
EL2120C
100 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

Undistorted Output Swing vs Frequency

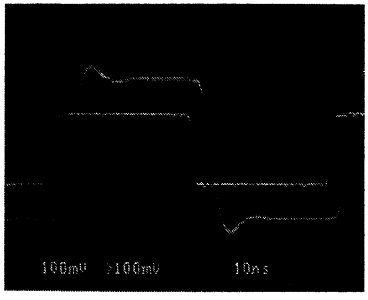


Slew Rate vs Temperature



2120-9

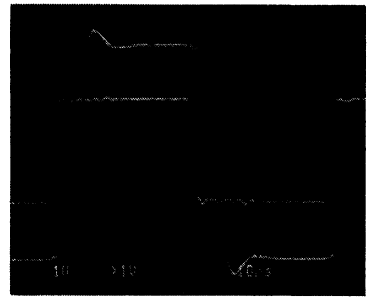
Small-Signal Transient Response



$A_V = +2$, $R_F = R_G = 270\Omega$, $R_L = 150\Omega$

2120-10

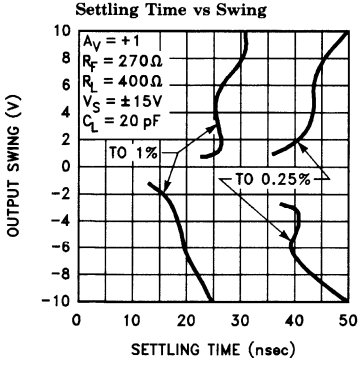
Large-Signal Transient Response



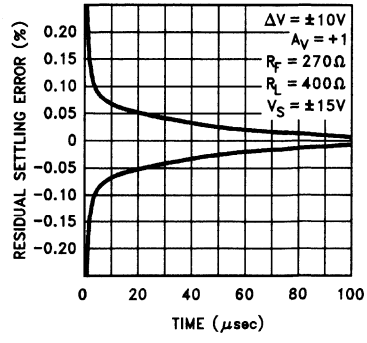
$A_V = +2$, $R_F = R_G = 270\Omega$, $R_L = 150\Omega$, $V_S = \pm 15V$

2120-11

Settling Time vs Swing



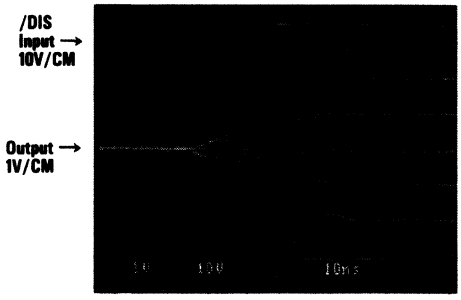
Long Term Settling Error



2120-12

Typical Performance Curves — Contd.

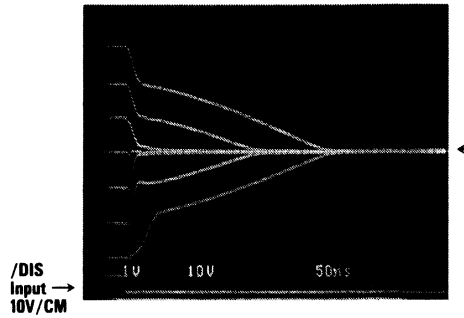
Enable Response for a Family of Inputs



$A_V = +2$, $R_L = 150\Omega$,
$V_S = \pm 5V$

2120-13

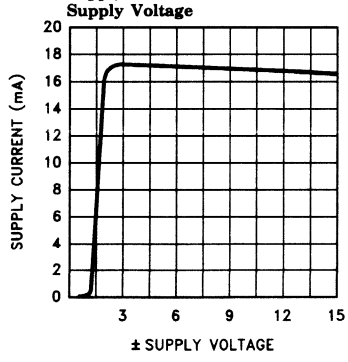
Disable Response for a Family of Inputs



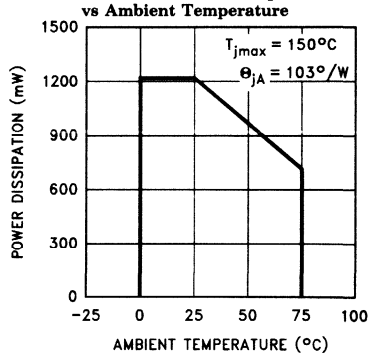
$A_V = +2$, $R_L = 150\Omega$,
$V_S = \pm 5V$

2120-14

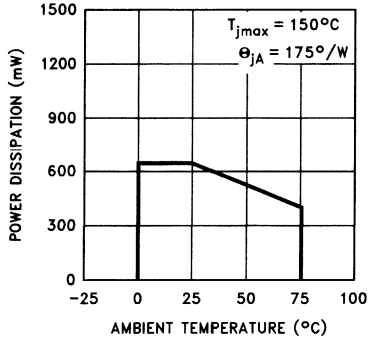
Supply Current vs Supply Voltage



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2120-15

EL2120C
100 MHz Current Feedback Amplifier

Applications Information

The EL2120C represents the third generation of current-feedback amplifier design. It is designed to provide good high-frequency performance over wide supply voltage, load impedance, gain, temperature, and manufacturing lot variations. It is a well-behaved amplifier in spite of its 100 MHz bandwidth, but a few precautions should be taken to obtain maximum performance.

The power supply pins must be well bypassed. 0.01 μF ceramic capacitors are adequate, but lead length should be kept below $\frac{1}{4}$" and a ground plane is recommended. Bypassing with 4.7 μF tantalum capacitors can improve settling characteristics, and smaller capacitors in parallel will not be needed. The lead length of sockets generally deteriorates the amplifier's frequency response by exaggerating peaking and increasing ringing in response to transients. Short sockets cause little degradation.

Load capacitance also increases ringing and peaking. Capacitance greater than 35 pF should be isolated with a series resistor. Capacitance at the V_{IN-} terminal has a similar effect, and should be kept below 5 pF. Often, the inductance of the leads of a load capacitance will be self-resonant at frequencies from 40 MHz to 200 MHz and can cause oscillations. A resonant load can be de-Q'ed with a small series or parallel resistor. A "snubber" can sometimes be used to reduce resonances. This is a resistor and capacitor in series connected from output to ground. Values of 68Ω and 33 pF are typical. Increasing the feedback resistor can also improve frequency flatness.

The V_{IN+} pin can oscillate in the 200 MHz to 500 MHz realm if presented with a resonant or inductive source impedance. A series 27Ω to 68Ω resistor right on the V_{IN+} pin will suppress such oscillations without affecting frequency response.

-3 dB bandwidth is inversely proportional to the value of feedback resistor R_F. The EL2120C will tolerate values as low as 180Ω for a maximum bandwidth of about 140 MHz, but peaking will increase and tolerance to stray capacitance will reduce. At gains greater than 5, -3 dB bandwidth begins to reduce, and a smaller R_F can be used to maximize frequency response.

The greatest frequency response flatness (to 0.1 dB, for instance) occurs with R_F = 300Ω to 330Ω. Even the moderate peaking caused by lower values of R_F will cause the gain to peak out of the 0.1 dB window, and higher values of R_F will cause an overcompensated response where the gain falls below the 0.1 dB level. Parasitic capacitances will generally degrade the frequency flatness.

The EL2120C should not output a continuous current above 50 mA, as stated in the ABSOLUTE MAXIMUM RATINGS table. The output current limit is set to 120 mA at a die temperature of 25°C and reduces to 85 mA at a die temperature of 150°C. This large current is needed to slew load capacitance and drive low impedance loads with low distortion but cannot be supported continuously. Furthermore, package dissipation capabilities cannot be met under short-circuit conditions. Current limit should not occur longer than a few seconds.

The output disable function of the EL2120C is optimized for video performance. While in disable mode, the feedthrough of the circuit can be modeled as a 0.2 pF capacitor from V_{IN+} to the output. No more than $\pm$5V can be placed between V_{IN+} and V_{IN-} in disable mode, but this is compatible with common video signal levels. In disabled state the output can withstand about 1000 V/μs slew rate signals impressed on it without the output transistors turning on.

The /Disable pin logic level is referred to V+. With $\pm$5V supplies, a CMOS or TTL driver with pull-up resistor will suffice. $\pm$15V supplies require a +14/+11V drive span, or +15/+10V nominally. Open-collector TTL with a tapped pull-up resistor can provide these spans. The impedance of the divider should be 1k or less for optimum enable/disable speed.

The EL2120C enables in 50 ns or less. When V_{IN} = 0, only a small switching glitch occurs at the output. When V_{IN} is some other value, the output overshoots by about 0.7V when settling toward its new enabled value.

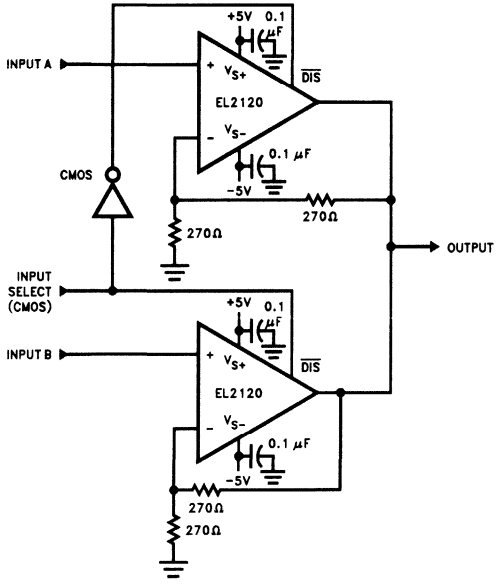
Applications Information — Contd.

When the EL2120C disables, it turns off very rapidly for inputs of ±1V or less, and the output sags more slowly for inputs larger than this. For inputs as large as ±2.5V the output current can be absorbed by another EL2120C simultaneously enabled. Under these conditions, switching will be properly completed in 50 ns or less.

The greater thermal resistance of the SO-8 package requires that the EL2120C be operated from ±10V supplies or less to maintain the 150°C maximum die temperature over the commercial temperature range. The P-DIP package allows the full ±16.5V supply operation.

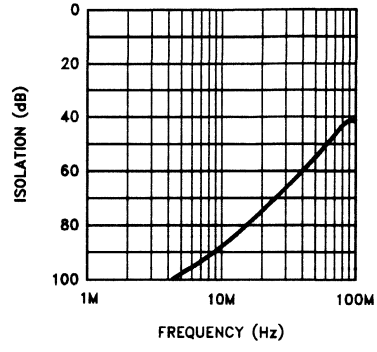
Typical Applications Circuit—A High Quality Two-Input Multiplexer

Dual EL2120C Multiplexer



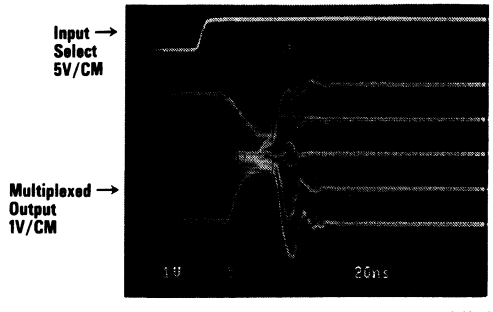
2120-16

Channel-to-Channel Isolation of Dual EL2120C Multiplexer



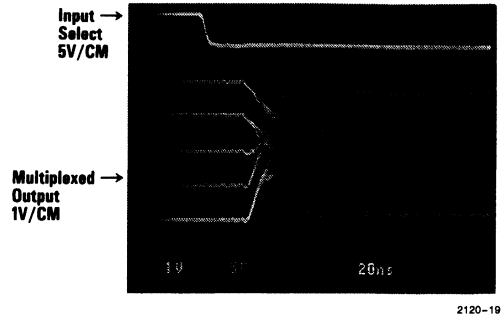
2120-17

Dual EL2120C Multiplexer Switching Channels: Uncorrelated Sinewave Switched to a Family of DC Levels



2120-18

Dual EL2120C Multiplexer Switching Channels: a Family of DC Levels Switched to an Uncorrelated Sinewave



2120-19

EL2120C
100 MHz Current Feedback Amplifier

The EL2120C Macromodel

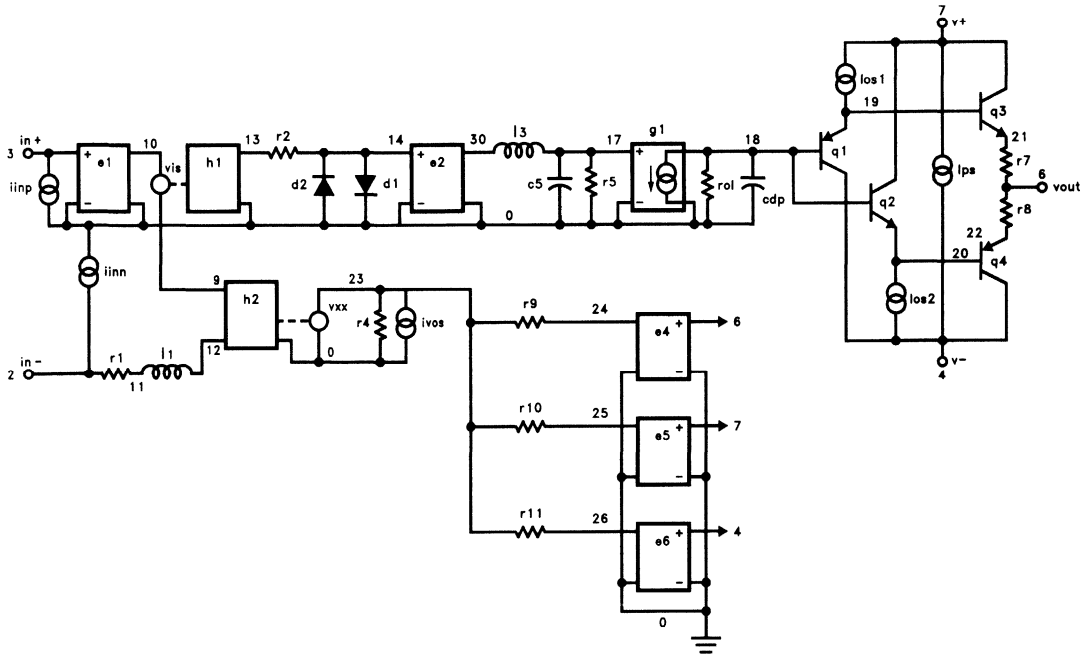
This macromodel has been developed to assist the user in simulating the EL2120C with surrounding circuitry. It was developed for the PSPICE simulator (copywritten by the Microsim corporation), and may need to be rearranged for other simulators, particularly the H operator. It approximates frequency response and small-signal transients as well, although the effects of load capacitance does not show. This model is slightly more complicated than the models used for low-frequency op-amps, but is much more accurate for AC.

The model does not simulate these characteristics accurately:

noise	non-linearities
slew rate limitations	temperature effects
settling time	manufacturing variations
input or output resonances	CMRR and PSRR

```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2120       3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 25
l1 11 12 20nH
iinp 3 0 10µA
iinm 2 0 5µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
s2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l5 30 17 1µH
c5 17 0 0.5pF
r5 17 0 600
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 140K
cdp 18 0 7.9pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5mA
ios2 20 4 2.5mA
*
* Supply
*
ips 7 4 10mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 6 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 10K
r11 26 23 10K
*
* Models
*
.model qn npn (is=5e-15 bf=500 tf=0.1nS)
.model qp pnp (is=5e-15 bf=500 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.02 bv=4 n =4)
.ends
```

The EL2120C Macromodel — Contd.



EL2120 Macromodel

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2130C
85 MHz Current Feedback Amplifier

Features

- −3 dB bandwidth = 85 MHz, A_V = 1
- −3 dB bandwidth = 75 MHz, A_V = 2
- NTSC/PAL dG ≤ 0.03%, dP ≤ 0.1°
- 50 mA output current
- Drives ±2.5V into 100Ω load
- Low voltage noise = 4 nV/$\sqrt{\text{Hz}}$
- Current mode feedback
- Low cost

Applications

- Video amplifier
- Video distribution amplifier
- Residue amplifiers in ADC
- Current to voltage converter
- Coaxial cable driver

Ordering Information

Part No.	Temp. Range	Pkg.	Outline*
EL2130CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2130CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

The EL2130 is a wideband current mode feedback amplifier optimized for gains between −10 and +10 while operating on ±5V power supplies. Built using Elantec's Complementary Bipolar process, this device exhibits −3 dB bandwidths in excess of 85 MHz at unity gain and 75 MHz at a gain of two. The EL2130 is capable of output currents in excess of 50 mA giving it the ability to drive either double or single terminated 50Ω coaxial cables.

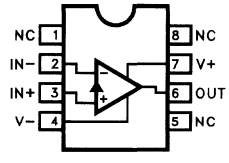
Exhibiting a Differential Gain of 0.03% and a Differential Phase of 0.1° at NTSC and PAL frequencies. The EL2130 is an excellent low cost solution to most video applications.

In addition, the EL2130 exhibits very low gain peaking, typically below 0.1 dB to frequencies in excess of 40 MHz as well as 50 ns settling time to 0.2% making it an excellent choice for driving flash A/D converters.

The device is available in the plastic 8-lead narrow-body small outline (SO) and the 8-pin mini DIP packages, and operates over the temperature range of 0°C to +75°C.

Connection Diagram

Mini DIP and SO



2130-1

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±6V	T_J	Operating Junction Temperature	150°C
V_{IN}	Input Voltage	$\pm V_S$	T_{ST}	Storage Temperature	−65°C to +150°C
ΔV_{IN}	Differential Input Voltage	±6V		Lead Temperature	
P_D	Maximum Power Dissipation	See Curves		DIP Package (soldering, <10 seconds)	300°C
I_{IN}	Input Current	±10 mA		SO Package	
I_{OP}	Output Short Circuit Duration	≤5 sec		Vapor Phase (60 seconds)	215°C
T_A	Operating Temperature Range:	0°C to +75°C		Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Electro performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX2002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX2002.
III	QA sample tested per QA test plan QCX2002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±5V; R_L = ∞, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage		25°C		2.0	10	I	mV
			T_{MIN}, T_{MAX}			15	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift				7		V	µV/°C
$+I_{IN}$	+Input Current		25°C		5.5	15	I	µA
			T_{MIN}, T_{MAX}			25	III	µA
$-I_{IN}$	+Input Current		25°C		10	40	I	µA
			T_{MIN}, T_{MAX}			50	III	µA
$+R_{IN}$	+Input Resistance		25°C	1.0	2.0		I	MΩ
C_{IN}	+Input Capacitance		25°C		1.0		V	pF
CMRR	Common Mode Rejection Ratio	V_{CM} = ±2.5V	25°C	50	60		I	dB
−ICMR	Input Current Common Mode Rejection	V_{CM} = ±2.5V	25°C		5	10	I	µA/V
			T_{MIN}, T_{MIN}			20	III	µA/V
PSRR	Power Supply Rejection Ratio	±4.5V ≤ V_S ≤ ±6V	25°C	60	70		I	dB
+IPSR	+Input Current Power Supply Rejection	±4.5V ≤ V_S ≤ ±6V	25°C		0.1	0.5	I	µA/V
			T_{MIN}, T_{MIN}			1.0	III	µA/V
−IPSR	−Input Current Power Supply Rejection	±4.5V ≤ V_S ≤ ±6V	25°C		0.5	5.0	I	µA/V
			T_{MIN}, T_{MIN}			8.0	III	µA/V

EL2130C
85 MHz Current Feedback Amplifier

Open Loop DC Electrical Characteristics

$V_S = \pm 5V$; $R_L = \infty$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
R_{OL}	Transimpedance	$V_{OUT} = \pm 2.5V$, $R_L = 100\Omega$	25°C	80	145		I	V/mA
			T_{MIN}, T_{MAX}	70			III	V/mA
A_{VOL}	Open Loop DC Voltage Gain	$V_{OUT} = \pm 2.5V$, $R_L = 100\Omega$	25°C	60	66		I	dB
			T_{MIN}, T_{MAX}	56			III	dB
V_O	Output Voltage Swing	$R_L = 100\Omega$	25°C	3	3.5		I	V
I_{OUT}	Output Current		25°C	30	50		I	mA
R_{OUT}	Output Resistance		25°C		5		V	Ω
I_S	Quiescent Supply Current		Full		17	21	I	mA
I_{SC}	Short Circuit Current		25°C		85		V	mA

Closed Loop AC Electrical Characteristics

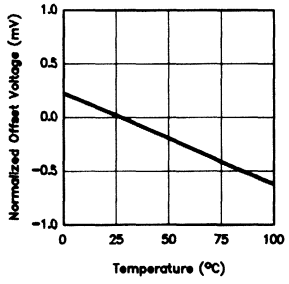
$V_S = \pm 5V$, $A_V = +2$, $R_F = R_G = 820\Omega$, $R_L = 100\Omega$, $T_A = 25°C$

Parameter	Description	Condition	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 1)	$V_O = 5\ V_{p-p}$		625		V	V/μs
t_r	Rise Time	$V_O = 200$ mV		4.6		V	ns
t_f	Fall Time	$V_O = 200$ mV		4.6		V	ns
t_{pd}	Prop Delay	$V_O = 200$ mV		4.0		V	ns
SSBW	3 dB Bandwidth	$V_O = 100$ mV		75		V	MHz
dG	NTSC/PAL Diff Gain			0.03		V	%
dP	NTSC/PAL Diff Phase			0.10		V	deg (°)
GFPL	Gain Flatness	f < 40 MHz		0.08		V	dB

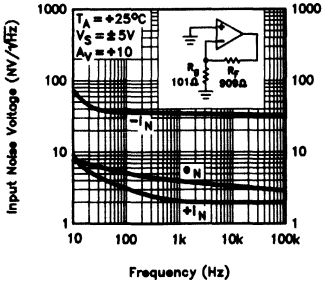
Note 1: Slew rate is measured with $V_O = 5V_{p-p}$ between −1.25V and +1.25V and +1.25V and −1.25V.

Typical Performance Curves

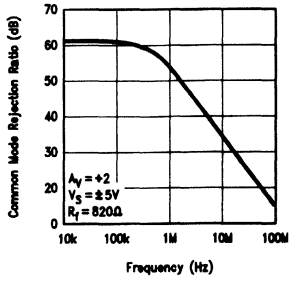
Normalized Offset Voltage vs Temperature



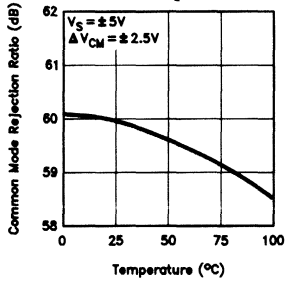
Equivalent Input Noise



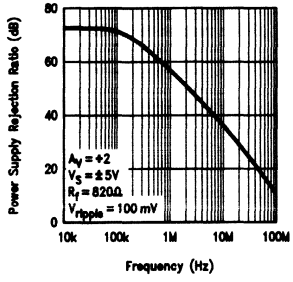
Common Mode Rejection Ratio vs Frequency



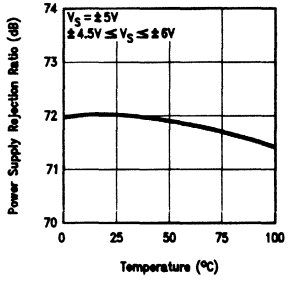
Common Mode Rejection Ratio vs Temperature



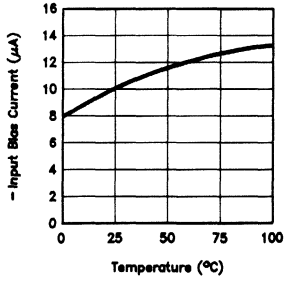
Power Supply Rejection Ratio vs Frequency



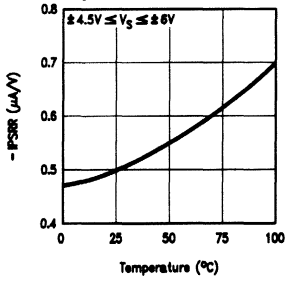
Power Supply Rejection Ratio vs Temperature



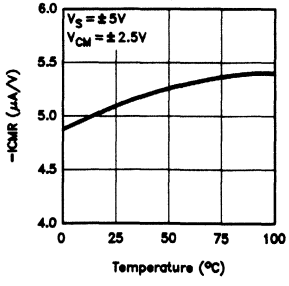
−Input Bias Current vs Temperature



−Input Bias Current Power Supply Rejection Ratio



−Input Bias Current Common Mode Rejection Ratio vs Temperature

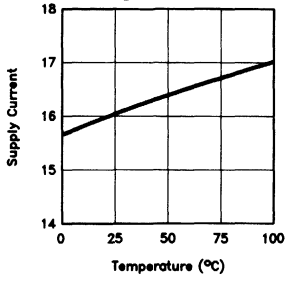


2130-2

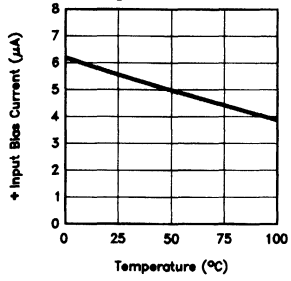
EL2130C
85 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

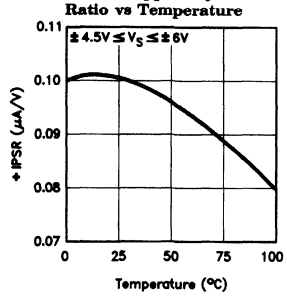
Supply Current vs Temperature



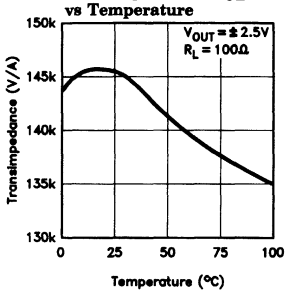
+Input Bias Current vs Temperature



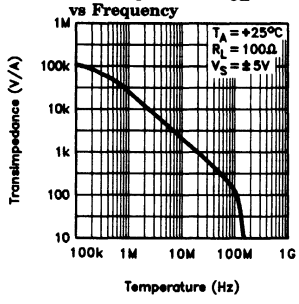
+Input Bias Current Power Supply Rejection Ratio vs Temperature



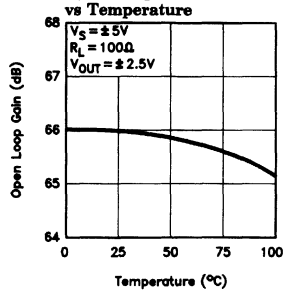
Transimpedance (R_{OL}) vs Temperature



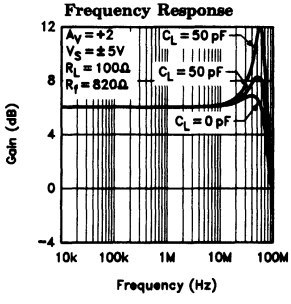
Transimpedance (R_{OL}) vs Frequency



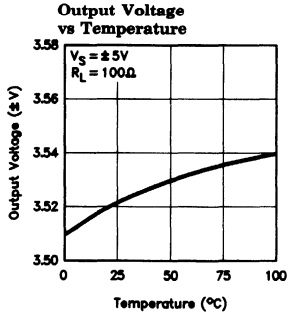
Open Loop Gain vs Temperature



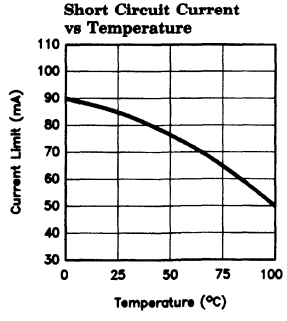
Frequency Response



Output Voltage vs Temperature



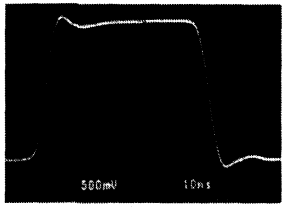
Short Circuit Current vs Temperature



2130-3

Typical Performance Curves — Contd.

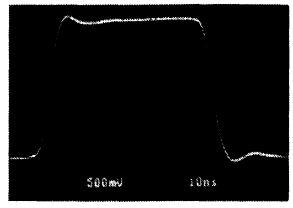
Large Signal Response



2130-4

$A_V = +1$, $R_F = 820\Omega$
$R_L = 100\Omega$, $C_L = 12$ pF

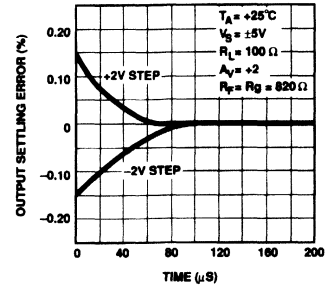
Large Signal Response



2130-5

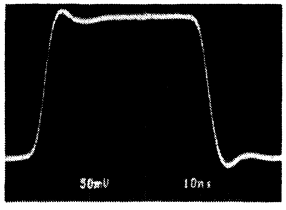
$A_V = +2$, $R_F = 820\Omega$
$R_L = 100\Omega$, $C_L = 12$ pF

Long-Term Output Settling Error vs Time, $V_S = \pm 5V$



2130-6

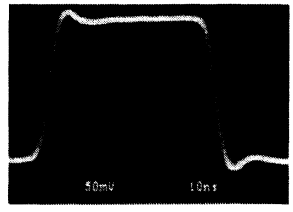
Small Signal Response



2130-7

$A_V = +1$, $R_F = 820\Omega$
$R_L = 100\Omega$, $C_L = 12$ pF

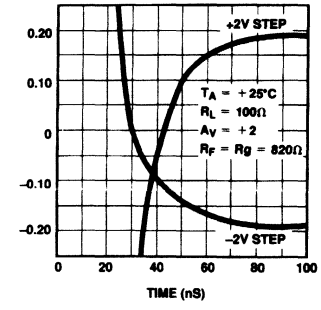
Small Signal Response



2130-8

$A_V = +2$, $R_F = 820\Omega$
$R_L = 100\Omega$, $C_L = 12$ pF

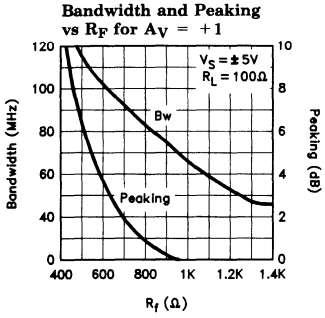
Short Term Output Settling Error vs Time, $V_S = \pm 5V$

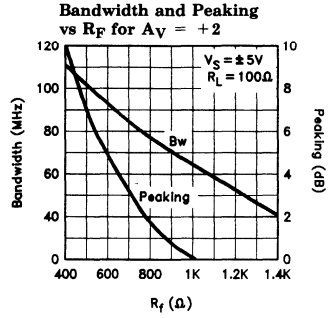


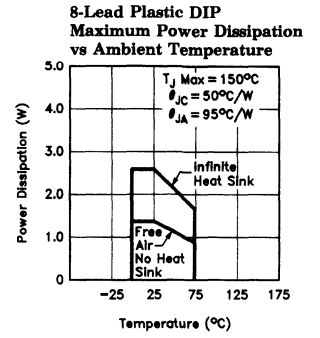
2130-9

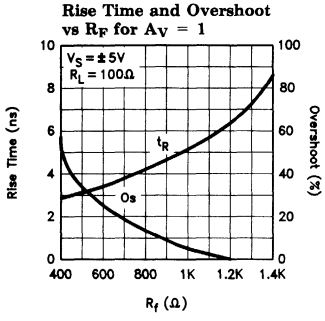
EL2130C
85 MHz Current Feedback Amplifier

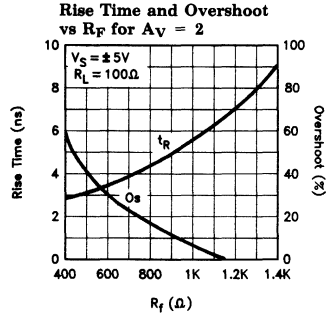
Typical Performance Curves — Contd.

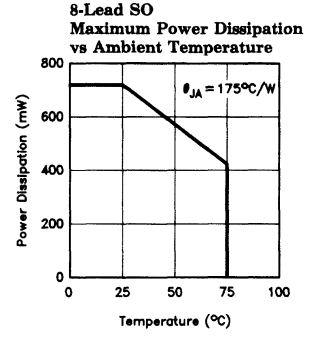












2130-10

Applications Information

Power Supply Bypassing

The EL2130 will exhibit ringing or oscillation if the power supply leads are not adequately bypassed. 0.1 μF ceramic disc capacitors are suggested for both supply pins at a distance no greater than ½ inch from the device. Surface mounting chip capacitors are strongly recommended.

Lead Dress

A ground plane to which decoupling capacitors and gain setting resistors are terminated will eliminate overshoot and ringing. However, the ground plane should not extend to the vicinity of both the non-inverting and inverting inputs (pins 3 and 2) which would add capacitance to these nodes, and lead lengths from these pins should be made as short as possible.

Use of sockets, particularly for the SO package, should be avoided if possible. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Video Characteristics and Applications

Frequency domain testing is performed at Elantec using a computer controlled HP model 8656B Signal Generator and an HP Model 4195A Network/Spectrum Analyzer. The DUT test board is built using microwave/strip line techniques, and solid coaxial cables route the stimulus to the DUT socket. Signals are routed to and from the DUT test fixture using subminiature coaxial cable.

Differential Gain and Phase are tested at a noise gain of 2 with 100Ω load. Gain and Phase measurements are made with a DC input reference

Applications Information — Contd.

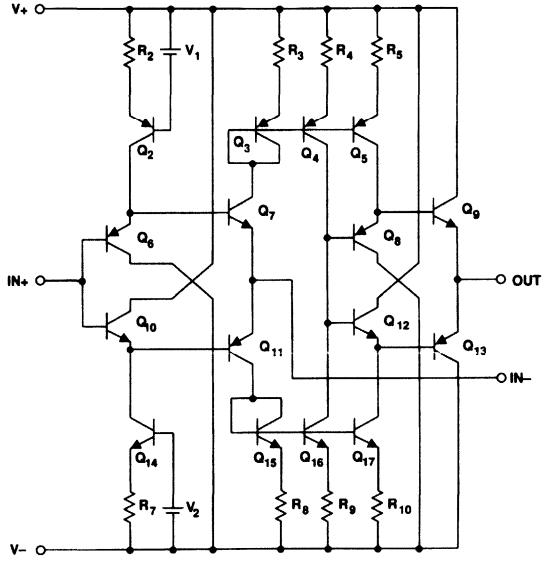
voltage at 0V and compared to those made at V_{ref} equal to 0.7V at frequencies extending to 30 MHz.

The EL2130 is capable of driving 100Ω to a minimum of 2.5V peak which means that it can naturally drive double terminated (50Ω) coaxial cables.

Capacitive Loads

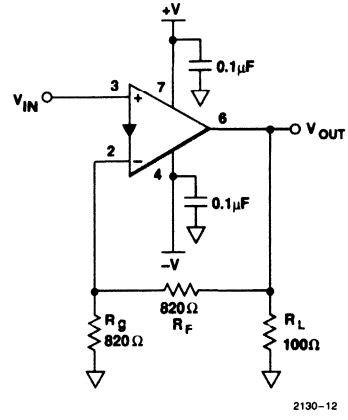
As can be seen from the Bode plot, the EL2130 will peak into capacitive loads greater than 20 pf. In many applications such as flash A/D's, capacitive loading is unavoidable. In these cases, the use of a snubber network consisting of a 100Ω resistor in series with 47 pF capacitor from the output to ground is recommended.

Equivalent Circuit



2130-11

AC Test Circuit



2130-12

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2160C
130 MHz Current Feedback Amplifier

Features

- 130 MHz 3 dB bandwidth ($A_V = +2$)
- 180 MHz 3 dB bandwidth ($A_V = +1$)
- 0.01% differential gain, $R_L = 500\Omega$
- 0.01° differential phase, $R_L = 500\Omega$
- Low supply current, 8.5 mA
- Wide supply range, ±2V to ±15V
- 80 mA output current (peak)
- Low cost
- 1500 V/μs slew rate
- Input common mode range to within 1.5V of supplies
- 35 ns settling time to 0.1%

Applications

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converter

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2160CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2160CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL2160C is a current feedback operational amplifier with −3 dB bandwidth of 130 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, this amplifer uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

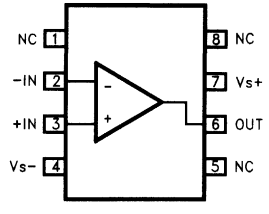
The EL2160C is designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (<0.01%/<0.01°) and double terminated 75Ω cables (0.025%/0.1°).

The amplifier can operate on any supply voltage from 4V (±2V) to 33V (±16.5V), yet consume only 8.5 mA at any supply voltage. Using industry standard pinouts, the EL2160C is available in 8-pin P-DIP and 8-pin SO packages. For dual and quad applications, please see the EL2260C/EL2460C datasheet.

Elantec's facilities comply with MIL-I-45208A and offer applicable quality specifications. For information on Elantec's military processing, see the Elantec document, QRA-2: *Elantec's Military Processing—Monolithic Products.*

Connection Diagram

EL2160C SO, P-DIP Packages



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Top View

November 1993 Rev A

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S^+ and V_S^-	+33V	Output Current	±50 mA
Voltage between +IN and −IN	±6V	Storage Temperature Range	−65°C to +150°C
Current into +IN or −IN	10 mA	Lead Temperature	
Internal Power Dissipation	See Curves	DIP Package	
Operating Ambient Temperature Range	−40°C to +85°C	(Soldering, <10 seconds)	300°C
Operating Junction Temperature		SO Package	
Plastic Packages	150°C	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2160C	
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V	25°C		2	10	I	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		10		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		0.5	3	I	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		5	25	I	µA
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	25°C	50	55		II	dB
−ICMR	−Input Current Common Mode Rejection (Note 2)	V_S = ±5V, ±15V	25°C		0.2	5	I	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		25°C	75	95		II	dB
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.2	5	I	µA/V

EL2160C
130 MHz Current Feedback Amplifier

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 15V$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2160C	
R_{OL}	Transimpedance (Note 4)	$V_S = \pm 15V$, $R_L = 400\Omega$	25°C	500	2000		I	kΩ
		$V_S = \pm 5V$, $R_L = 150\Omega$	25°C	500	1800		I	kΩ
$+R_{IN}$	+Input Resistance		25°C	1.5	3.0		II	MΩ
$+C_{IN}$	+Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range	$V_S = \pm 15V$	25°C		±13.5		V	V
		$V_S = \pm 5V$	25°C		±3.5		V	V
V_O	Output Voltage Swing	$R_L = 400\Omega$, $V_S = \pm 15V$	25°C	±12	±13.5		I	V
		$R_L = 150\Omega$, $V_S = \pm 15V$	25°C		±12		V	V
		$R_L = 150\Omega$, $V_S = \pm 5V$	25°C	±3.0	±3.7		I	V
I_{SC}	Output Short Circuit Current (Note 4)	$V_S = \pm 5V$, $V_S = \pm 15V$	25°C	60	100	150	I	mA
I_S	Supply Current	$V_S = \pm 15V$	25°C		8.5	11.0	I	mA
		$V_S = \pm 5V$	25°C		6.4	8.5	I	mA

Closed Loop AC Electrical Characteristics

V_S = ±15V, A_V = +2, R_F = 560Ω, R_L = 150Ω, T_A = 25°C unless otherwise noted

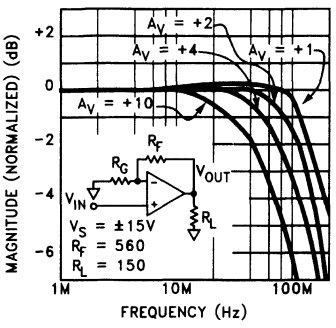
Parameter	Description	Conditions	Limits			Test Level	Units
			Min	Typ	Max	EL2160C	
BW	−3 dB Bandwidth (Note 8)	V_S = ±15V, A_V = +2		130		V	MHz
		V_S = ±15V, A_V = +1		180		V	MHz
		V_S = ±5V, A_V = +2		100		V	MHz
		V_S = ±5V, A_V = +1		110		V	MHz
SR	Slew Rate (Notes 6, 8)	R_L = 400Ω	1000	1500		IV	V/μs
		R_F = 1KΩ, R_G = 110Ω, R_L = 400Ω		1500		V	V/μs
t_r, t_f	Rise Time, Fall Time, (Note 8)	V_{OUT} = ±500mV		2.7		V	ns
t_{pd}	Propagation Delay (Note 8)			3.2		V	ns
OS	Overshoot (Note 8)	V_{OUT} = ±500 mV		0		V	%
t_s	0.1% Settling Time (Note 8)	V_{OUT} = ±10V, A_V = −1, R_L = 1K		35		V	ns
dG	Differential Gain (Notes 7, 8)	R_L = 150Ω		0.025		V	%
		R_L = 500Ω		0.006		V	%
dP	Differential Phase (Notes 7, 8)	R_L = 150Ω		0.1		V	deg (°)
		R_L = 500Ω		0.005		V	deg (°)

Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: V_{CM} = ±13V for V_S = ±15V and T_A = 25°C
V_{CM} = ±3V for V_S = ±5V and T_A = 25°C
Note 3: The supplies are moved from ±2.5V to ±15V.
Note 4: V_{OUT} = ±7V for V_S = ±15V, and V_{OUT} = ±2V for V_S = ±5V.
Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 6: Slew Rate is with V_{OUT} from +10V to −10V and measured at the 25% and 75% points.
Note 7: DC offset from −0.714V through +0.714V, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.
Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

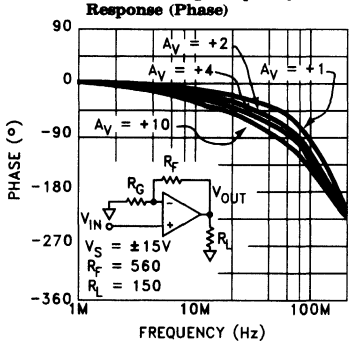
EL2160C
130 MHz Current Feedback Amplifier

Typical Performance Curves

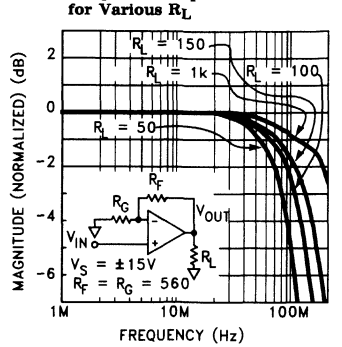
Non-Inverting Frequency Response (Gain)



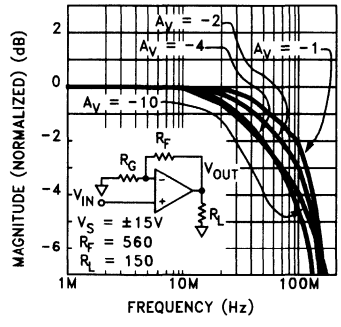
Non-Inverting Frequency Response (Phase)



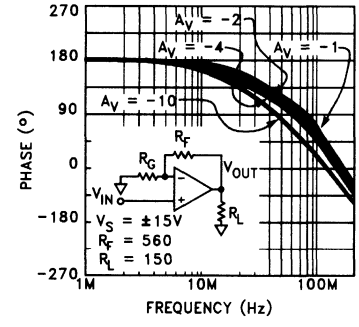
Frequency Response for Various R_L



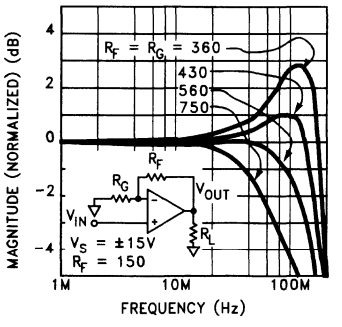
Inverting Frequency Response (Gain)



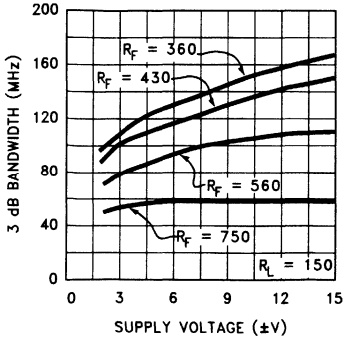
Inverting Frequency Response (Phase)



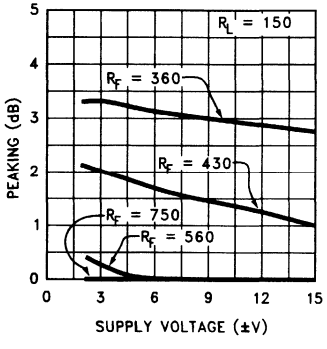
Frequency Response for Various R_F and R_G



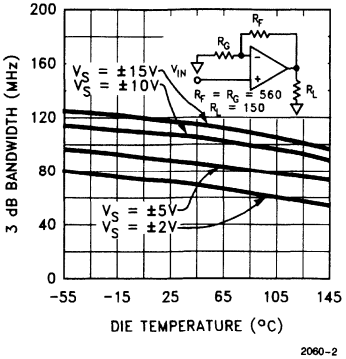
3 dB Bandwidth vs Supply Voltage for $A_V = -1$



Peaking vs Supply Voltage for $A_V = -1$



3 dB Bandwidth vs Temperature for $A_V = -1$



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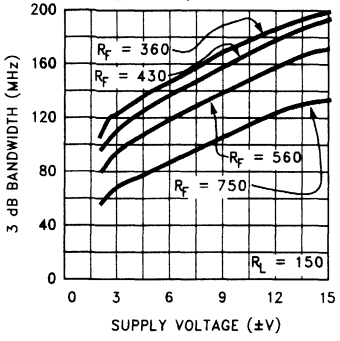
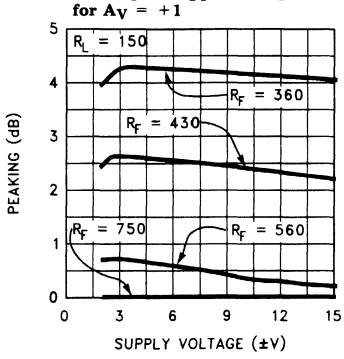
Typical Performance Curves — Contd.

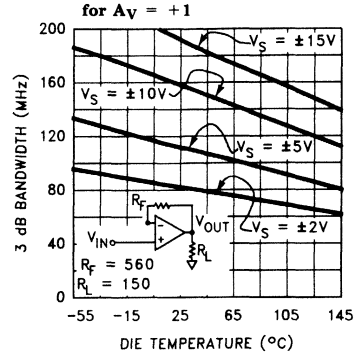
3 dB Bandwidth vs Supply Voltage for A_V = +1



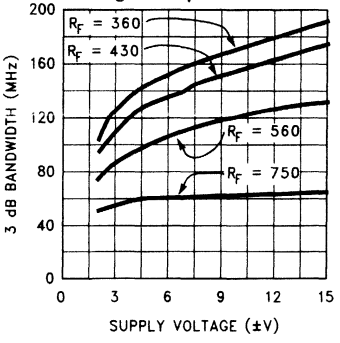
Peaking vs Supply Voltage for A_V = +1



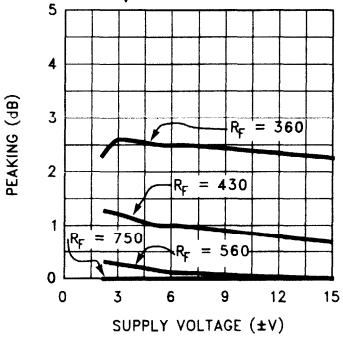
3 dB Bandwidth vs Temperature for A_V = +1



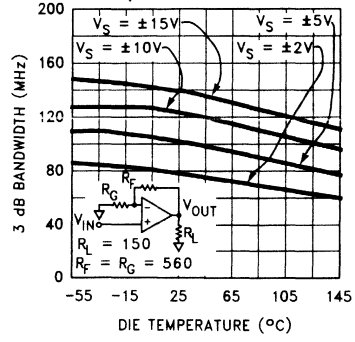
3 dB Bandwidth vs Supply Voltage for A_V = +2



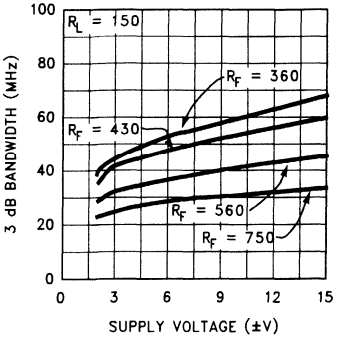
Peaking vs Supply Voltage for A_V = +2



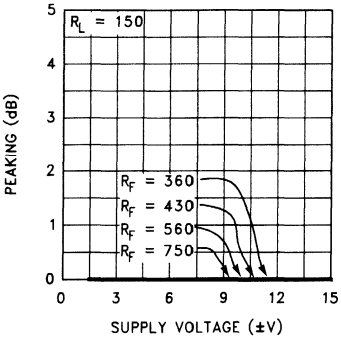
3 dB Bandwidth vs Temperature for A_V = +2



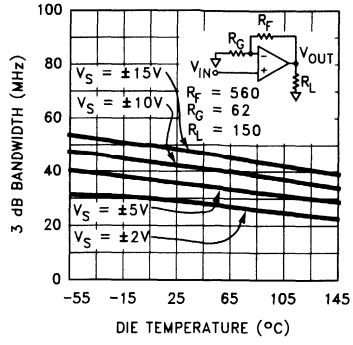
3 dB Bandwidth vs Supply Voltage for A_V = +10



Peaking vs Supply Voltage for A_V = +10



3 dB Bandwidth vs Temperature for A_V = +10

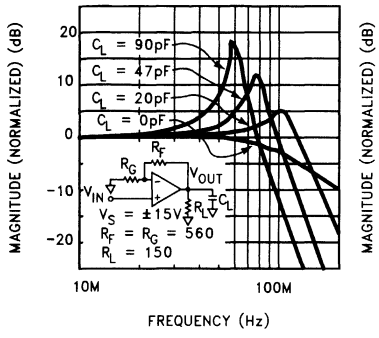


2060-3

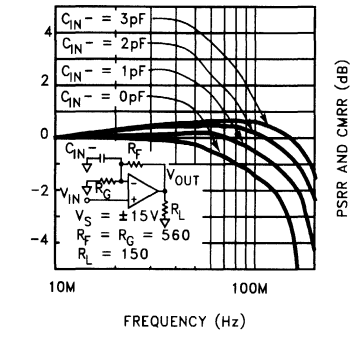
EL2160C
130 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

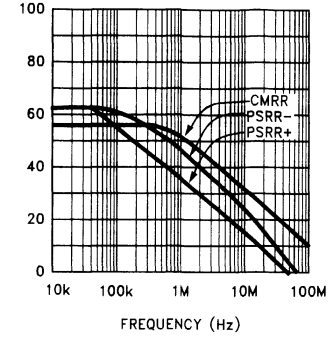
Frequency Response for Various C_L



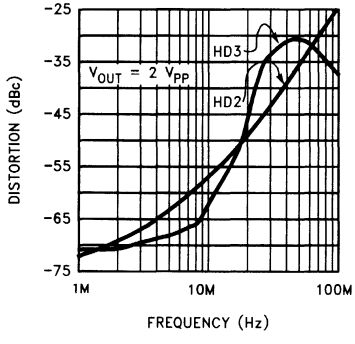
Frequency Response for Various C_{IN-}



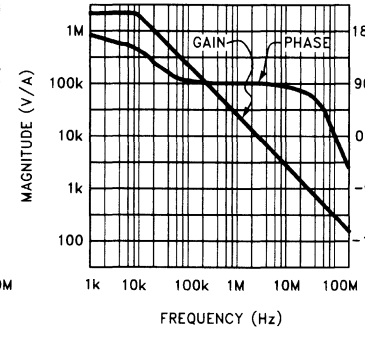
PSRR and CMRR vs Frequency



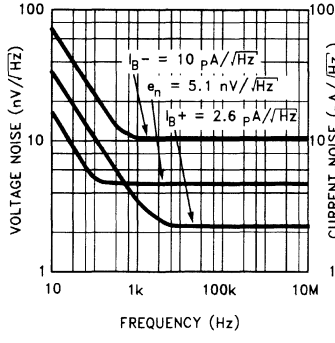
2nd and 3rd Harmonic Distortion vs Frequency



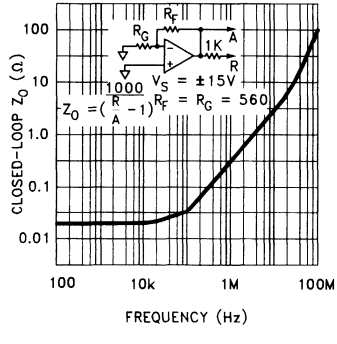
Transimpedance (R_{OL}) vs Frequency



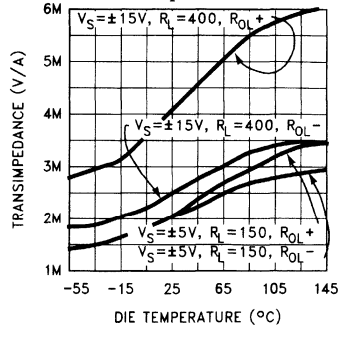
Voltage and Current Noise vs Frequency



Closed-Loop Output Impedance vs Frequency



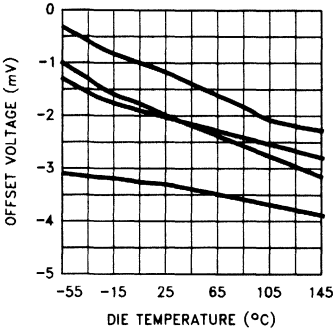
Transimpedance (R_{OL}) vs Die Temperature



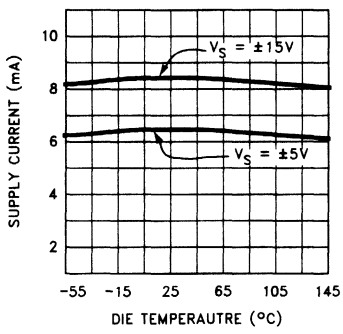
2060-4

Typical Performance Curves — Contd.

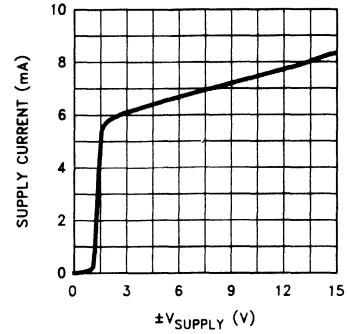
Offset Voltage vs Die Temperature (4 Samples)



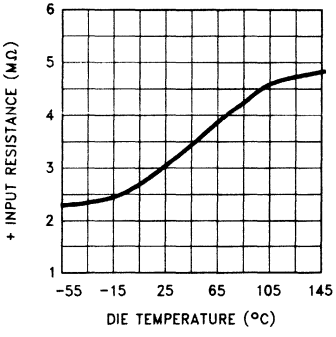
Supply Current vs Die Temperature



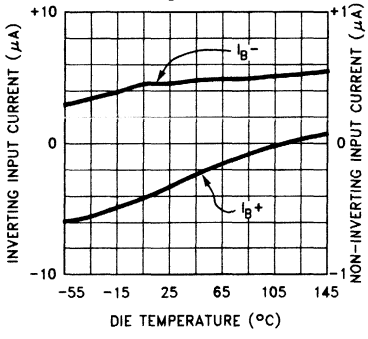
Supply Current vs Supply Voltage



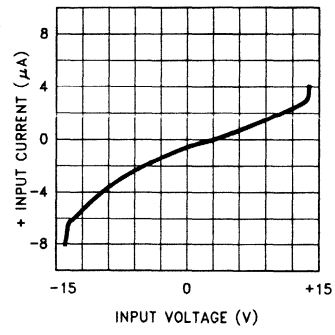
+Input Resistance vs Die Temperature



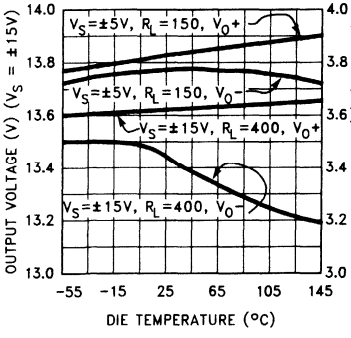
Input Current vs Die Temperature



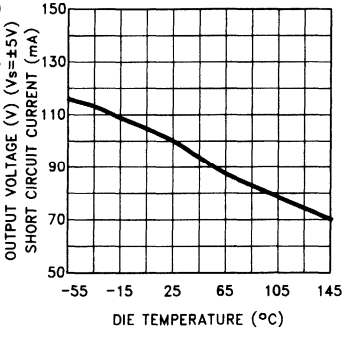
+Input Bias Current vs Input Voltage



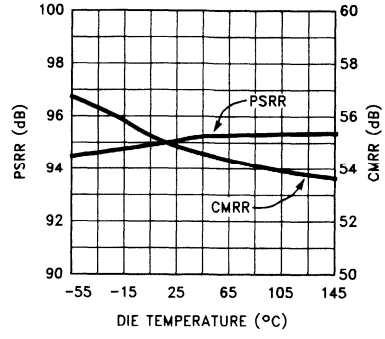
Output Voltage Swing vs Die Temperature



Short Circuit Current vs Die Temperature



PSRR & CMRR vs Die Temperature



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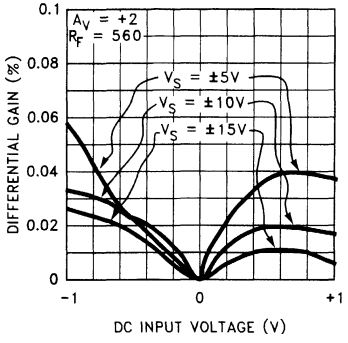
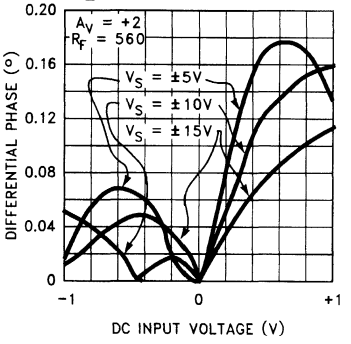
EL2160C
130 MHz Current Feedback Amplifier

Typical Performance Curves — Contd.

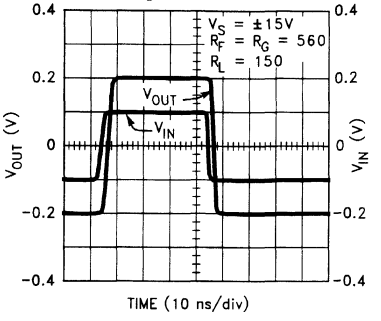
Differential Gain vs DC Input Voltage, R_L = 150



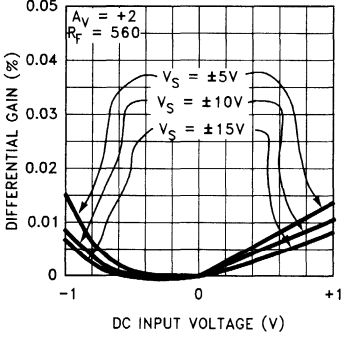
Differential Phase vs DC Input Voltage, R_L = 150



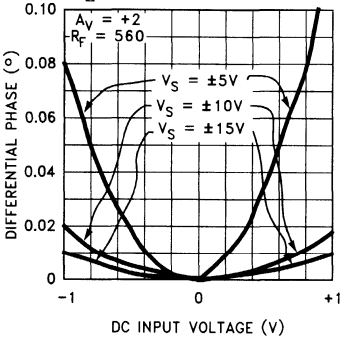
Small Signal Pulse Response



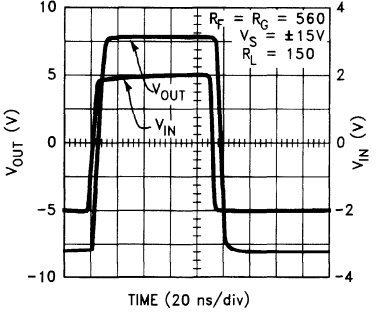
Differential Gain vs DC Input Voltage, R_L = 500



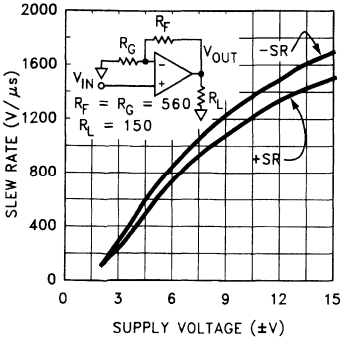
Differential Phase vs DC Input Voltage, R_L = 500



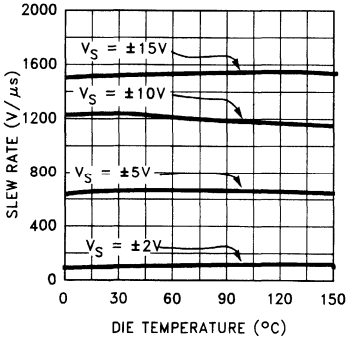
Large Signal Pulse Response



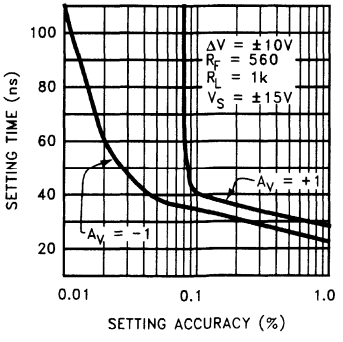
Slew Rate vs Supply Voltage



Slew Rate vs Temperature



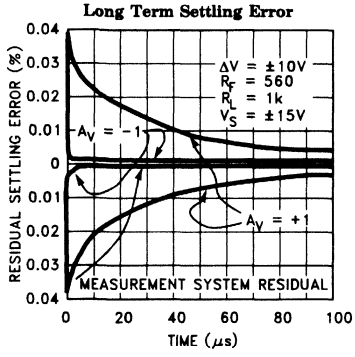
Settling Time vs Settling Accuracy



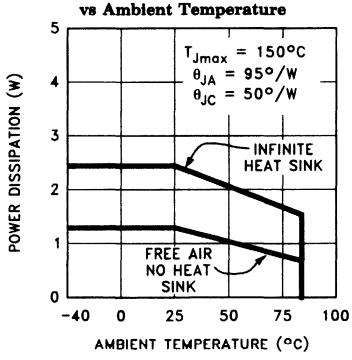
2060-6

Typical Performance Curves — Contd.

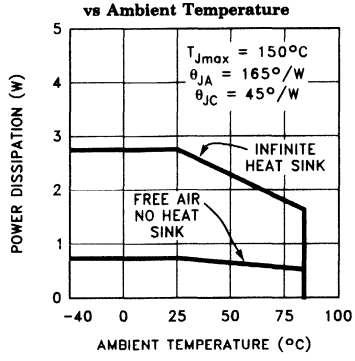
Long Term Settling Error



8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



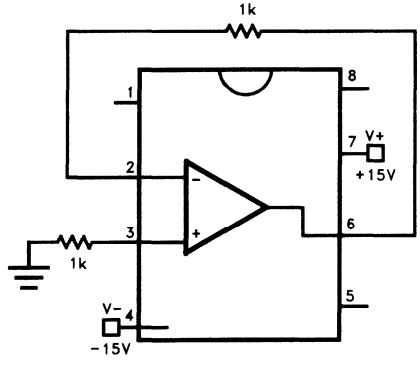
8-Lead Plastic SO
Maximum Power Dissipation
vs Ambient Temperature



2060-7

Burn-In Circuit

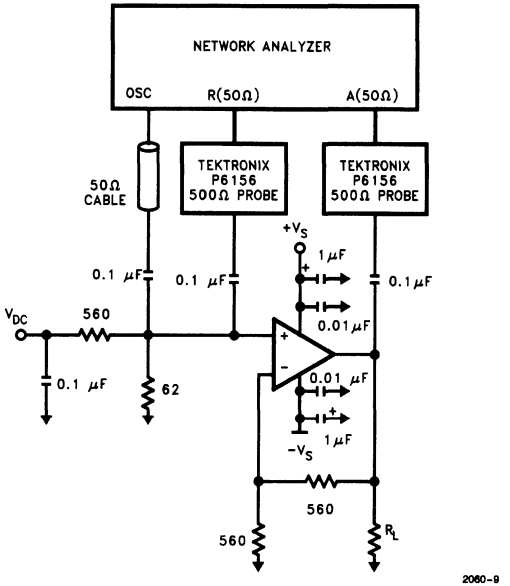
EL2160C



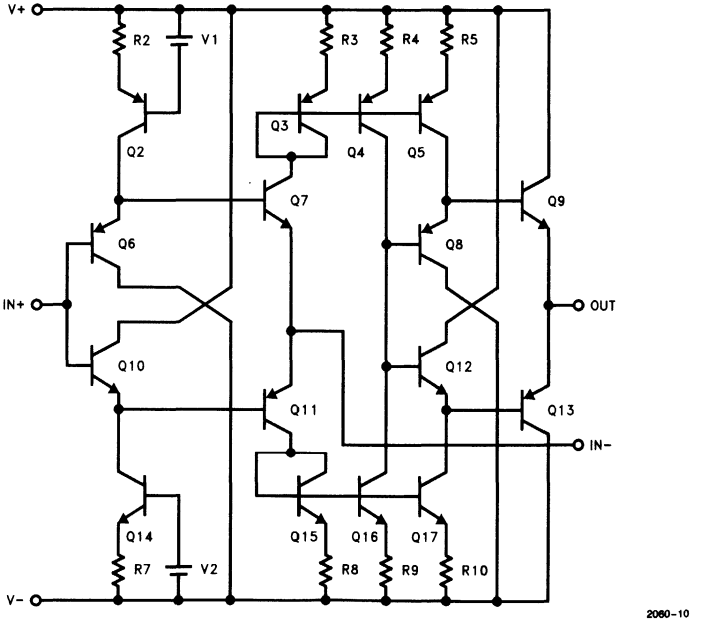
2060-8

EL2160C
130 MHz Current Feedback Amplifier

Differential Gain and Phase Test Circuit



Simplified Schematic (One Amplifier)



Applications Information

Product Description

The EL2160C is a current mode feedback amplifier that offers wide bandwidth and good video specifications at a moderately low supply current. It is built using Elantec's proprietary complimentary bipolar process and is offered in industry standard pin-outs. Due to the current feedback architecture, the EL2160C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, internal junction capacitances increase, causing a reduction in closed loop bandwidth. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼". The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO package, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2160C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN}-$ emphasizes this effect. The curve illustrates how the bandwidth can be extended to beyond 200 MHz with some additional peaking with an additional 2 pF of capacitance at the $V_{IN}-$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values

The EL2160C has been designed and specified with $R_F = 560\Omega$ for $A_V = +2$. This value of feedback resistor yields extremely flat frequency response with little to no peaking out to 130 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing R_F to 430Ω, bandwidth can be extended to 170 MHz with under 1 dB of peaking. Further reduction of R_F to 360Ω increases the bandwidth to 195 MHz with about 2.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

Bandwidth vs Temperature

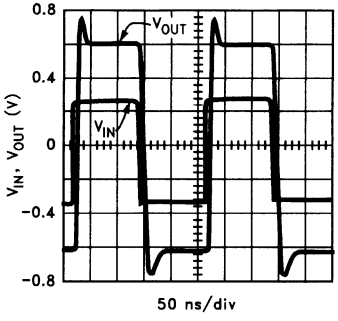
Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2160C was designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 150 MHz to 110 MHz over the entire die junction temperature range of $0°C < T < 150°C$.

EL2160C
130 MHz Current Feedback Amplifier

Applications Information — Contd.

Supply Voltage Range

The EL2160C has been designed to operate with supply voltages from ±2V to ±15V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2V supplies, the 3 dB bandwidth at A_V = +2 is a respectable 70 MHz. The following figure is an oscilloscope plot of the EL2160C at ±2V supplies, A_V = +2, R_F = R_G = 560Ω, driving a load of 150Ω, showing a clean ±600 mV signal at the output.



2060-11

If a single supply is desired, values from +4V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2160C.

Settling Characteristics

The EL2160C offers superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2160C is not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for A_V = +1, there is approximately a 0.035% residual which tails away to 0.01% in about 40 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For A_V = −1, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With A_V = −1, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2160C amplifier combines both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2160C remains within its absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = 2 * V_S * I_S + (V_S - V_{OUT}) * \frac{V_{OUT}}{R_L}$$

where I_S is the supply current. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, the EL2160C maintains almost constant supply

Applications Information — Contd.

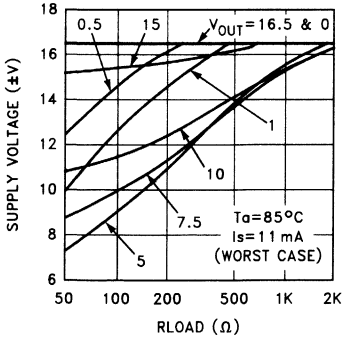
current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn't come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

The EL2160C consumes typically 8.5 mA and maximum 11.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum values if it cannot reach half supply. If we set the two P_{DMAX} equations equal to each other, and solve for V_S, we can get a family of curves for various loads and output voltages according to:

$$V_S = \frac{\frac{R_L * (T_{JMAX} - T_{AMAX})}{\theta_{JA}} + (V_{OUT})^2}{(2 * I_S * R_L) + V_{OUT}}$$

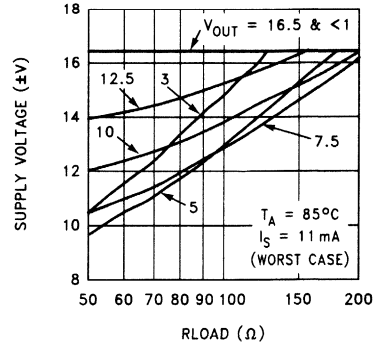
The following curves show supply voltage ($\pm V_S$) vs R_{LOAD} for various output voltage swings for the 2 different packages. The curves assume worst case conditions of $T_A = +85°C$ and $I_S = 11$ mA.

Supply Voltage vs R_{LOAD} for Various V_{OUT} (SO Package)



2060-12

Supply Voltage vs R_{LOAD} for Various V_{OUT} (PDIP Package)



2060-13

The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2160C has an internal current limit that protects the circuit in the event of the output being shorted to ground. This limit is set at 100 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 65 mA. If the output is shorted to ground, the power dissipation could be well over 1W. Heat removal is required in order for the EL2160C to survive an indefinite short.

Driving Cables and Capacitive Loads

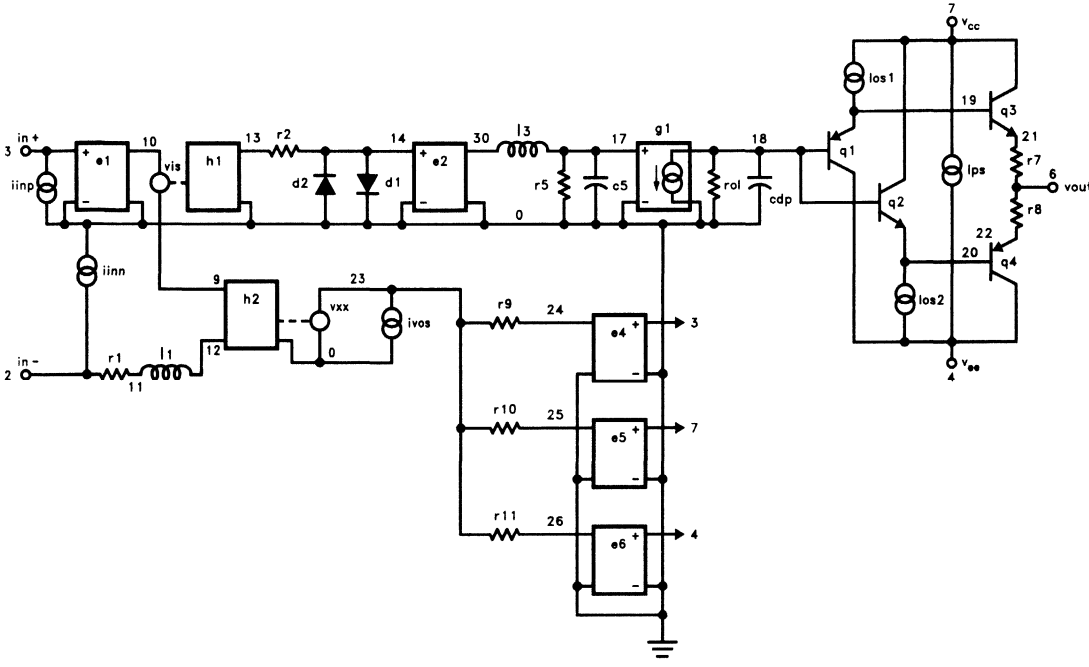
When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2160C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistor at the output.

EL2160C
130 MHz Current Feedback Amplifier

EL2160C Macromodel

```
* Revision A, November 1993
* AC Characteristics used C_IN− (pin 2) = 1 pF; R_F = 560Ω
* Connections:          +input
*                       |     −input
*                       |     |     +Vsupply
*                       |     |     |     −Vsupply
*                       |     |     |     |     output
*                       |     |     |     |     |
.subckt EL2160C/EL  3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5µA
iinm 2 0 5µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.43µH
c5 17 0 0.27pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
ro1 18 0 2Meg
cdp 18 0 2.285pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
* Supply Current
*
ips 7 4 3mA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is = 5e−15 bf = 100 tf = 0.1ns)
.model qp pnp (is = 5e−15 bf = 100 tf = 0.1ns)
.model dclamp d (is = 1e−30 ibv = 0.266 bv = 2.24 n = 4)
.ends
```

EL2160C Macromodel — Contd.



2060-14

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2210C/11C/EL2410C/11C

Low Cost, Dual and Quad Video Op Amps

Features

- Stable at gain of 2 and 100 MHz gain—bandwidth product (EL2211, EL2411)
- Stable at gain of 1 and 50 MHz gain—bandwidth product (EL2210, EL2410)
- 130V/μs slew rate
- Drives 150Ω load to video levels
- Inputs and outputs operate at negative supply rail
- ±5V or +10V supplies
- −60 dB isolation at 4.2 MHz

Applications

- Consumer video amplifier
- Active filters/integrators
- Cost sensitive applications
- Single supply amplifiers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2210CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL2211CN	−40°C to +85°C	8-pin P-DIP	MDP0031
EL2210CS	−40°C to +85°C	8-lead SO	MDP0027
EL2211CS	−40°C to +85°C	8-lead SO	MDP0027
EL2410CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2411CN	−40°C to +85°C	14-pin P-DIP	MDP0031
EL2410CS	−40°C to +85°C	14-lead SO	MDP0027
EL2411CS	−40°C to +85°C	14-lead SO	MDP0027

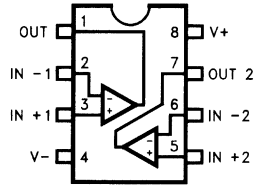
General Description

This family of dual and quad operational amplifiers built using Elantec's Complementary Bipolar process offers unprecedented high frequency performance at a very low cost. They are suitable for any application such as consumer video, where traditional DC performance specifications are of secondary importance to the high frequency specifications. On ±5V supplies at a gain of +1 the EL2210C and the EL2410C will drive a 150Ω load to +2V, −1V with a bandwidth of 50 MHz and a channel to channel isolation of 60 dB or more. At a gain of +2 the EL2211C and EL2411C will drive a 150Ω load to +2V, −1V with a bandwidth of 100 MHz with the same channel to channel isolation. All four achieve 0.1 dB BW at 5 MHz.

The power supply operating range is fixed at ±5V or +10/0V. In single supply operation the inputs and outputs will operate to ground. Each amplifier draws only 7 mA of supply current.

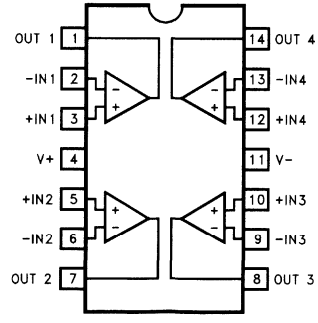
Connection Diagrams

EL2210C/EL2211C



2210-1

EL2410C/EL2411C



2210-2

Absolute Maximum Ratings

Total Voltage Supply	18V	Storage Temperature Range	−65°C to +150°C
Input Voltage	±Vs	Operating Temperature Range	−40°C to +85°C
Differential Input Voltage	6V	Lead Temperature	
Peak Output Current	75 mA per amplifier	DIP package (soldering <5 sec.)	300°C
Power Dissapation	See Curves	SO package (vapor phase 60 sec.)	215°C
		Infrared (15 sec.)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±5V, R_L = 1 KΩ, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	EL2210C/EL2410C				Units
			Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage			10	20	I	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)		−25		V	µV/°C
I_B	Input Bias Current		−15	−7	−3	I	µA
I_{OS}	Input Offset Current			0.5	1.5	I	µA
TCI_{OS}	Average Offset Current Drift	(Note 2)		−7		V	nA/°C
A_{VOL}	Open-Loop Gain	V_{OUT} = ±2V, R_L = 1 KΩ	160	250		I	V/V
		V_{OUT} = +2V/0V, R_L = 150Ω	160	250		V	
PSRR	Power Supply Rejection	V_S = ±4.5V to ±5.5V	50	60		I	dB
CMRR	Common Mode Rejection	V_{CM} = ±2.4V, V_{OUT} = 0V	60	80		I	dB
CMIR	Common Mode Input Range	V_S = ±5V		−5/+3		V	V
V_{OUT}	OutputVoltage Swing	R_L = R_F = 1 KΩ R_L to Gnd	−2.5	−3, 3	2.7	I	V
		R_L = R_F = 1 KΩ +150Ω to Gnd	−0.45	−0.6, 2.9	2.5	I	
		R_L = R_F = 1 KΩ R_L to V_{EE}	−4.95		3	V	
I_{SC}	Output Short Circuit Current	Output to Gnd (Note 1)	75	125		I	mA
I_S	Supply Current	No Load (per channel)	5.5	6.8	8.5	I	mA
R_{IN}	Input Resistance	Differential		150		V	KΩ
		Common Mode		1.5		V	MΩ
C_{IN}	Input Capacitance	A_V = +1 @ 10 MHz		1		V	pF
R_{OUT}	Output Resistance			0.150		V	Ω
PSOR	Power Supply Operating Range	Dual Supply	±4.5		±6.5	V	V
		Single Supply	9		13	V	

DC Electrical Characteristics $V_S = \pm 5V$, $R_L = 1\ K\Omega$, $A_V = +2$, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	EL2211C/EL2411C				Units
			Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage			5	10	I	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)		−25		V	µV/°C
I_B	Input Bias Current		−15	−7	−3	I	µA
I_{OS}	Input Offset Current			0.5	1.5	I	µA
TCI_{OS}	Average Offset Current Drift	(Note 2)		−7		V	nA/°C
A_{VOL}	Open-Loop Gain	$V_{OUT} = \pm 2V$, $R_L = 1\ K\Omega$	250	380		I	V/V
		$V_{OUT} = +2V/0V$, $R_L = 150\Omega$	250	380		V	
PSRR	Power Supply Rejection	$V_S = \pm 4.5V$ to $\pm 5.5V$	55	68		I	dB
CMRR	Common Mode Rejection	$V_{CM} = \pm 2.5V$, $V_{OUT} = 0V$	70	90		I	dB
CMIR	Common Mode Input Range	$V_S = \pm 5V$		−5/+3		V	V
V_{OUT}	Output Voltage Swing	$R_L = R_F = 1\ K\Omega$ R_L to Gnd	2.5	−3.5, 3.3	2.7	I	V
		$R_L = R_F = 1\ K\Omega + 150\Omega$ to Gnd	−0.45	−0.6, 2.9	2.5	I	
		$R_L = R_F = 1\ K\Omega$ R_L to V_{EE}	−4.95		3	V	
I_{SC}	Output Short Circuit Current	Output to Gnd (Note 1)	75	125		I	mA
I_S	Supply Current	No Load	5.5	6.8	8.5	I	mA
R_{IN}	Input Resistance	Differential		150		V	KΩ
		Common Mode		1.5		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$ @ 10 MHz		1		V	pF
R_{OUT}	Output Resistance			0.150		V	Ω
PSOR	Power Supply Operating Range	Dual Supply	±4.5		6.5	V	V
		Single Supply	9		13	V	

Closed-Loop AC Characteristics V_S = ±5V, AC Test Figure 1, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	EL2210C/EL2410C				Units
			Min.	Typ.	Max.	Test Level	
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +1		110		V	MHz
BW	±0.1 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +1		12		V	MHz
GBWP	Gain Bandwidth Product			55		V	MHz
PM	Phase Margin			60		V	(°)
SR	Slew Rate		85	130		V	V/µs
FBWP	Full Power Bandwidth	(Note 3)	8	11		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step		2		V	ns
OS	Overshoot	0.1V Step		15		V	%
t_{PD}	Propagation Delay			3.5		V	ns
t_S	Settling to 0.1% (A_V = 1)	V_S = ±5V, 2V Step		80		V	ns
d_G	Differential Gain (Note 4)	NTSC/PAL		0.1		V	%
d_P	Differential Phase (Note 4)	NTSC/PAL		0.2		V	(°)
e_N	Input Noise Voltage	10 KHz		15		V	nV/rt (Hz)
i_N	Input Noise Current	10 KHz		1.5		V	pA/rt (Hz)
CS	Channel Separation	P = 5 MHz		55		V	dB

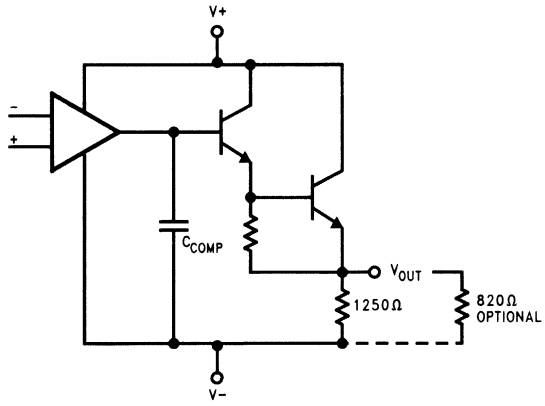
Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: Measured from T_{MIN} to T_{MAX}
Note 3: For V_S = ±5V, V_{OUT} = 4 V_{PP}. Full power bandwidth is based on slew rate measurement using:
FPBW = SR/(2pi * V_{peak})
Note 4: Video performance measured at V_S = ±5V, A_V = +2 with 2 times normal video level across R_L = 150Ω.

Closed-Loop AC Characteristics V_S = ±5V, AC Test Figure 1, Temp. = 25°C unless otherwise noted

Parameter	Description	Conditions	EL2211C/EL2411C				Units
			Min	Typ	Max	Test Level	
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +2		100		V	MHz
BW	±0.1 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	A_V = +2		8		V	MHz
GBWP	Gain Bandwidth Product			130		V	MHz
PM	Phase Margin			60		V	(°)
SR	Slew Rate		100	140		V	V/µs
FBWP	Full Power Bandwidth	(Note 3)	8	11		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step		2.5		V	ns
OS	Overshoot	0.1V Step		6		V	%
t_{PD}	Propagation Delay			3.5		V	ns
t_S	Settling to 0.1% (A_V = 1)	V_S = ±5V, 2V Step		80		V	ns
d_G	Differential Gain (Note 4)	NTSC/PAL		0.04		V	%
d_P	Differential Phase (Note 4)	NTSC/PAL		0.15		V	(°)
e_N	Input Noise Voltage	10 KHz		15		V	nV/rt (Hz)
i_N	Input Noise Current	10 KHz		1.5		V	pA/rt (Hz)
CS	Channel Separation	P = 5 MHz		55		V	dB

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: Measured from T_{MIN} to T_{MAX}
Note 3: For V_S = ±5V, V_{OUT} = 4 V_{PP}. Full power bandwidth is based on slew rate measurement using:
FPBW = SR/(2pi * V_{peak})
Note 4: Video performance measured at V_S = ±5V, A_V = +2 with 2 times normal video level across R_L = 150Ω.

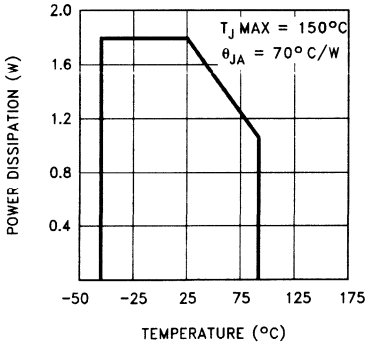
Simplified Block Diagram



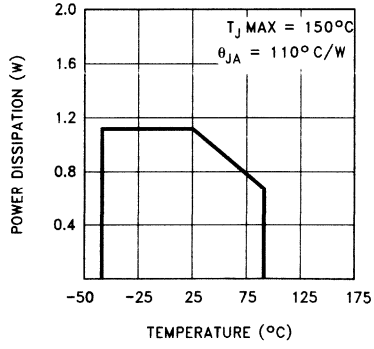
2210-3

Typical Performance Curves

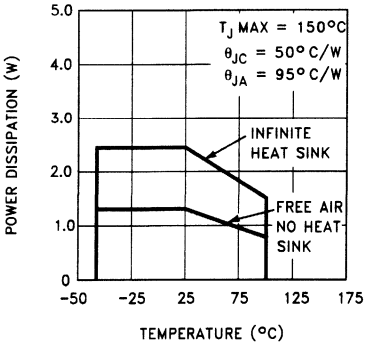
14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



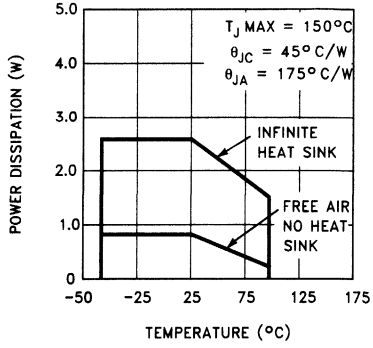
14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



2210-4

Application Information

Product Description

The EL2210 and EL2410 are dual and quad operational amplifiers stable at a gain of 1. The EL2211 and the EL2411 are dual and quad operational amplifiers stable at a gain of 2. All four are built on Elantec's proprietary complimentary process and share the same voltage mode feedback topology. This topology allows them to be used in a variety of applications where current mode feedback amplifiers are not appropriate because of restrictions placed on the feedback elements. These products are especially designed for applications where high bandwidth and good video performance characteristics are desired but the higher cost of more flexible and sophisticated products are prohibitive.

Power Supplies

These amplifiers are designed to work at a supply voltage difference of 10V to 12V. These amplifers will work on any combination of ± supplies. All Electrical characteristics are measured with ±5V supplies. Below 9V total supply voltage the amplifiers' performance will degrade dramatically. The quiescent current is a direct function of total supply voltage. With a total supply voltage of 12V the quiescent supply current will increase from a typical 6.8 mA per amplifier to 8.5 mA per amplifer.

Output Swing vs Load

Please refer to the simplified block diagram. These amplifiers provide an NPN pull-up transistor output and a passive 1250Ω pull-down resistor to the most negative supply. In an application where the load is connected to V_S- the output voltage can swing to within 200 mV of V_S-. In split supply applications where the DC load is connected to ground the negative swing is limited by the voltage divider formed by the load, the internal 1250Ω resistor and any external pull-down resistor. If R_L were 150Ω then it and the 1250Ω internal resistor limit the maximum negative swing to (V_{EE}(150/1250+150)) or −0.53V. The negative swing can be increased by adding an external resistor of appropriate value from the output to the negative supply. The simplified block diagram shows an 820Ω external pull-down resistor. This resistor is in parallel with the internal 1250Ω resistor. This will increase the negative swing to V_{EE} (150/((1250 * 820/(1250 + 820) + 150) or −1.16V.

Power Dissipation and Loading

Without any load and a 10V supply difference the power dissipation is 70 mW per amplifier. At 12V supply difference this increases to 105 mW per amplifier. At 12V this translates to a junction temperature rise above ambient of 33° for the dual and 40° for the quad amplifier. When the amplifiers provide load current the power dissipation can rapidly rise.

In ±5V operation each output can drive a grounded 150Ω load to more than 2V. This operating condition will not exceed the maximum junction temperature limit as long as the ambient temperature is below 85°C, the device is soldered in place, and the extra pull-down resistor is 820Ω or more.

If the load is connected to the most negative voltage (ground in single supply operation) you can easily exceed the absolute maximum die temperature. For example the maximum die temperature should be 150°C. At a maximum expected ambient temperature of 85°C, the total allowable power dissipation for the SO-8 package would be:

$P_D = (150 - 75)/180°C/W = 416\ mW$

At 12V total supply voltage each amplifier draws a maximum of 8.5 mA and dissipates 12V * 8.5 mA = 100 mW or 200 mW for the dual amplifier. Which leaves 216 mW of increased power due to the load. If the load were 150Ω connected to the most negative voltage and the maximum voltage out were V_S- +2V the load current would be 13 mA. Then an extra 266 mW ((12V − 2V) * 13.3 mA * 2) would be dissipated in the EL2210 or EL2211. The total dual amplifier power dissipation would be 266 mW + 200 mW = 466 mW, more than the maximum 416 mW allowed. If the total supply difference were reduced to 10V, the same calculations would yield 170 mW quiescent power dissipation and 213 mW due to loading. This results in a die temperature of 143°C (75°C + 69°C).

In the above example, if the supplies were split ±6V and the 150Ω loads were connected

Application Information — Contd.

to ground, the load induced power dissipation would drop to 106 mW (13.3 mA * (6 − 2) * 2) and the die temperature would be below the rated maximum.

Video Performance

Following industry standard practices (see EL2044 applications section) these four devices exhibit good differential gain (dG) and good differential phase (dP) with ±5V supplies and an external 820Ω resistor to the negative supply, in a gain of 2 configuration, driving 75Ω back terminated cables to standard video levels (1.428V at the amplifier) the EL2210 and EL2410 have dG of 0.1% and dP of 0.2°. The EL2211 and the EL2411 have dG of 0.04% and dP of 15°.

Due to the negative swing limitations described above, inverted video at a gain of 2 is just not practical. If swings below ground are required then changing the extra 820Ω resistor to 500Ω will allow reasonable dG and dP to approximately −0.75 mV. The EL2211 and EL2411 will achieve approximately 0.1%/0.4° between 0V and −0.75V. Beyond −0.75V dG and dP get worse by orders of magnitude.

Differential gain and differential phase are fairly constant for all loads above 150Ω. Differential phase performance will improve by a factor of 3 if the supply voltage is increased to ±6V.

Output Drive Capability

None of these devices have short circuit protection. Each output is capable of more than 100 mA into an shorted output. Care must be used in the design to limit the output current with a series resistor.

Printed-Circuit Layout

The EL2210C/EL2211C/EL2410C/EL2411C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 KΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2223C

Dual, 500 MHz High Speed, Operational Amplifier

Features

- Wide gain bandwidth—500 MHz
- High slew rate—350 V/μs
- High power bandwidth (± 10 V_{out}) 5.5 MHz
- Large open loop gain 83 dB
- Low power—5 mA/amplifier
- Low input offset—0.5 mV typ.
- Wide supply voltage range $V_S = \pm 5V$ to $\pm 15V$
- Output short circuit protected

Applications

- High performance active filters
- Video and pulse amplifiers
- Local area networks
- Wideband amplifiers
- Replace two HA2540s

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2223CN	0°C to +75°C	P-DIP	MDP0031
EL2223CM	0°C to +75°C	SOL	MDP0027

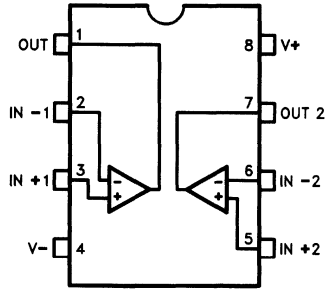
General Description

The EL2223 monolithic dual operational amplifier is an extension of Elantec's position in high speed analog products. This patented amplifier features 350 V/μs slew rate, a 500 MHz gain bandwidth gain-of-10 stable, along with an excellent speed power relationship. The dual 500 MHz EL2223 consumes only 10 mA, making it ideal for HA2540 type applications. The EL2223 has short-circuit-protected outputs and will operate from $\pm 5V$ to $\pm 15V$. It is fabricated using Elantec's complementary bipolar process which allows both fast PNP and NPN transistors to be manufactured on a single chip.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *"Elantec's Processing, Monolithic Integrated Circuits"*.

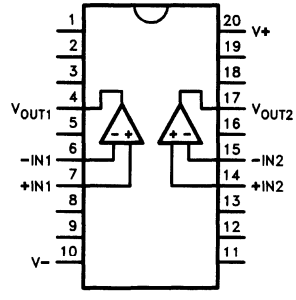
Connection Diagrams

EL2223CN



2223-1

EL2223CM



2223-3

This product covered under U.S. Patent No. 4,837,523

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	±6V	Maximum Junction Temperature	150°C
Internal Power Dissipation	See Curves	Lead Temperature	
Peak Output Current	Short Circuit Protected	DIP Package	300°C
Output Short Circuit Duration (Note 1)	Continuous	SOL Package	
		Vapor Phase (60 seconds)	215°C
Operational Temperature Range	0°C to +75°C	Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2223C				Units
			Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	+25°C Full		0.5	5 8	I III	mV mV
TCV_{OS}	Average Offset Voltage Drift	Full		3		V	µV/°C
I_B	Bias Current	+25°C Full		1.5	4 6	I III	µA µA
I_{OS}	Offset Current	+25°C Full		0.2	2 3	I III	µA µA
R_{IN}	Input Resistance	+25°C		6		V	kΩ
C_{IN}	Input Capacitance	+25°C		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±12		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	+25°C		7		7	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	+25°C Full	20k 10k	40k		I III	V/V V/V

EL2223C
Dual, 500 MHz High Speed, Operational Amplifier

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified — Contd.

Parameter	Description	Temp	EL2223C				Units
			Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	90		II	dB
V_O	Output Voltage Swing	Full	±11	±12.5		II	V
I_{SC}	Short Circuit Current	+25°C		±50	±70	I	mA
R_O	Output Resistance	+25°C		40		V	Ω
I_s	Supply Current	Full		9.5	13	II	mA
PSRR	Power Supply Rejection Ratio (Note 5)	Full	70	90		II	dB

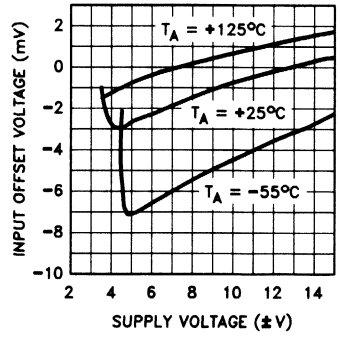
AC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2223C				Units
			Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	+25°C		500		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 7)	+25°C	3.98	5.5		I	MHz
t_r	Rise Time (Note 8)	+25°C		7		V	ns
OS	Overshoot (Note 8)	+25°C		30		V	%
SR	Slew Rate (Note 8)	+25°C	250	350		I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.05%	+25°C		330		V	ns
Ch S_p	Channel Separation (f = 10 MHz)			70		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: V_O = ±10V.
Note 3: RL = 2 kΩ.
Note 4: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 5: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 6: V_O = 100 mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/ $2\pi V_{peak}$.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurement are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN September 19, 1985.
Note 10: A_V = +10, R_L = 2 kΩ.

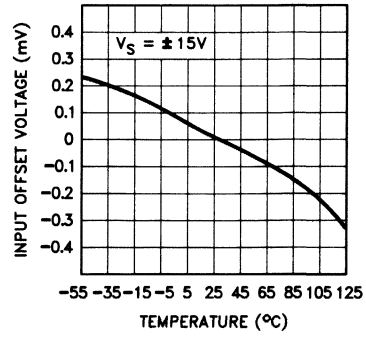
Typical Performance Curves

Input Offset Voltage vs Supply Voltage



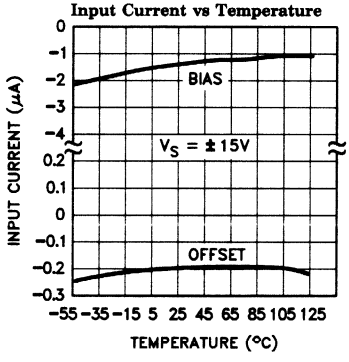
2223-4

Normalized Input Offset Voltage vs Temperature



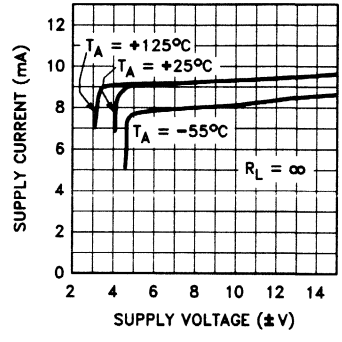
2223-5

Input Current vs Temperature



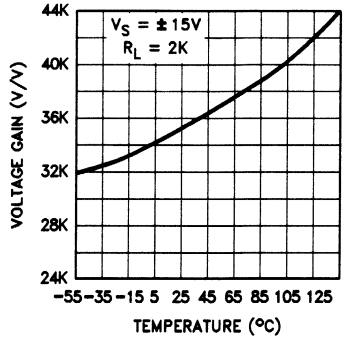
2223-6

Supply Current vs Supply Voltage



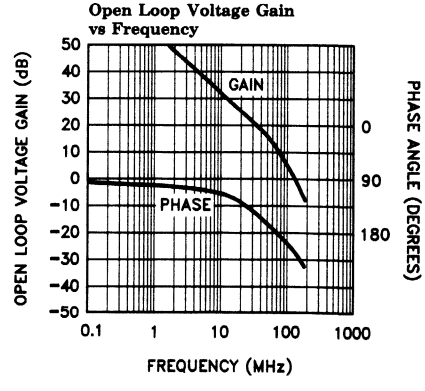
2223-7

Voltage Gain vs Temperature



2223-8

Open Loop Voltage Gain vs Frequency

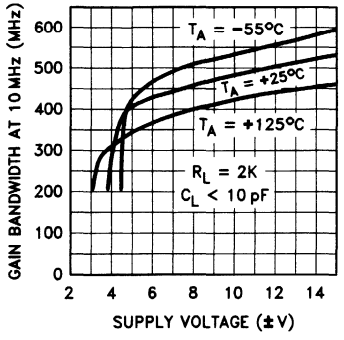


2223-9

EL2223C
Dual, 500 MHz High Speed, Operational Amplifier

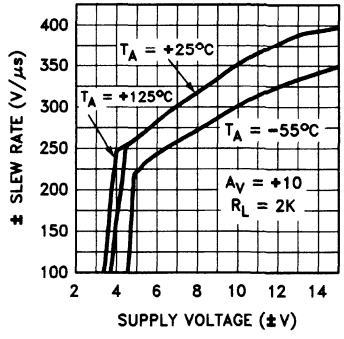
Typical Performance Curves — Contd.

Gain Bandwidth at 10 MHz vs Supply Voltage



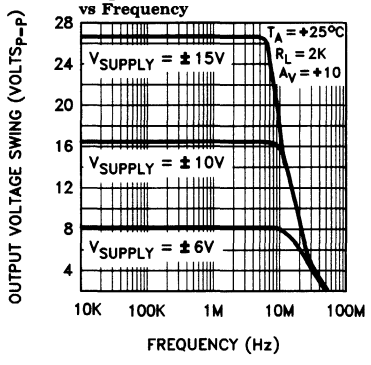
2223-10

Slew Rate vs Supply Voltage



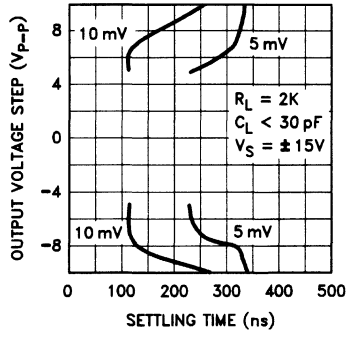
2223-11

Output Voltage Swing vs Frequency



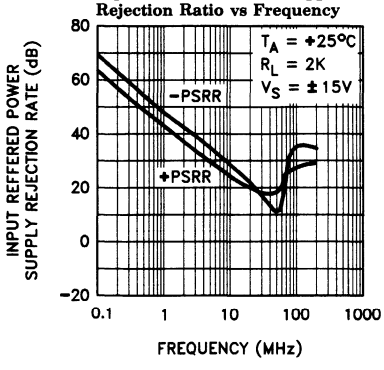
2223-12

Settling Time A_V = +10



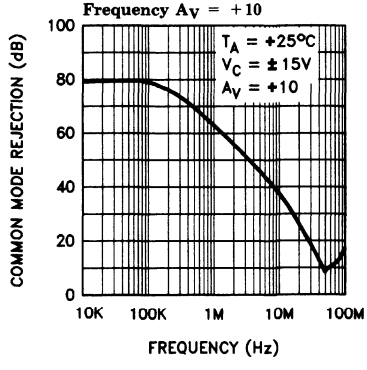
2223-13

Input Referred Power Supply Rejection Ratio vs Frequency



2223-14

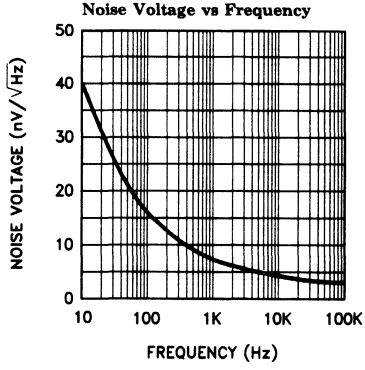
Common Mode Rejection vs Frequency A_V = +10



2223-15

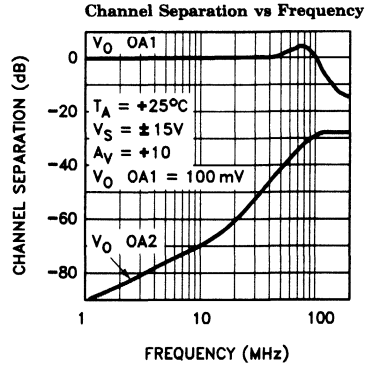
Typical Performance Curves — Contd.

Noise Voltage vs Frequency



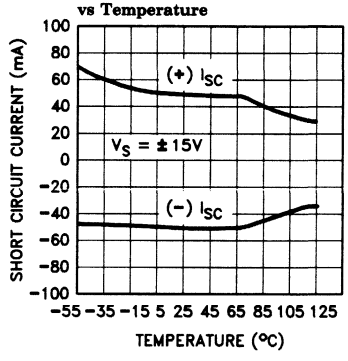
2223-16

Channel Separation vs Frequency



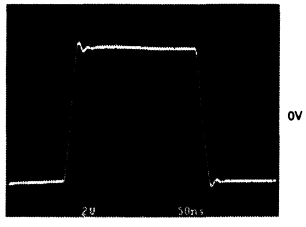
2223-17

Short Circuit Current vs Temperature



2223-18

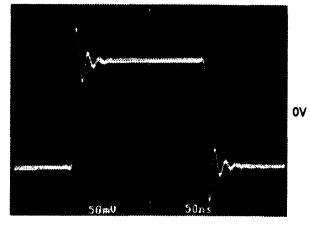
Large Signal Response



A_V = +10
V_{IN} = ±0.5V
V_O = ±5V
R_L = 2k

2223-19

Small Signal Response



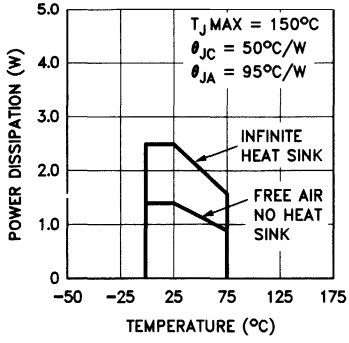
A_V = +10
V_{IN} = ±10 mV
V_O = ±100 mV
R_L = 2k

2223-20

EL2223C
Dual, 500 MHz High Speed, Operational Amplifier

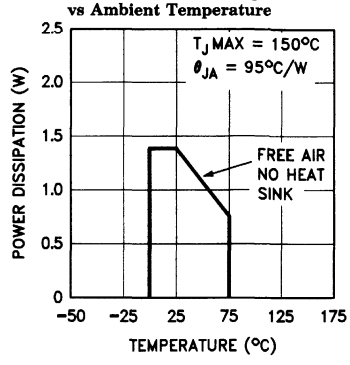
Typical Performance Curves — Contd.

8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



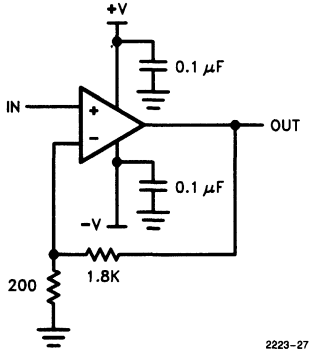
2223-22

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2223-24

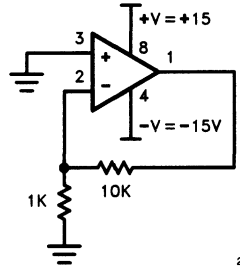
Test Circuit



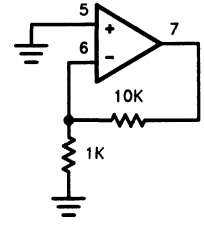
2223-27

A_V = +10
$C_L \leq$ 10 pF Scope Probe

Burn-In Circuit



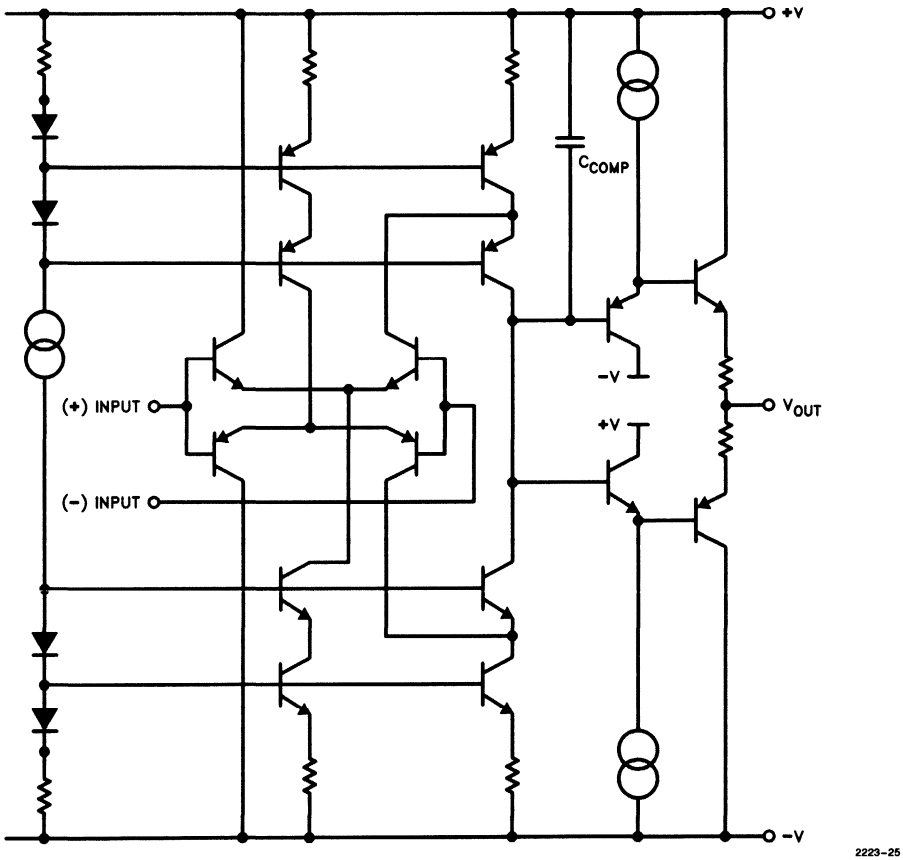
2223-28



2223-29

Pin numbers are for the 8-Lead CerDIP.
Burn-in circuit is identical for all package types.

Simplified Schematic (one amplifier)

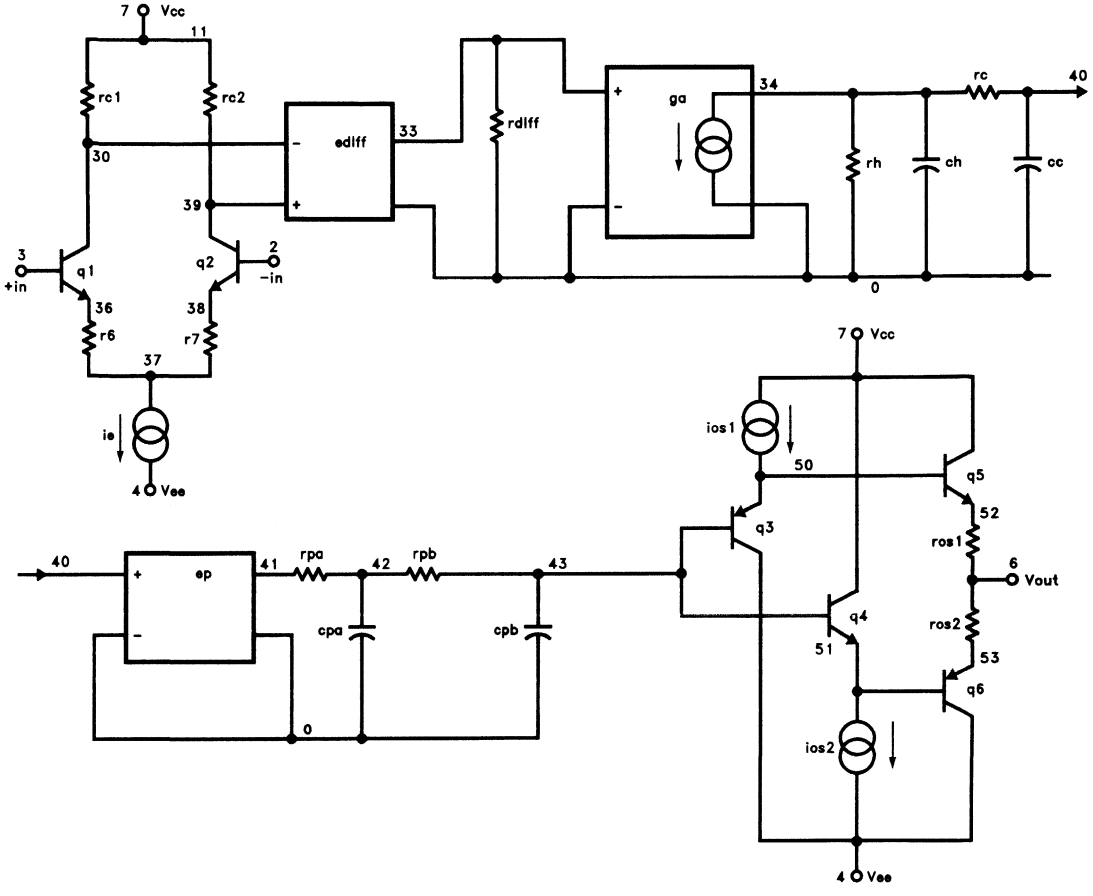


EL2223C
Dual, 500 MHz High Speed, Operational Amplifier

EL2223 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2233       3     2     7     4     6
* Input stage
ie 37 4 2mA
r6 36 37 60
r7 38 37 60
rc1 7 30 75
rc2 7 39 75
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 7.25
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 2.6m
rh 34 0 3Meg
ch 34 0 1.5pF
rc 34 40 600
cc 40 0 7pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 25pF
rpb 42 43 50
cpb 43 0 15pF
* Output Stage
ios1 7 50 1.25mA
ios2 51 4 1.25mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
* models
.model qn npn (is=800.0E-18 bf=250 tf=0.2nS)
.model qna npn (is=864E-18 bf=300 tf=0.2nS)
.model qp pnp (is=800E-18 bf=60 tf=0.2nS)
.ends
```

EL2223 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2224C

Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

Features

- Unity gain stable
- Wide bandwidth—60 MHz
- High slew rate—200 V/μs
- High power bandwidth (± 10 V_{out}) 3 MHz
- Large open loop gain 75 dB
- Low power—5 mA/amplifier
- Low input offset—1 mV typ.
- Wide supply voltage range $V_S = \pm 5V$ to $\pm 15V$
- Output short circuit protected

Applications

- High performance active filters
- Video and pulse amplifiers
- Local area networks
- Wideband amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2224CN	0°C to +75°C	P-DIP	MDP0031
EL2224CM	0°C to +75°C	SOL	MDP0027

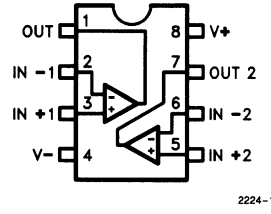
General Description

The EL2224 monolithic dual operational amplifier is an extension of Elantec's position in high speed analog products. This amplifier features unity gain stability, high slew rate and wide bandwidth, along with an excellent speed power relationship. The dual 60 MHz EL2224 consumes only 10 mA, making it ideal for video applications. The EL2224 has short circuit protected outputs and will operate from $\pm 5V$ to $\pm 15V$. It is fabricated using Elantec's Complementary Bipolar process which allows both fast PNP and NPN transistors to be manufactured on a single chip.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *"Elantec's Processing, Monolithic Integrated Circuits"*.

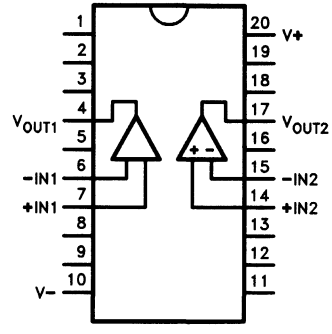
Connection Diagrams

EL2224CN



2224-1

EL2224CM



2224-3

This product covered under U.S. Patent No. 4,837,523

EL2224C

Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage Between V+ and V−	35V	Operational Temperature Range	0°C to +75°C
Differential Input Voltage	±6V	Storage Temperature Range	−65°C to +150°C
Internal Power Dissipation	See Curves	Maximum Junction Temperature	
Peak Output Current	Short Circuit Protected	Plastic DIP, SOL	150°C
Output Short Circuit Duration (Note 1)	Continuous	Lead Temperature	
		DIP Package	300°C
		SOL Package	
		Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

Test Level

All parameters listed in the Electrical Specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance. Military grade parts are electrical tests using maximum high-speed automatic test equipment, generally per MIL-STD-883 Rev. C methods. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	EL2224C				Units
		Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage		0.5	5 8	I III	mV mV
TCV_{OS}	Average Offset Voltage Drift		20		V	µV/°C
I_B	Bias Current		1.5	4 6	I III	µA µA
I_{OS}	Offset Current		0.2	2 3	I III	µA µA
R_{IN}	Input Resistance		40		V	kΩ
C_{IN}	Input Capacitance		1		V	pF
V_{CM}	Common Mode Input Range	±10	±12		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)		15		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	4k 2.5k	6k		I III	V/V V/V

EL2224C
Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified — Contd.

Parameter	Description	EL2224C				Units
		Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio (Note 4)	60	80		II	dB
V_O	Output Voltage Swing	±11	±12.5		II	V
I_{SC}	Short Circuit Current		±50	±70	I	mA
R_O	Output Resistance		40		V	Ω
I_s	Supply Current		9.5	13	II	mA
PSRR	Power Supply Rejection Ratio (Note 5)	60	75		II	dB

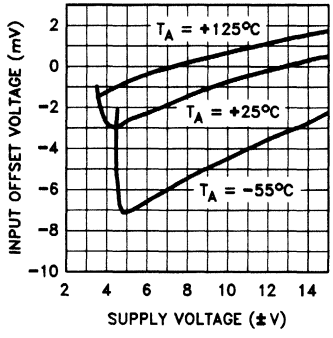
AC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	EL2224C				Units
		Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)		60		V	MHz
FPBW	Full Power Bandwidth (Notes 2, 7)	2.4	3.1		I	MHz
t_r	Rise Time (Note 8)		6		V	ns
OS	Overshoot (Note 8)		20		V	%
SR	Slew Rate (Note 8)	150	200		I	V/μs
t_s	Settling Time (Notes 9, 10) 10V Step to 0.05%		120		V	ns
Ch S_p	Channel Separation (f = 10 MHz)		70		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: V_O = ±10V.
Note 3: R_L = 2 kΩ.
Note 4: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0 to −10V.
Note 5: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 6: V_O = 100 mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/ 2 π V_{PEAK}.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurement are made with techniques in the following reference: "Take The Guesswork Out of Settling-Time Measurements," EDN September 19, 1985.
Note 10: A_V = + 1, R_L = 2 kΩ.

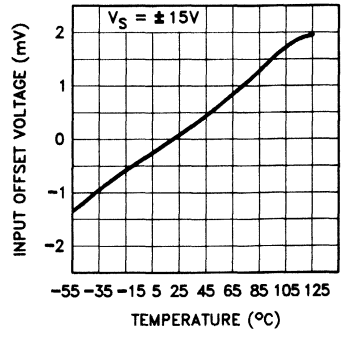
Typical Performance Curves

Input Offset Voltage vs Supply Voltage



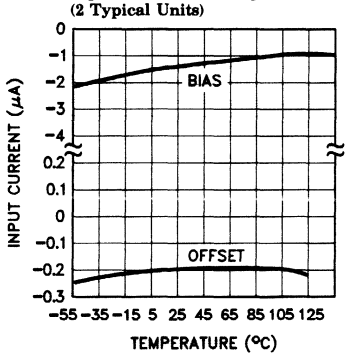
2224-4

Normalized Input Offset Voltage vs Temperature



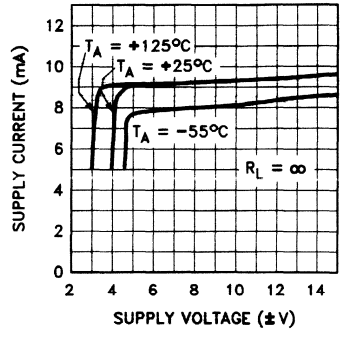
2224-5

Input Current vs Temperature (2 Typical Units)



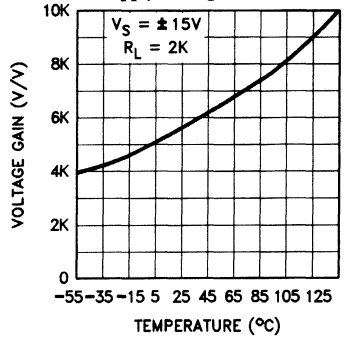
2224-6

Supply Current vs Supply Voltage



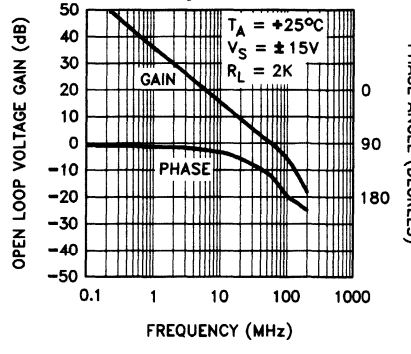
2224-7

Voltage Gain vs Supply Voltage



2224-8

Open Loop Voltage Gain vs Frequency

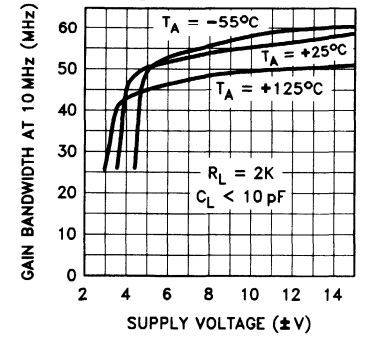


2224-9

EL2224C
Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

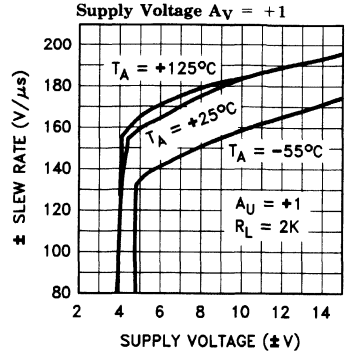
Typical Performance Curves — Contd.

Gain Bandwidth at 10 MHz vs Supply Voltage



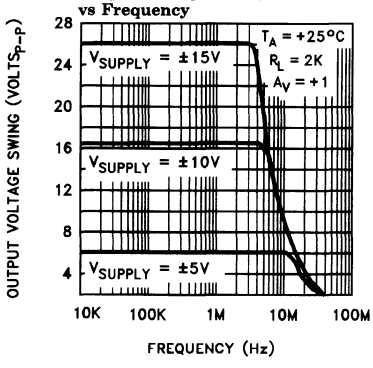
2224-10

Slew Rate vs Supply Voltage A_V = +1



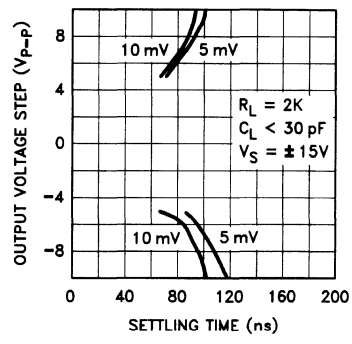
2224-11

Output Voltage Swing vs Frequency



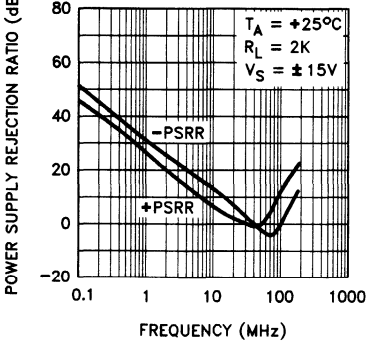
2224-12

Settling Time A_V = +1



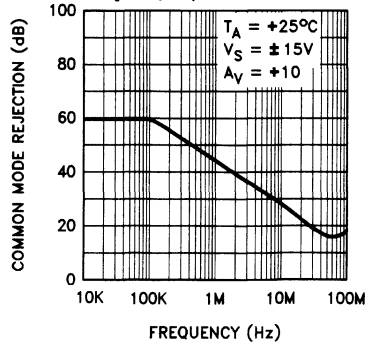
2224-13

Power Supply Rejection Ratio vs Frequency



2224-14

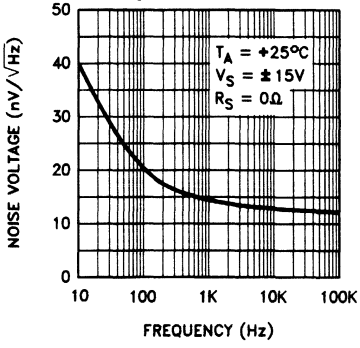
Common Mode Rejection vs Frequency A_V = +10



2224-15

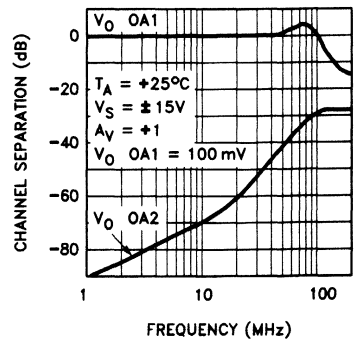
Typical Performance Curves — Contd.

Noise Voltage vs Frequency



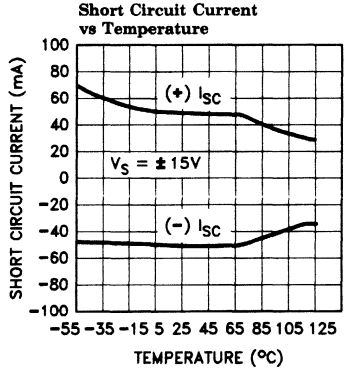
2224-16

Channel Separation vs Frequency



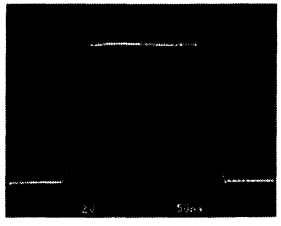
2224-17

Short Circuit Current vs Temperature



2224-18

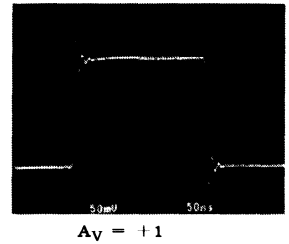
Large Signal Response



A_V = +1
V_{IN} = ±5V
V_O = ±5V
R_L = 2k

2224-19

Small Signal Response



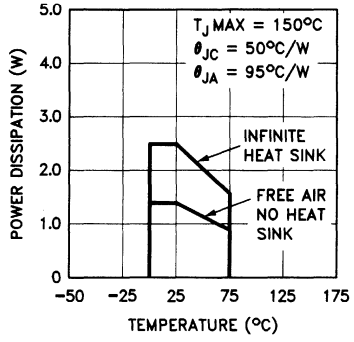
A_V = +1
V_{IN} = ±100 mV
V_O = ±100 mV
R_L = 2k

2224-20

EL2224C
Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

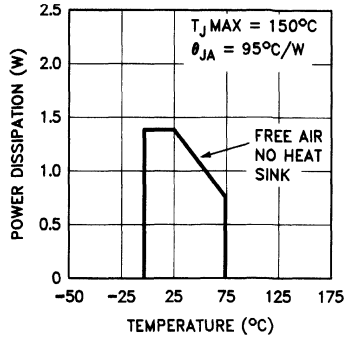
Typical Performance Curves — Contd.

8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



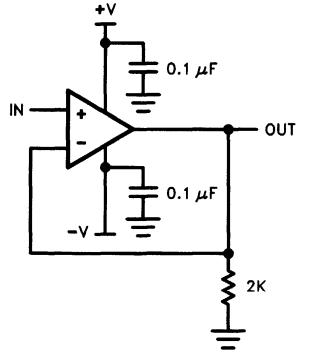
2224-22

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2224-24

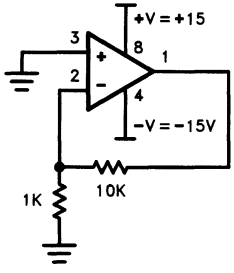
Test Circuit



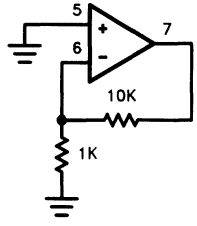
2224-27

A_V = +1
$C_L \leq$ 10 pF Scope Probe

Burn-In Circuit



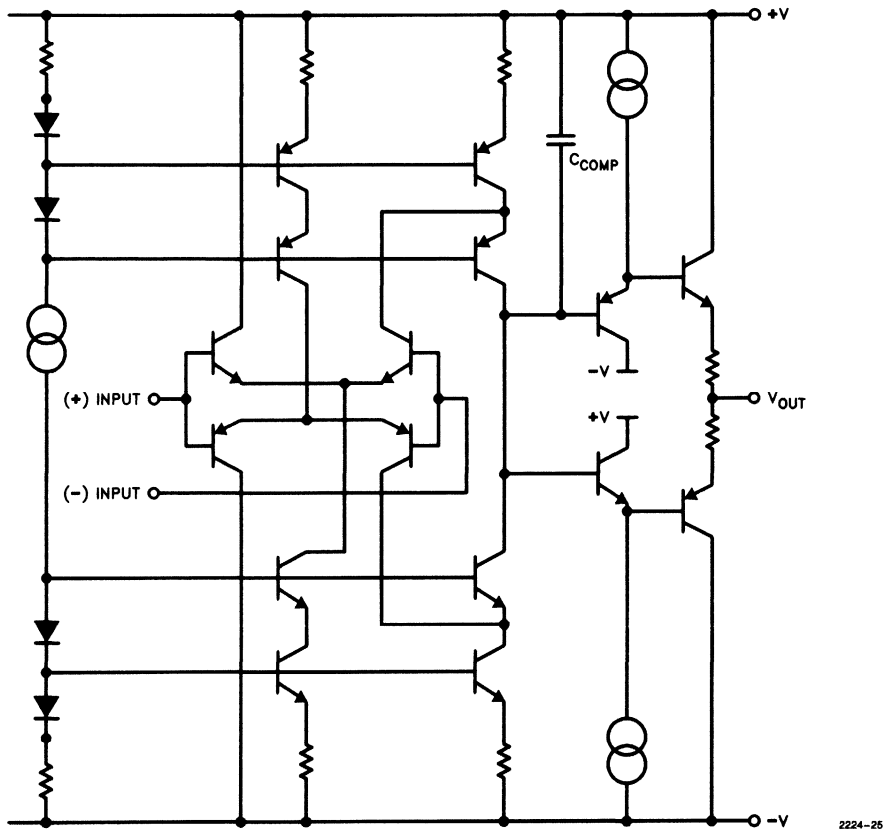
2224-28



2224-29

Pin numbers are for the 8-lead CerDIP.
Burn-in circuit is identical for all package types.

Simplified Schematic (one amplifier)

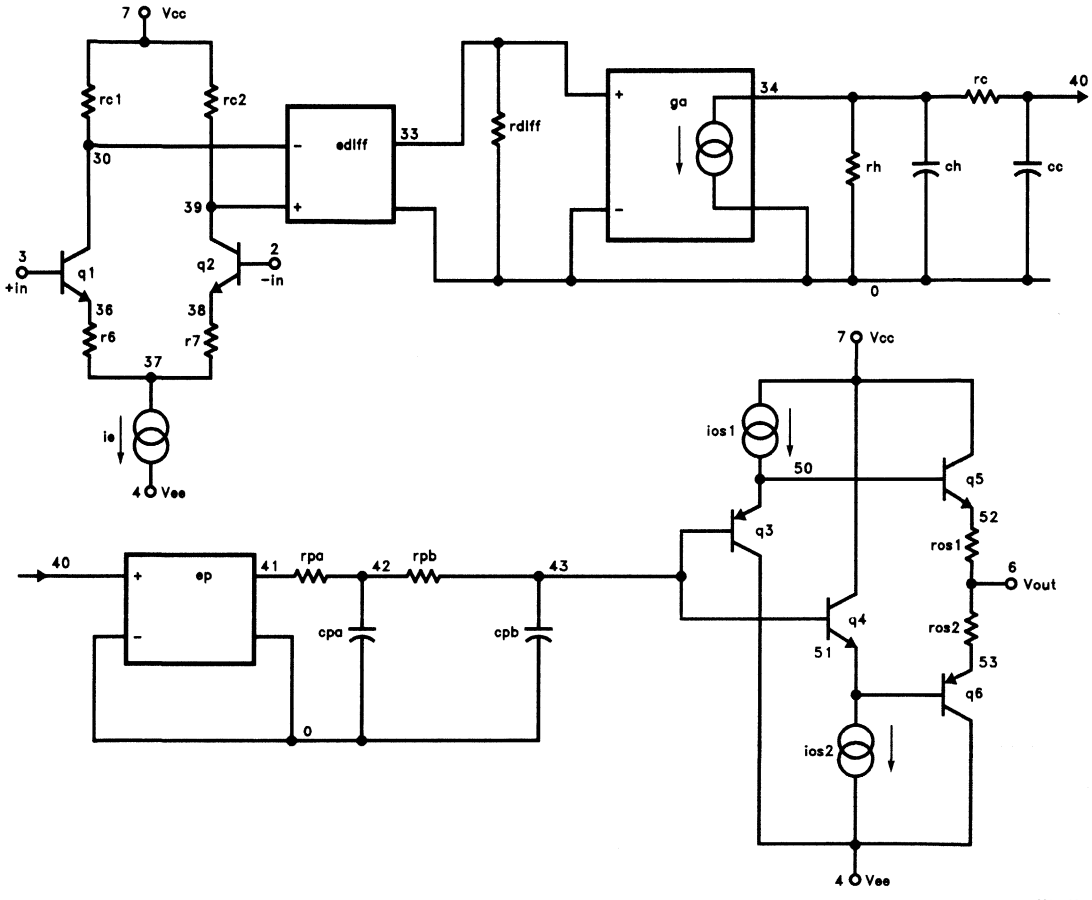


EL2224C
Dual, 60 MHz, Unity Gain Stable, Operational Amplifier

EL2224 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2224        3     2     7     4     6
* Input stage
ie 37 4 4.5mA
r6 36 37 75
r7 38 37 75
rc1 7 30 75
rc2 7 39 75
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 2.6
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 3m
rh 34 0 1Meg
ch 34 0 15pF
rc 34 40 300
cc 40 0 1pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 3pF
rpb 42 43 50
cpb 43 0 3pF
* Output Stage
ios1 7 50 0.5mA
ios2 51 4 0.5mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
* models
.model qn npn(is=800.0E-18 bf=350 tf=0.2nS)
.model qna npn(is=864E-18 bf=400 tf=0.2nS)
.model qp pnp(is=800E-18 bf=60 tf=0.2nS)
.ends
```

EL2224 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2232C

60 MHz, Fast Settling, Dual Current Feedback Amplifier

Features

- 60 MHz −3 dB bandwidth, $A_V = 1$
- 50 MHz −3 dB bandwidth, $A_V = 2$
- 3 mV offset voltage
- 10 μV/°C Offset Drift
- 600 V/μs Slew Rate
- 30 mA output current
- Drives ±12.5 into 500Ω load
- Characterized at ±5V and ±15V
- 9.5 mA supply current
- 125 ns settling time to 0.02% for 10V step
- Output short circuit protected
- Low cost
- Dual version of the EL2020

Applications

- Video amplifiers
- Video distribution amplifiers
- Fast, precise D/A converter output amplifier
- High speed A/D input amplifier
- CCD imager amplifier
- Ultrasound and sonar systems

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2232CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2232CM	0°C to +75°C	16-Lead SOL	MDP0027

General Description

The EL2232 is a dual monolithic operational amplifier with a 60 MHz unity gain bandwidth. Built using Elantec's in-house high speed bipolar process, the dual amplifier uses current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier. The EL2232 design was optimized to achieve fast rise and fall times and short settling times.

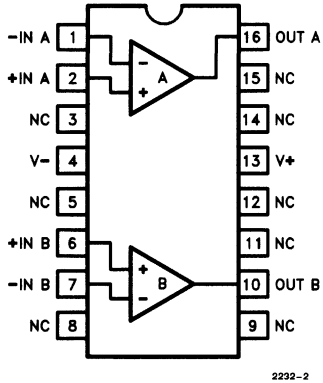
The EL2232 is a dual version of the popular EL2020, demonstrating similar AC performance, yet the 2 amplifiers of the EL2232 consume no more power than a single EL2020.

The EL2232 operates on standard ±15V supplies, swings ±12.5V at its output into a 500Ω load. The EL2232 was designed and is characterized to operate with supply voltages between ±5V and ±15V. Its low power consumption and short circuit protection make the EL2232 a safe and reliable amplifier to be used in commercial, industrial and military applications where the part is available screened to MIL-STD-883.

Elantec's facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing—Monolithic Products.*

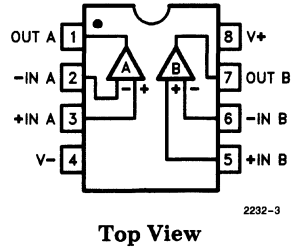
Connection Diagrams

SOL Package



Top View

Plastic DIP



Top View

EL2232C
60 MHz, Fast Settling, Dual Current Feedback Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V or 36V	T_J	Operating Junction Temperature	150°C
V_{IN}	Input Voltage	±15V or V_S	T_{ST}	Storage Temperature	−65°C to +150°C
ΔV_{IN}	Differential Input Voltage	±6V		Lead Temperature	
P_D	Maximum Power Dissipation	See Curves		DIP Package	
I_{IN}	Input Current	±10 mA		(Soldering, <10 seconds)	300°C
I_{OP}	Peak Output Current	Short Circuit Protected		SOL Package	
	Output Short Circuit Duration (Note 1)	Continuous		Vapor Phase (60 seconds)	215°C
				Infrared (15 seconds)	220°C
T_A	Operating Temperature Range	0°C to +75°C			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics V_S = ±15V, R_L = 500Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V	25°C		2	7	I	mV
			T_{MIN}, T_{MAX}			10	III	mV
dV_{OS}/dT	Offset Voltage Drift		Full		10		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		1.2	5	I	µA
			T_{MIN}, T_{MAX}			7.5	III	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		5	20	I	µA
			T_{MIN}, T_{MAX}			25	III	µA
$+R_{IN}$	+Input Resistance		Full	2	20		II	MΩ
C_{IN}	Input Capacitance		25°C		3		V	pF
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	Full	56	63		II	dB
−ICMR	Input Current Common-Mode Rejection (Note 2)		25°C		0.25	0.75	I	µA/V
			T_{MIN}, T_{MAX}			1	II	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		Full	66	80		II	dB
+IPSR	+Input Current Power Supply Rejection (Note 3)		25°C		0.03	0.06	II	µA/V
			T_{MIN}, T_{MAX}			0.1	III	µA/V
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.06	0.2	II	µA/V
			T_{MIN}, T_{MAX}			0.3	III	µA/V
R_{OL}	Transimpedance ($dV_{OUT}/d\text{-}I_{IN}$) (Note 4)	V_S = ±5V, ±15V	25°C	0.3	1.3		II	MΩ
			T_{MIN}, T_{MAX}	0.05			III	MΩ

EL2232C
60 MHz, Fast Settling, Dual Current Feedback Amplifier

Open Loop DC Electrical Characteristics

$V_S = \pm 15V$, $R_L = 500\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 500\Omega$	Full	11.5	12.5		II	V
		$V_S = \pm 5V$, $R_L = 500\Omega$	Full	2	2.5		II	V
I_{OUT}	Output Current	$V_S = \pm 15V$	Full	23	30		II	mA
		$V_S = \pm 5V$	Full		25		V	mA
I_S	Quiescent Supply Current		25°C		9.5	13	II	mA
			T_{MIN}, T_{MAX}			14	III	mA
I_{SC}	Short-Circuit Current	$V_S = \pm 15V$	25°C		50		V	mA
		$V_S = \pm 5V$	25°C		45		V	mA

Closed Loop AC Electrical Characteristics

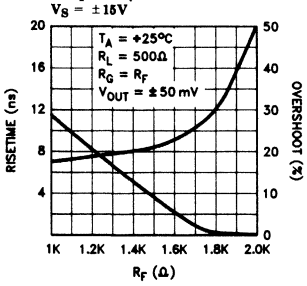
$V_S = \pm 15V$, $A_V = +1$, $R_F = 1.5k\Omega$, $R_L = 500\Omega$, $T_A = 25°C$

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 5)	$A_V = +1$	25°C	400	600		I	V/μs
		$A_V = +10$	25°C		650		V	Vμs
BW	−3 dB Bandwidth	$A_V = -1$	25°C		50		V	MHz
		$A_V = +1$	25°C		60		V	MHz
		$A_V = +10$	25°C		35		V	MHz
t_r, t_f	Rise Time, Fall Time	100 mV Step	25°C		8		V	ns
	$A_V = +1$, 10% to 90%	10V Step	25°C		21		V	ns
t_s	Settling Time (Note 6)	$A_V = -1$, 0.1%	25°C		85		V	ns
		0.02%	25°C		120		V	ns
		$A_V = +1$, 0.1%	25°C		85		V	ns
		0.02%	25°C		110		V	ns
		$A_V = +10$, 0.1%	25°C		85		V	ns
		0.02%	25°C		125		V	ns
CS	Channel Separation	100 kHz, $R_L = 1M\Omega$	25°C		100		V	dB
dG	Differential Gain (Note 7)	$R_L = 150\Omega$	25°C		0.1		V	% p-p
dPhase	Differential Phase (Note 7)	$R_L = 150\Omega$	25°C		0.1		V	° p-p

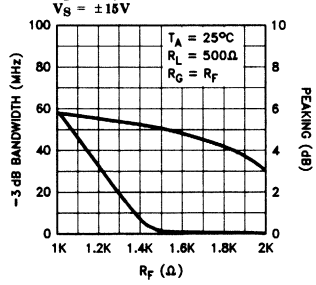
Note 1: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 2: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$. For $V_S = \pm 5V$, $V_{CM} = \pm 2V$.
Note 3: V_{OS} is measured at $V_S = \pm 4.5V$ and at $V_S = \pm 18V$. Both supplies are changed simultaneously.
Note 4: $R_L = 500\Omega$, $V_O = \pm 10V$ for $V_S = \pm 15V$, $V_O = \pm 2V$ for $V_S = \pm 5V$.
Note 5: $V_O = \pm 10V$, SR is tested at $V_O = \pm 5V$.
Note 6: Setting time measurement techniques are shown in: "Take The Guesswork Out of Settling Time Measurements", EDN, September 19, 1985. Available from the factory upon request.
Note 7: NTSC (3.58 MHz) and PAL (4.43 MHz). See Differential Gain and Phase Test Circuit.

Typical Performance Curves

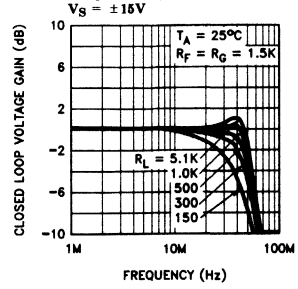
Rise Time and Overshoot vs R_F for $A_V = -1$, $V_S = \pm 15V$



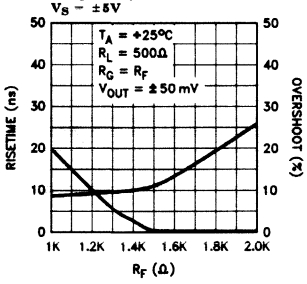
Bandwidth and Peaking vs R_F for $A_V = -1$, $V_S = \pm 15V$



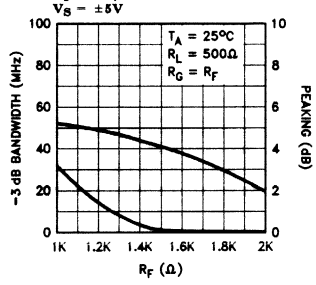
Voltage Gain vs Frequency $A_V = -1$, $V_S = \pm 15V$



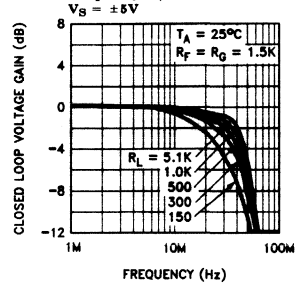
Rise Time and Overshoot vs R_F for $A_V = -1$, $V_S = \pm 5V$



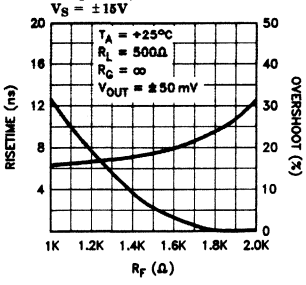
Bandwidth and Peaking vs R_F for $A_V = -1$, $V_S = \pm 5V$



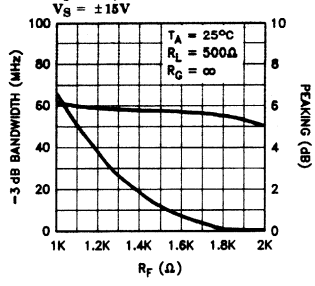
Voltage Gain vs Frequency $A_V = -1$, $V_S = \pm 5V$



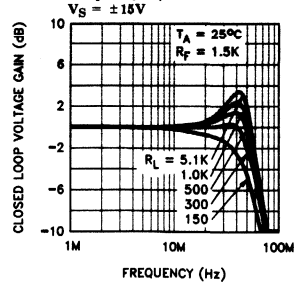
Rise Time and Overshoot vs R_F for $A_V = +1$, $V_S = \pm 15V$



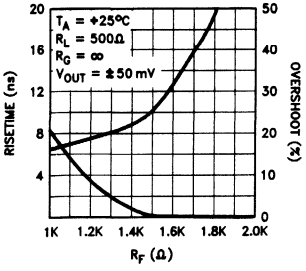
Bandwidth and Peaking vs R_F for $A_V = +1$, $V_S = \pm 15V$



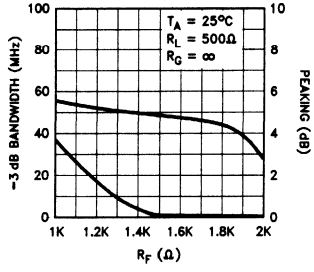
Voltage Gain vs Frequency $A_V = +1$, $V_S = \pm 15V$



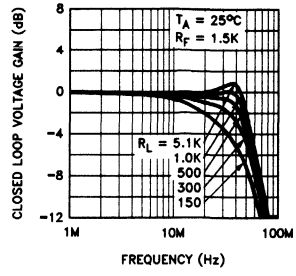
Rise Time and Overshoot vs R_F for $A_V = +1$, $V_S = \pm 5V$



Bandwidth and Peaking vs R_F for $A_V = +1$, $V_S = \pm 5V$



Voltage Gain vs Frequency $A_V = +1$, $V_S = \pm 5V$



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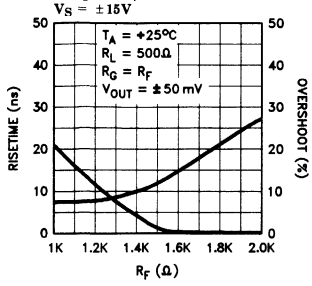
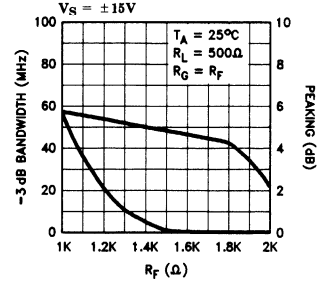
EL2232C
60 MHz, Fast Settling, Dual Current Feedback Amplifier

Typical Performance Curves — Contd.

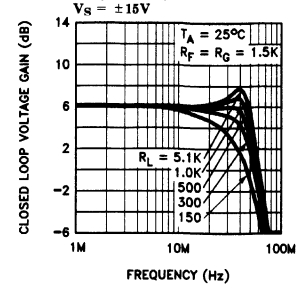
Rise Time and Overshoot vs R_F for A_V = +2, V_S = ±15V



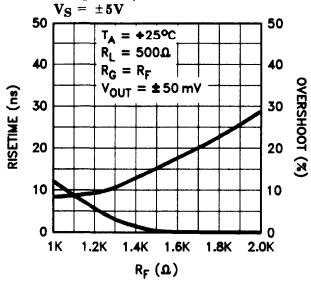
Bandwidth and Peaking vs R_F for A_V = +2, V_S = ±15V



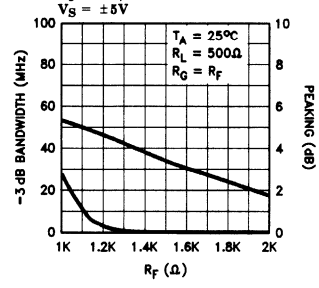
Voltage Gain vs Frequency A_V = +2, V_S = ±15V



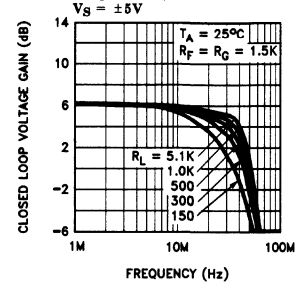
Rise Time and Overshoot vs R_F for A_V = +2, V_S = ±5V



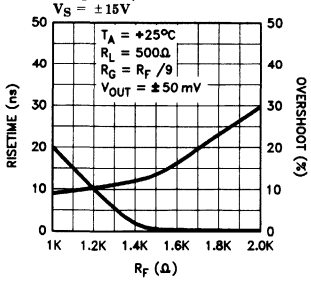
Bandwidth and Peaking vs R_F for A_V = +2, V_S = ±5V



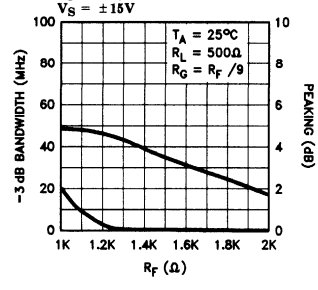
Voltage Gain vs Frequency A_V = +2, V_S = ±5V



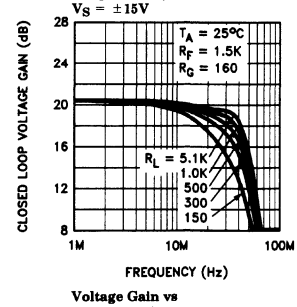
Rise Time and Overshoot vs R_F for A_V = +10, V_S = ±15V



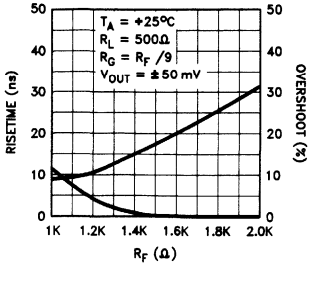
Bandwidth and Peaking vs R_F for A_V = +10, V_S = ±15V



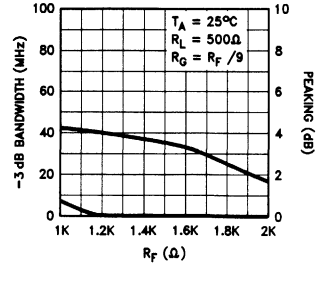
Voltage Gain vs Frequency A_V = +10, V_S = ±15V



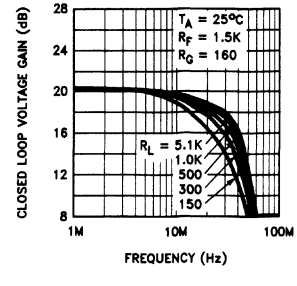
Rise Time and Overshoot vs R_F for A_V = +10, V_S = ±5V



Bandwidth and Peaking vs R_F for A_V = +10, V_S = ±5V



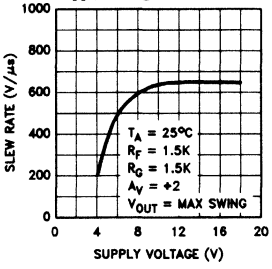
Voltage Gain vs Frequency A_V = +10, V_S = ±5V



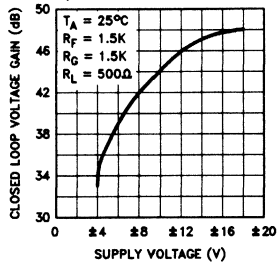
2232-5

Typical Performance Curves — Contd.

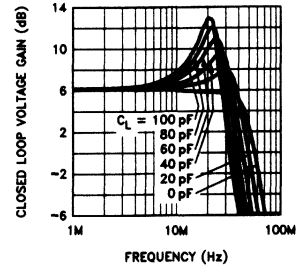
Slew Rate vs Supply Voltage



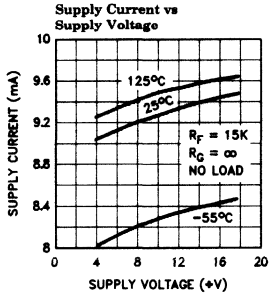
Small-Signal −3 dB Bandwidth vs Supply Voltage A_V = +2



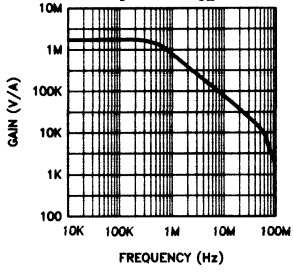
Voltage Gain vs Frequency for A_V = +2, Various Capacitive Loads



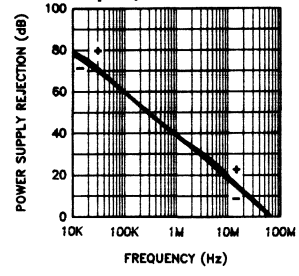
Supply Current vs Supply Voltage



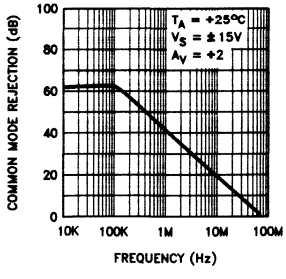
Transimpedance (R_{OL})



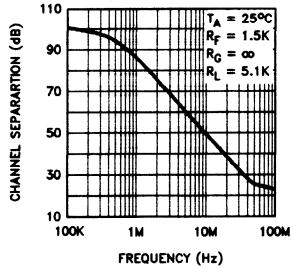
Power Supply Rejection vs Frequency



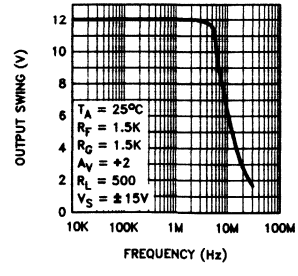
Common Mode Rejection vs Frequency



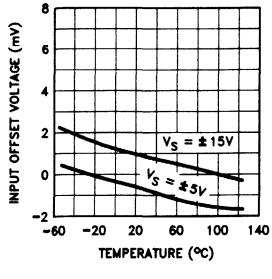
Channel Separation vs Frequency



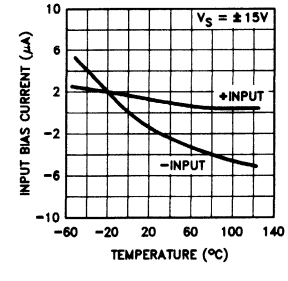
Maximum Output Swing vs Frequency



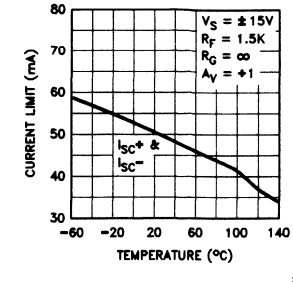
Input Offset Voltage vs Temperature



Input Bias Current vs Temperature



Current Limit vs Temperature

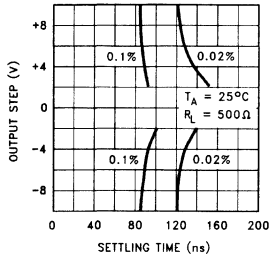


2232-6

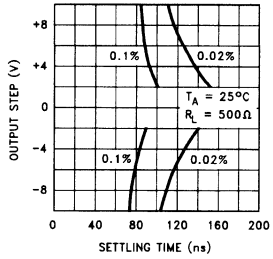
EL2232C
60 MHz, Fast Settling, Dual Current Feedback Amplifier

Typical Performance Curves — Contd.

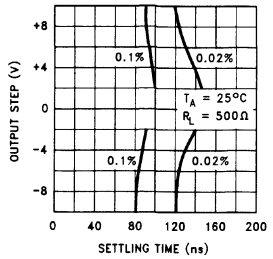
Settling Time vs Output Swing
$A_V = -1$, $V_S = \pm 15V$



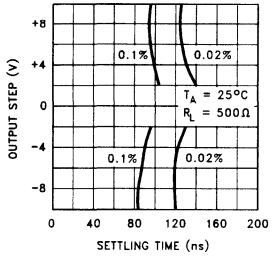
Settling Time vs Output Swing
$A_V = +1$, $V_S = \pm 15V$



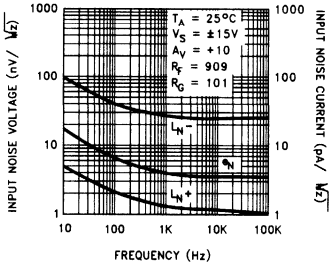
Settling Time vs Output Swing
$A_V = +2$, $V_S = \pm 15V$



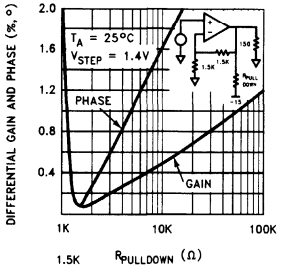
Settling Time vs Output Swing
$A_V = +10$, $V_S = \pm 15V$



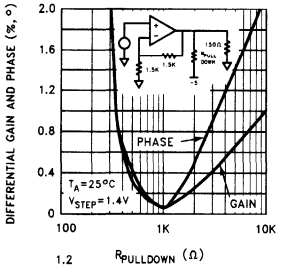
Equivalent Input Noise



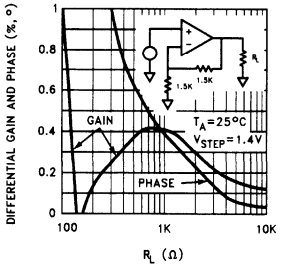
Differential Gain and Phase vs R Pulldown
$A_V = +2$, $V_S = \pm 15V$



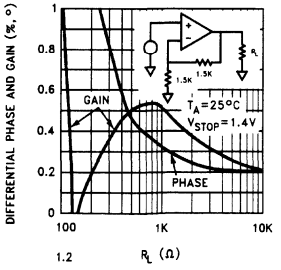
Differential Gain and Phase vs R Pulldown
$A_V = +2$, $V_S = \pm 5V$



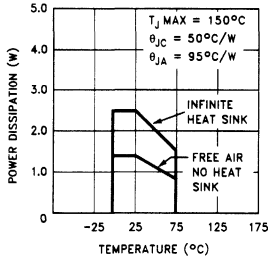
Differential Gain and Phase vs R_L $A_V = +2$, $V_S = \pm 15V$



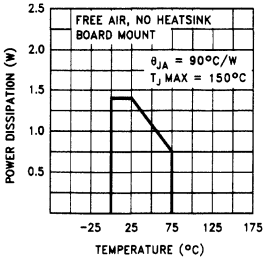
Differential Gain and Phase vs R_L $A_V = +2$, $V_S = \pm 5V$



8-Lead Plastic DIP
Maximum Power Dissipation vs Ambient Temperature



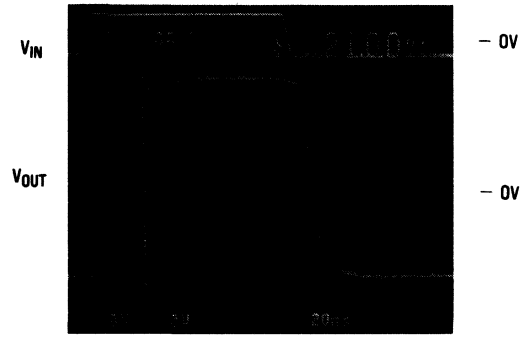
16-Lead SOL
Maximum Power Dissipation vs Ambient Temperature



2232-7

Typical Performance Curves — Contd.

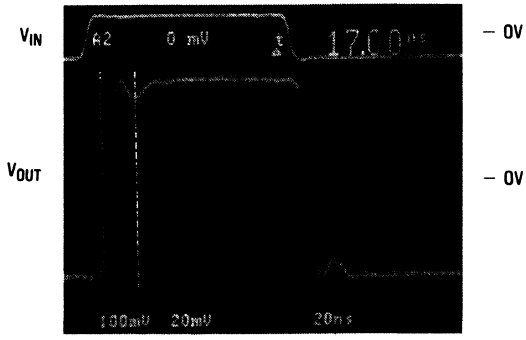
Large Signal Response



$A_V = +1$, $R_F = 1.5k$,
$R_L = 500\Omega$, $V_S = \pm 15V$

2232-8

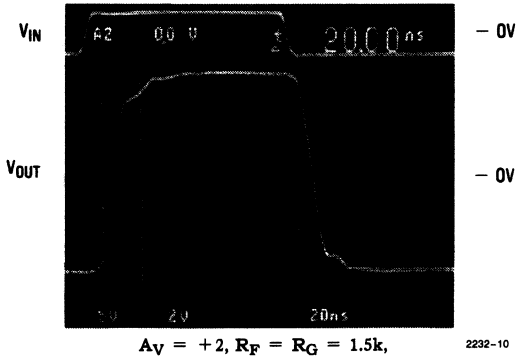
Small Signal Response



$A_V = +1$, $R_F = 1.5k$,
$R_L = 500\Omega$, $V_S = \pm 15V$

2232-9

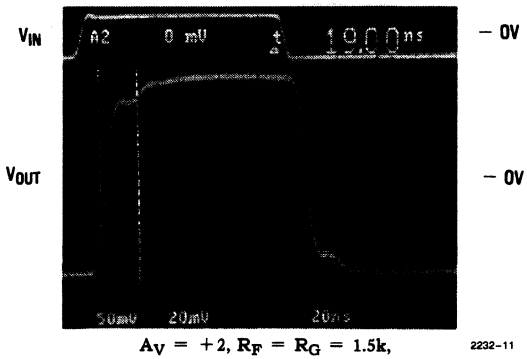
Large Signal Response



$A_V = +2$, $R_F = R_G = 1.5k$,
$R_L = 500\Omega$, $V_S = \pm 15V$

2232-10

Small Signal Response



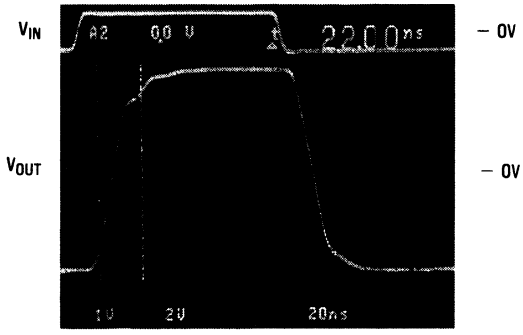
$A_V = +2$, $R_F = R_G = 1.5k$,
$R_L = 500\Omega$, $V_S = \pm 15V$

2232-11

EL2232C
60 MHz, Fast Settling, Dual Current Feedback Amplifier

Typical Performance Curves — Contd.

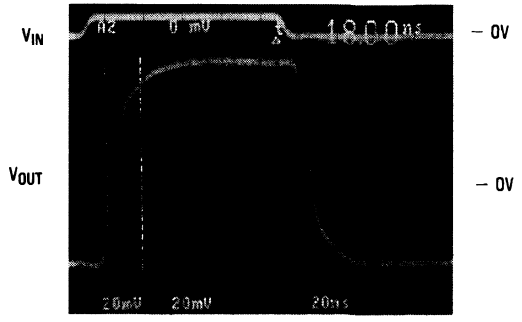
Large Signal Response



A_V = +10, R_F = 1.5k, R_G = 167,
R_L = 500Ω, V_S = ±15V

2232-12

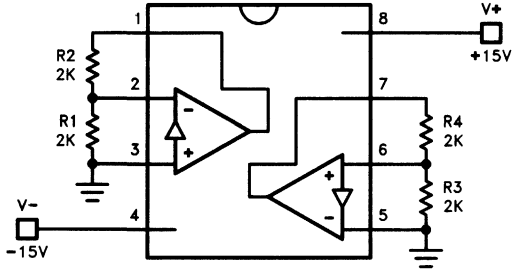
Small Signal Response



A_V = +10, R_F = 1.5k, R_G = 167,
R_L = 500Ω, V_S = ±15V,

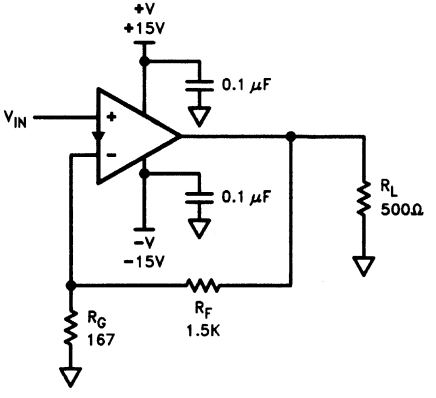
2232-13

Burn-In Circuit



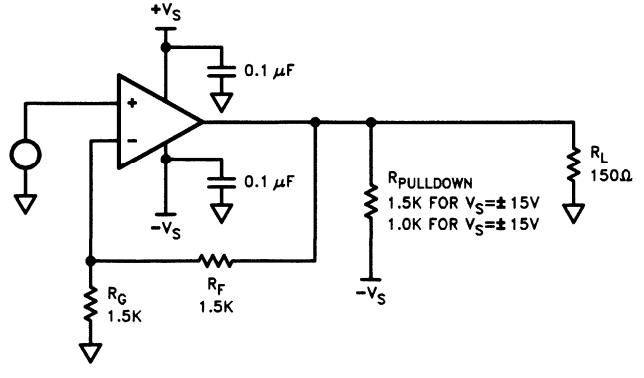
2232-14

Test Circuit



2232-15

Differential Gain and Phase Test Circuit



2232-16

Applications Information

Product Description

The EL2232 is a dual current-mode feedback amplifier similar to the industry-standard EL2020. Each of the EL2232's amplifiers has greater −3 dB bandwidth (60 MHz) and slew-rate (600 V/μs) than the EL2020, yet the total supply current for the EL2232 (9.5 mA) is only slightly more than the EL2020. Furthermore, the EL2232 has been characterized at both V_S = ±5V and V_S = ±15V.

With two amplifiers in a single package, the EL2232 allows 2-channel amplification with matched performance, as well as reduction of PC board area when compared to 2 single amplifiers. Designing with the EL2232 is simple, since in most applications it performs similarly to a conventional voltage-feedback operational amplifier.

Power Supply Bypassing/Lead Dressing

It is important to bypass the power supplies of the EL2232 with 0.1 μF or 0.01 μF ceramic disc capacitors. A 4.7 μF tantalum capacitor is also recommended for each supply. These capacitors should be placed as close to the package as possible, and long lead lengths should be avoided. Failure to bypass the supplies in this manner will result in oscillation or signal distortion.

The −input of the EL2232 is fairly sensitive to stray capacitance, therefore it is important for the feedback and gain-setting resistors to be as close as possible to the −input. It is also a good idea to remove the PC board ground-plane near the −input.

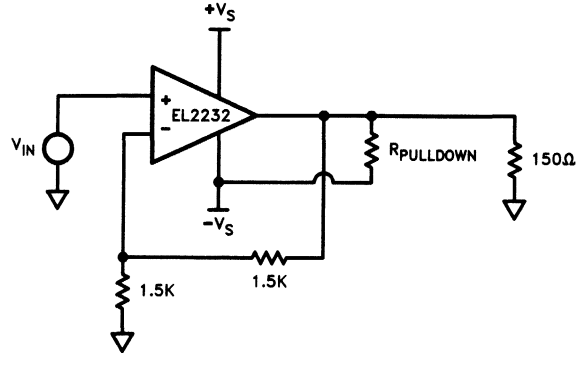
Current Limit

The EL2232 has an internal current limit of approximately 50 mA per amplifier, so if one of the outputs is shorted to ground (with V_S ±15V) the power dissipation could be as much as 1.1W. A heatsink is therefore required to survive an indefinite short at one of the outputs. If both of the outputs are shorted, power dissipation can approach 2W, resulting in the eventual destruction of the device, even with a heatsink.

Video Performance

To keep total supply current for the EL2232 at 9.5 mA, the output stage idle current had to be reduced substantially from the values used in the EL2020. As a consequence, a pulldown resistor is needed at the output of the EL2232 to achieve good video performance when driving the standard 150Ω double-terminated load. As seen in the Differential Gain and Phase Test Schematic, with ±15V rails a 1.5k pulldown resistor from the output to the −15V rail gives good video performance (0.1% dG 0.1° dP). With 5V rails, a 1k resistor gives similar results. These resistor values will vary with different load impedances, but in general the video performance improves as load impedance increases.

Adding a Pulldown Resistor to Improve Video Performance



2232-17

EL2232C
60 MHz, Fast Settling, Dual Current Feedback Amplifier

Applications Information — Contd.

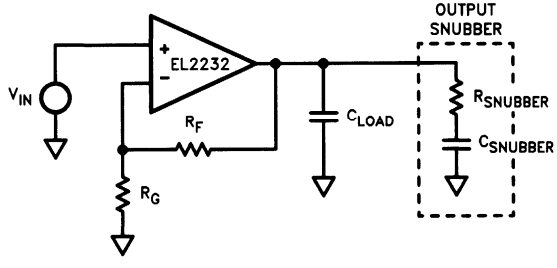
Capacitive Loading/Snubbing

The EL2232 has been designed to be stable in most situations with purely capacitive loads of up to about 50 pF. With 500Ω in parallel with the load capacitance, the EL2232 is usually stable with load capacitances of up to 100 pF, and often more (see the Cload vs Peaking curve). As expected with any high speed amplifier, the capacitive loading will increase the peaking of the closed loop frequency response (and therefore overshoot and ringing in the time domain) due to the decreased phase margin of the amplifier.

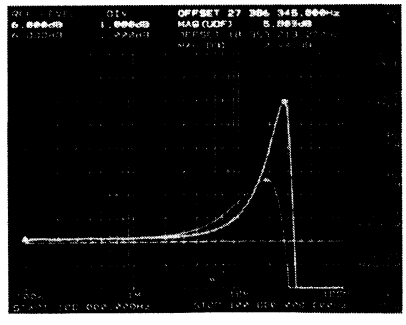
The use of an output snubber can be a valuable technique for improving stability when driving large capacitive loads. The output snubber is simply a series RC network placed from the output to ground, so that at high frequencies the amplifier is driving the load capacitance in parallel with a low value resistance (the snubber R). At low frequencies, the capacitance of the snubber is a high enough impedance so that the load looks the same as if the snubber were not tied to the output.

Selection of the R and C for the snubber is fairly simple. First, an R is selected to reduce peaking. As seen in the Frequency Response vs RL curves, the EL2232 has dramatically reduced peaking with a 150Ω load, so this is a good starting value. The resistor is then placed from the output to ground, and its value is varied until the desired response has been achieved. The capacitor is then chosen so that the corner frequency of the RC snubber is below the frequency of the peaking. Looking at the Cload vs Peaking Curve, the peaking is generally in the 20 MHz range for a gain of 2. Setting the corner frequency at 10 MHz, we get Csnubber = $1/(2\pi * Rsnubber * 10\ MHz)$ = 100 pF. This capacitance is then put in series with the snubber resistor and adjusted to achieve the desired response. As seen in the photograph, a 150Ω/100 pF snubber in conjunction with a 68 pF load reduces peaking from 5.8 dB down to a respectable 2.4 dB.

Adding An Output Snubber to Tame Capacitive Loads



2232-18

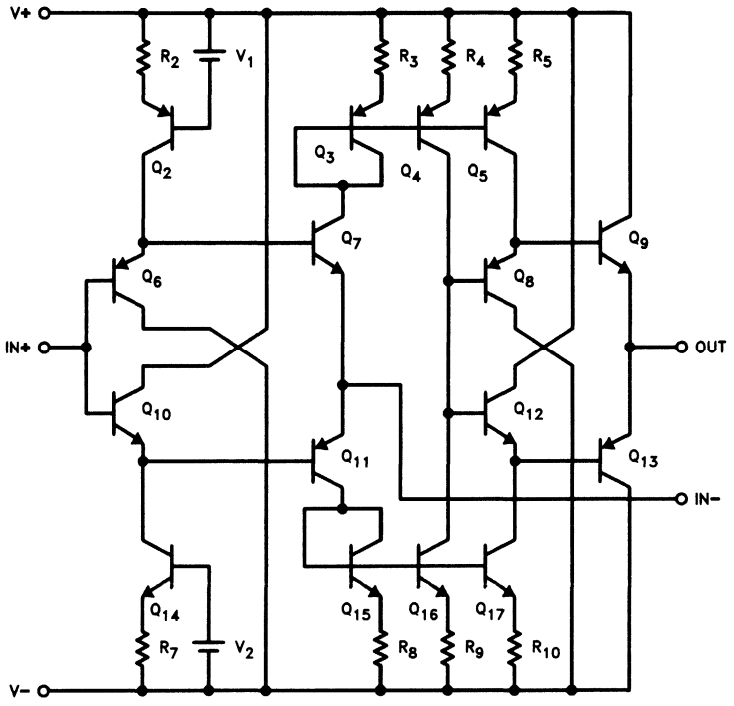


2232-19

EL2232 Frequency response with and without 150Ω/100 pF output snubber C_L = 68 pF

Applications Information — Contd.

Equivalent Circuit (One of Two Amplifiers)



2232-20

EL2232 Macromodel

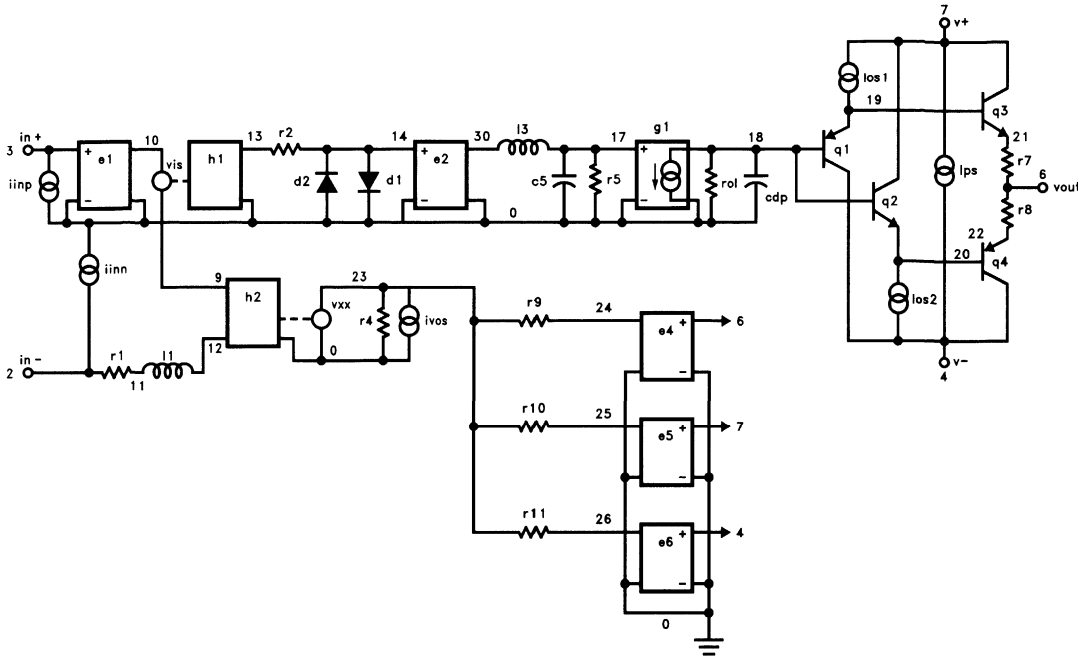
```
* Revision A. March 1992
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2232       3     2     8     4     1
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l1 11 12 29nH
iinp 3 0 1.2µA
iinm 2 0 5µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 10
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
e2 30 0 14 0 0.001
15 30 17 1.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 2Meg
cdp 18 0 2.5pF
*
* Output Stage
*
q1 4 18 19 qp
q2 8 18 20 qn
q3 8 19 21 qn
q4 4 20 22 qp
r7 21 1 5
r8 22 1 5
```

EL2232 Macromodel — Contd.

```
ios1 8 19 1mA
ios2 20 4 1mA
*
* Supply
*
ips 8 4 2mA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 1 0 1.0
e5 25 0 8 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1 4K
r10 25 23 10K
r11 26 23 10K
*
* Models
*
.model qn npn (is=5e-15 bf=250 tf=0.1nS)
.model qp pnp (is=5e-15 bf=250 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=10pA bv=0.8 n=4)
.ends
```

EL2232C
60 MHz, Fast Settling, Dual Current Feedback Amplifier

EL2232 Macromodel — Contd.



2232-21

EL2242C

Dual Fast Single-Supply Unity-Gain Stable Op Amp

Features

- Inputs and outputs operate at negative supply rail
- Unity gain bandwidth—30 MHz
- High slew rate—40 V/μs
- Settles to 0.01% of a 10V swing in 500 ns
- Operates with supplies as low as 3V or as great as 32V while consuming only 3.7 mA per amplifier
- Large open loop gain—110 dB
- Inputs tolerant of overload
- MIL-STD-883 Rev. C compliant

Applications

- Battery-powered instruments
- 12-bit DAC output amplifiers
- Fast-settling instrumentation amplifiers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2242CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2242CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

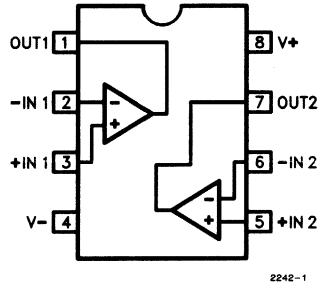
The EL2242 dual monolithic operational amplifier is as flexible as prior 324 devices but offers 30 times the bandwidth and slew-rate. Its inputs and outputs are able to operate down to the negative supply and are not damaged by overloads.

The EL2242 is useable in battery-operated systems with supplies as low as 3V, yet it has excellent gain and settling times while consuming only 3.7 mA per amplifier.

Elantec's products and facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see the Elantec document QRA-1: *Elantec's processing-Monolithic Products.*

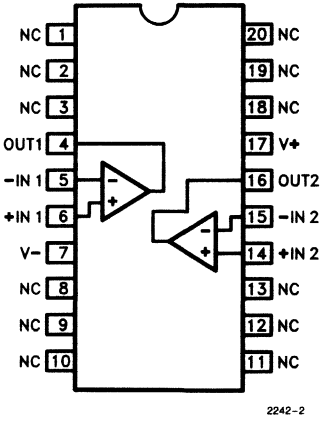
Connection Diagrams

Mini DIP



Top View

SOL



Top View

EL2242C

Dual Fast Single-Supply Unity-Gain Stable Op Amp

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Operating Junction Temperature	150°C
Voltage between −IN and +IN pins	36V	Storage Temperature Range	−65°C to +150°C
Voltage at −IN or +IN pins	V+ to V−	Lead Temperature	
Output Current	50 mA (Peak)	DIP Package	
	30 mA (Continuous)	(Soldering, <10 seconds)	300°C
Current into +IN or −IN	5 mA	SOL Package	
Internal Power Dissipation	See Curves	Vapor Phase (<60 seconds)	215°C
Operating Ambient Temperature Range	0°C to +75°C	Infrared (<15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±15V; R_L = 1k; T_A = 25°C, unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	25°C		2	7	I	mV
		Full			9	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		7		V	µV/°C
I_B	Input Bias Current	25°C		0.5	1.0	I	µA
		Full			2.0	III	µA
I_{OS}	Input Offset Current	25°C		0.200	0.200	I	µA
		Full			0.300	III	µA
$R_{IN, DIFF}$	Input Differential Resistance	25°C		20		V	MΩ
$R_{IN, COMM}$	Input Common-Mode Resistance	25°C		100		V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	pF
V_{CM+}	Positive Common-Mode Input Range	Full	12	13.3		II	V
V_{CM-}	Negative Common-Mode Input Range	Full	−15	−15.3		II	V
E_{IN}	Input Noise Voltage (f = 1 kHz, R_S = 0Ω)	25°C		15		VV	nV/√Hz

DC Electrical Characteristics

V_S = ±15V; R_L = 1k; T_A = 25°C, unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
A_{VOL}	Large Signal Voltage Gain (V_O = ±10V)	25°C	150	300		I	V/mV
		Full	15			III	V/mV
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	70	95		II	dB
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	70	95		II	dB
V_O	Output Voltage Swing Negative Swing, R_L to V− V+ = +5V, V− = 0V	Full	±12	±13.5		II	V
		Full			+20	II	mV
I_O	Output Current (Note 3)	Full	±12	±50	±70	II	mA
I_S	Supply Current (Both Amplifiers)	Full		8.2	10	II	mA

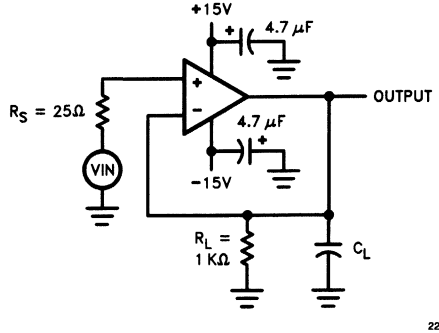
AC Electrical Characteristics

V_S = ±15V; R_L = 1 kΩ; C_L = 20 pF; T_A = 25°C, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
BW	Unity Gain −3 dB Bandwidth (Note 4)		30		V	MHz
GBW	Gain-Bandwidth Product (Note 4)		16		V	MHz
SR	Slew Rate (V_O = ± 10V)		40		V	V/μs
OS	Overshoot (Note 4)		30		V	%
t_s	Settling Time to 0.1%		480		V	ns
	10V Step to 0.01%		550		V	ns

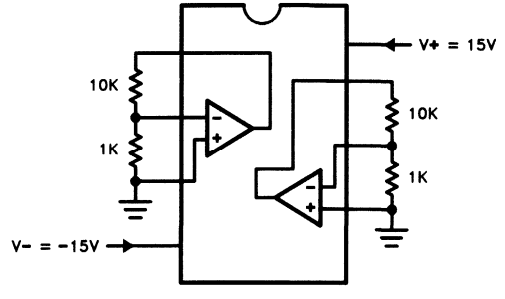
Note 1: Two tests are performed with V_{CM} = 0V to −12V and V_{CM} = 0V to 12V.
Note 2: Two tests are performed with V+ = 3V, V− changed from −2V to −27V; V− = −2V, V+ changed from 3V to 28V.
Note 3: The inputs are overdriven by ±15V and the output R_L = 100Ω.
Note 4: V_{IN} = 100 mV peak-to-peak.

Test Circuit



2242-3

Burn-In Circuit

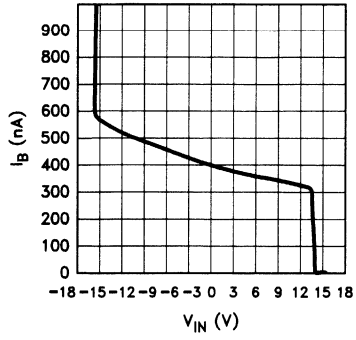


2242-4

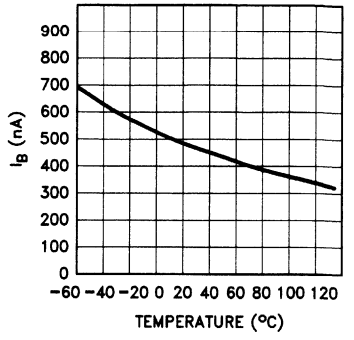
EL2242C
Dual Fast Single-Supply Unity-Gain Stable Op Amp

Typical Performance Curves

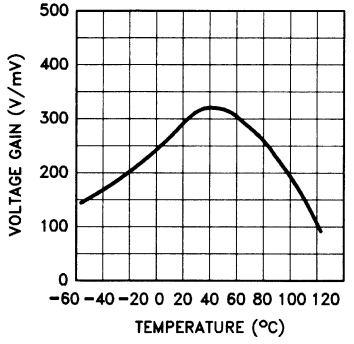
Input Bias Current vs Common-Mode Voltage



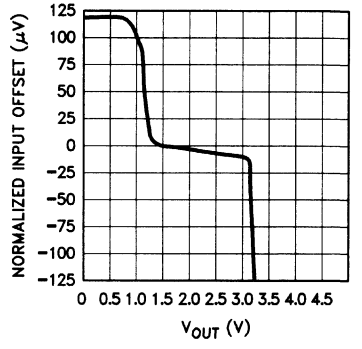
Input Bias Current vs Temperature



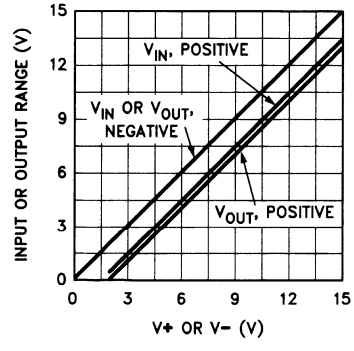
Voltage Gain vs Temperature



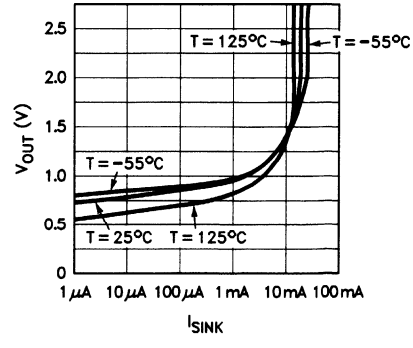
Input-Output Transfer Function, +5V Supply



Input and Output Voltage Swings vs Supply Voltages



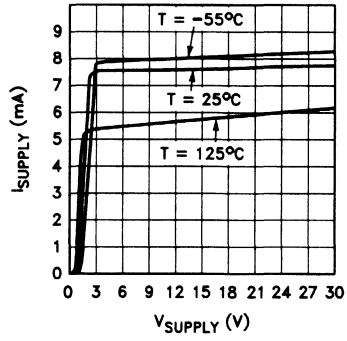
Output Voltage vs Current Sinking



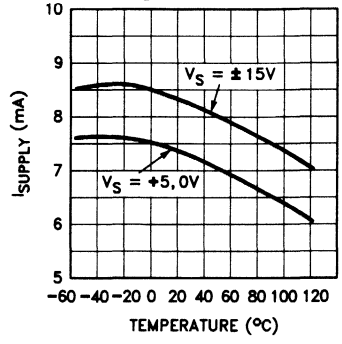
2242-5

Typical Performance Curves — Contd.

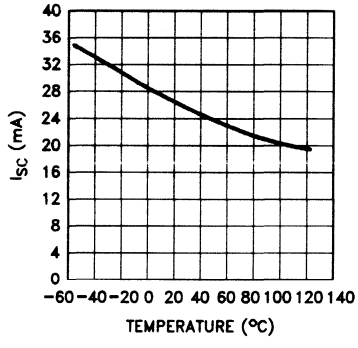
Supply Current vs Supply Voltage—Both Amplifiers



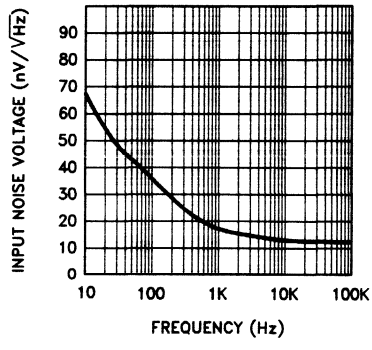
Supply Current vs Temperature Both Amplifiers



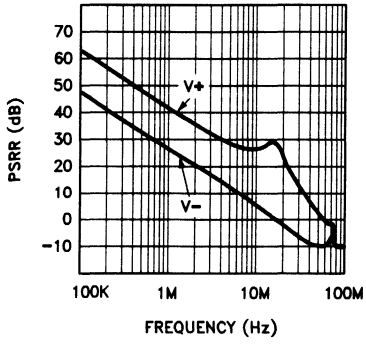
Output Short-Circuit Current vs Temperature



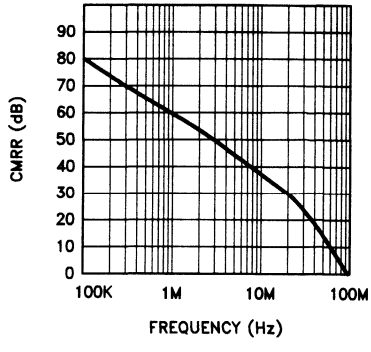
Input Voltage Noise vs Frequency



Power Supply Rejection Ratio vs Frequency



Common-Mode Rejection Ratio vs Frequency

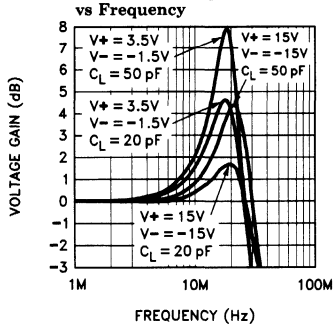


2242-6

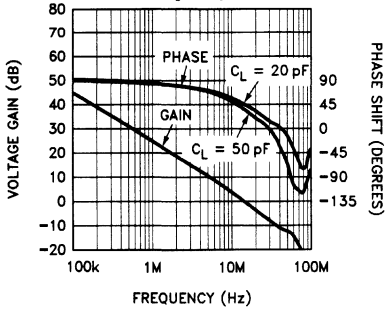
EL2242C
Dual Fast Single-Supply Unity-Gain Stable Op Amp

Typical Performance Curves — Contd.

Utility-Gain Response vs Frequency

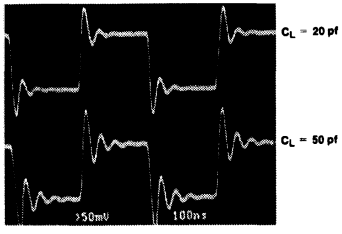


Open-Loop Gain and Phase vs Frequency



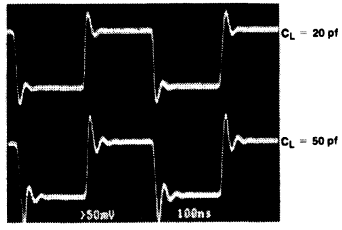
2242-7

Pulse Response with V+ = 3V, V− = −2V



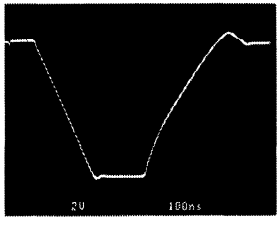
2242-8

Pulse Response with V+ = 15V, V− = −15V



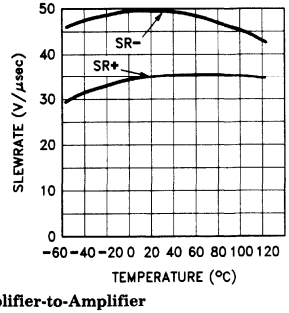
2242-9

Slew Characteristics



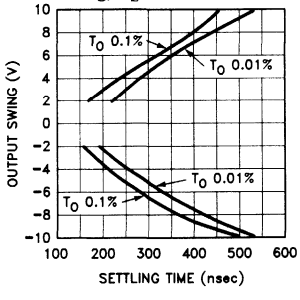
2242-10

Slew Rate vs Temperature

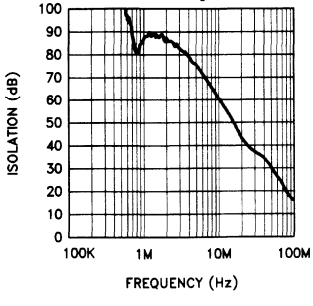


2242-11

Settling Time vs Output Swing, V_S = ±15V



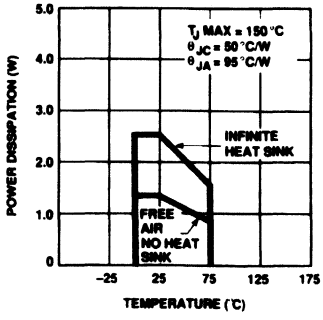
Amplifier-to-Amplifier Isolation vs Frequency



2242-12

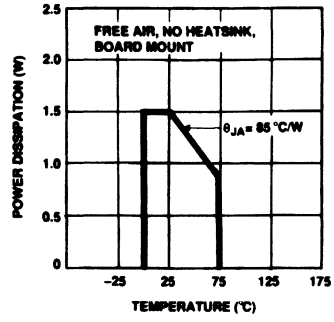
Typical Performance Curves — Contd.

8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



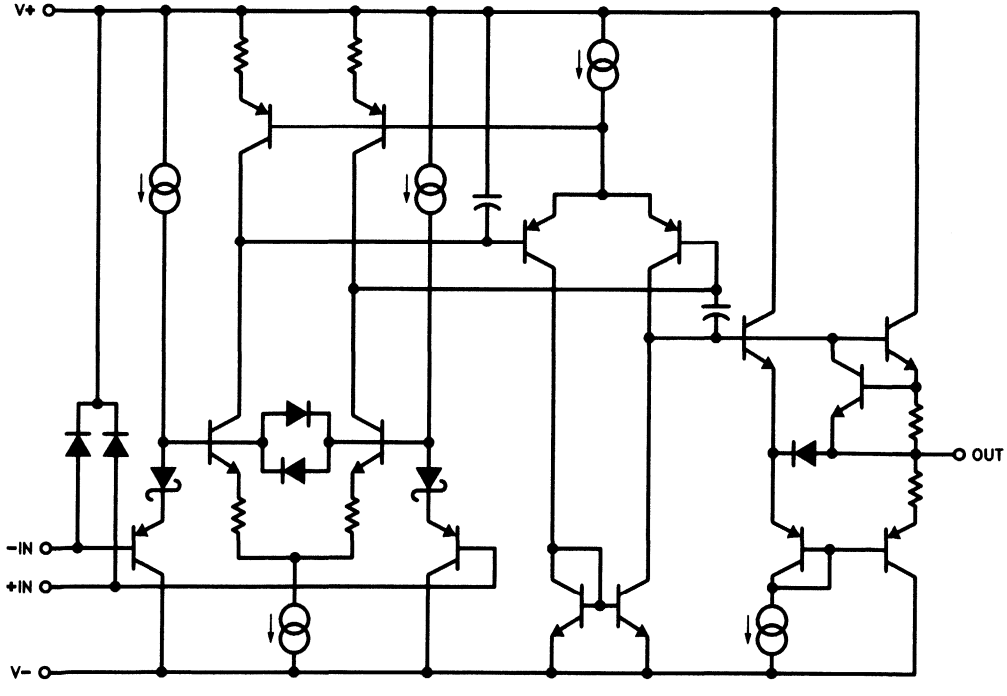
2242-13

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2242-15

Simplified Schematic (One Amplifier)



2242-16

EL2242C
Dual Fast Single-Supply Unity-Gain Stable Op Amp

Applications Information

The EL2242 is a fast amplifier designed to operate from a very wide range of power supply voltages. The inputs operate all the way to the negative supply (actually about 200 mV below it) and up to typically 2V below the positive supply. The outputs swing a similar range, but some attention is required in practice.

Specifically, while the output NPN transistor can source load current over the full output span (see the simplified schematic), the output PNP device simply turns off at negative swings below about a volt above the negative supply rail. This property is shown in the "Output Voltage vs Current-Sinking" typical curve. All single-supply amplifiers have this characteristic, and the solution is to provide a load resistor from the output to the negative supply rail.

When the output is in this extreme negative swing region, the bandwidth, gain, and settling properties are all degraded by a factor of about 2. Even so, the AC characteristics are well-behaved in this region.

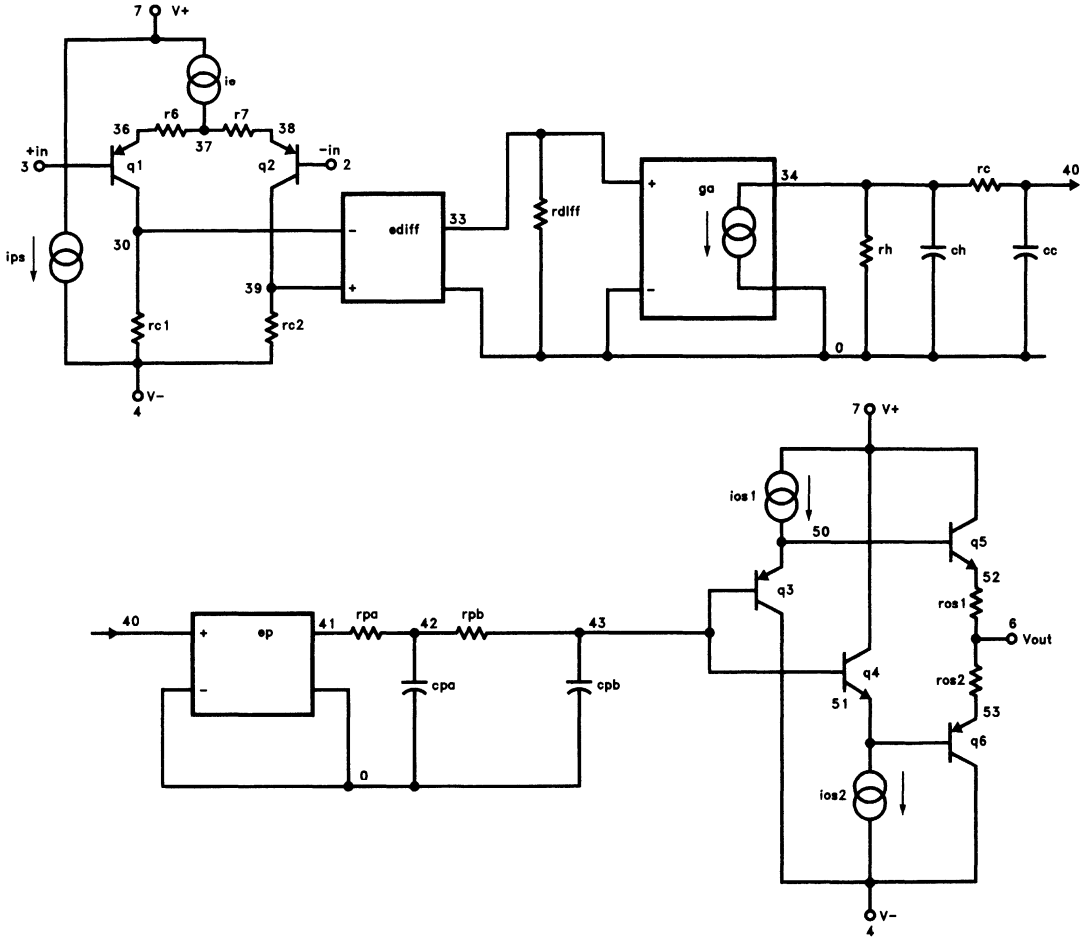
Electrostatic discharge protection devices clamp the inputs a diode drop above V+ and a diode drop below V−.

As for all amplifiers, good supply bypassing will optimize settling and amplifier-to-amplifier rejection. 4.7 μF tantalum capacitors seem to be the best, and no additional small capacitor is needed in parallel for very high-frequency bypassing. Reasonably low feedback impedances are important to preserving closed-loop stability, 1k or less being acceptable when capacitive parasitics are minimized. Stability is best when the EL2242 is operated from large supplies, especially when driving capacitive loads.

EL2242 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2242       3     2     7     4     6
* Input Stage
ie 7 37 84uA
r6 36 37 2.1K
r7 38 37 2.1K
rc1 4 30 6K
rc2 4 39 6K
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 1m
rh 34 0 175Meg
ch 34 0 5pF
rc 34 40 1K
cc 40 0 7pF
* Poles
ep 41 0 40 0 1.0
rpa 41 42 200
cpa 42 0 4pF
rpb 42 43 1K
cpb 43 0 2pF
* Output Stage
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
* Power Supply Current
ips 7 4 1.8mA
* Models
.model qn npn(is=800E-18 bf=100 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=120 tf=0.2nS)
.model qp pnp(is=800E-18 bf=50 tf=0.2nS)
.ends
```

EL2242 Macromodel — Contd.



2242-17

EL2243C

Dual Fast Single-Supply Decompensated Op Amp

Features

- Inputs and outputs operate at negative supply rail
- Gain bandwidth product—70 MHz
- High slew rate—90 V/μs
- Settles to 0.01% of a 10V swing in 400 ns
- Operates with supplies as low as 3V or as great as 32V while consuming only 3.7 mA per amplifier
- Large open loop gain—114 dB
- Inputs tolerant of overload
- MIL-STD-883 Rev. C compliant

Applications

- Battery-powered instruments
- 12-bit DAC output amplifiers
- Fast-settling instrumentation amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2243CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2243CM	0°C to +75°C	20-Lead SOL	MDP0027

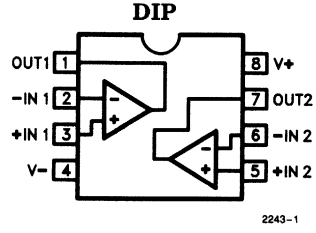
General Description

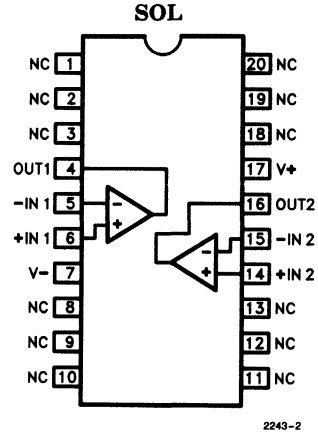
The EL2243 dual monolithic operational amplifier is as flexible as prior 324 devices but offers 100 times the bandwidth and slewrate. Its inputs and outputs are able to operate down to the negative supply and are not damaged by overloads.

The EL2243 is useable in battery-operated systems with supplies as low as 3V, yet it has excellent gain and settling times while consuming only 3.7 mA per amplifier.

Elantec's products and facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see the Elantec document QRA-1: *"Elantec's processing-Monolithic Products"*.

Connection Diagrams





EL2243C

Dual Fast Single-Supply Decompensated Op Amp

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Operating Junction Temperature	150°C
Voltage between −IN and +IN Pins	36V	Storage Temperature Range	−65°C to +150°C
Voltage at −IN or +IN Pins	V+ to V−	Lead Temperature	
Output Current	50 mA (Peak)	DIP Package	
	30 mA (Continuous)	(Soldering, 10 seconds)	300°C
Current into +IN or −IN	5 mA	SOL Package	
Internal Power Dissipation	See Curves	Vapor Phase (<60 seconds)	215°C
Operating Ambient Temperature Range	0°C to +75°C	Infrared (<15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1k; T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	25°C Full		1.5	7 9	I III	mV mV
TCV_{OS}	Average Offset Voltage Drift	Full		5		V	µV/C
I_B	Input Bias Current	25°C Full		0.5	1.0 2.0	I III	µA µA
I_{OS}	Input Offset Current	25°C Full		0.01	0.200 0.300	I III	µA µA
R_{IN}, Diff	Input Differential Resistance	25°C		10		V	MΩ
R_{IN}, Comm	Input Common-Mode Resistance	25°C		100		V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	pF
V_{CM+}	Positive Common-Mode Input Range	Full	12	13.3		II	V
V_{CM-}	Negative Common-Mode Input Range	Full	−15	−15.3		II	V
E_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		12		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (V_O = ±10V)	25°C Full	250 15	500		I III	V/mV V/mV
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	70	100		II	dB

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1k$; $T_A = 25°C$ unless otherwise specified — Contd.

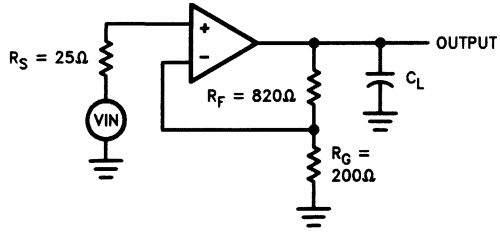
Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	70	100		II	dB
V_O	Output Voltage Swing Negative Swing, R_L to V− V+ = +5V, V− = 0V	Full	±12	±13.5	 −20	II II	V mV
I_O	Output Current (Note 3)	Full	±12	±30	±70	II	mA
I_S	Supply Current (Both Amplifiers)	Full		8.2	10	II	mA

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 1\ k\Omega$; $C_L = 20\ pF$; $T_A = 25°C$; unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
GBW	Gain-Bandwidth Product (Note 4)		70		V	MHz
SR	Slew Rate ($V_O = \pm 10V$)		90		V	V/μs
OS	Overshoot (Note 4)		30		V	%
t_s	Settling Time to 0.1% 10V Step to 0.01%		320 380		V V	ns ns

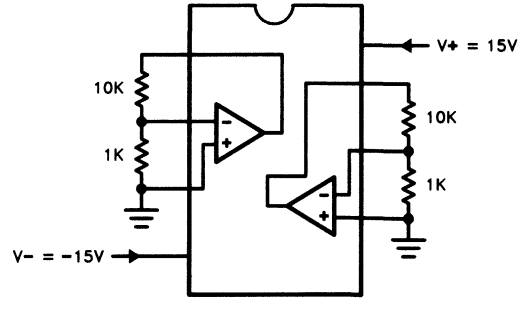
Note 1: Two tests are performed with $V_{CM} = 0V$ to $-12V$ and $V_{CM} = 0V$ to 12V.
Note 2: Two tests are performed with V+ = 3V, V− changed from −2V to −27V; V− = −2V, V+ changed from 3V to 28V.
Note 3: The inputs are overdriven by ±15V and the output R1 = 100Ω.
Note 4: V_{OUT} = 100 mV peak-to-peak.

Test Circuit



2243-3

Burn-In Circuit

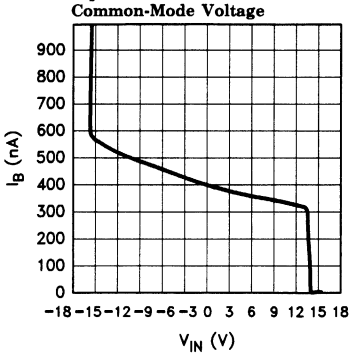


2243-4

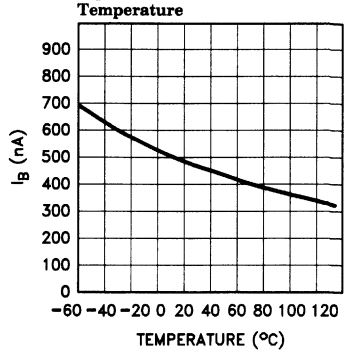
EL2243C
Dual Fast Single-Supply Decompensated Op Amp

Typical Performance Curves

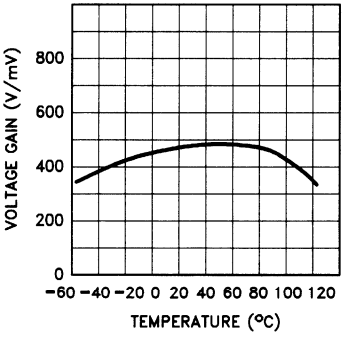
Input Bias Current vs Common-Mode Voltage



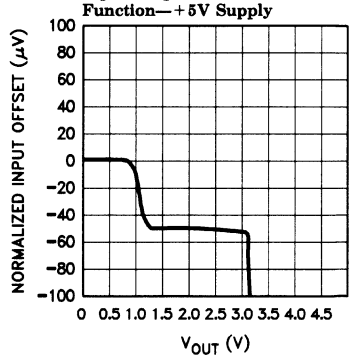
Input Bias Current vs Temperature



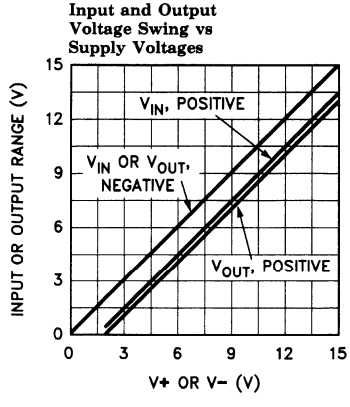
Voltage Gain vs Temperature



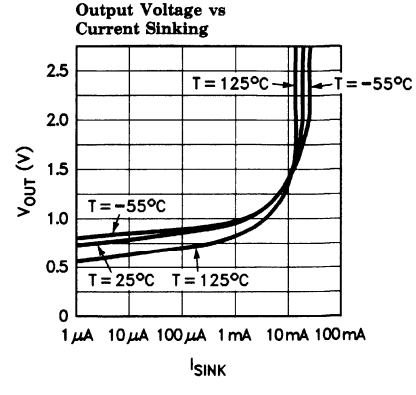
Input-Output Transfer Function—+5V Supply



Input and Output Voltage Swing vs Supply Voltages



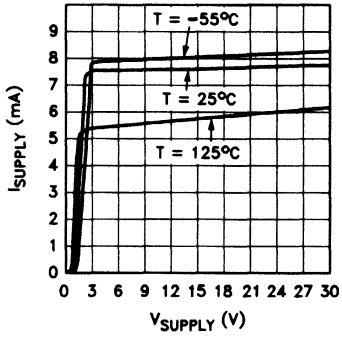
Output Voltage vs Current Sinking



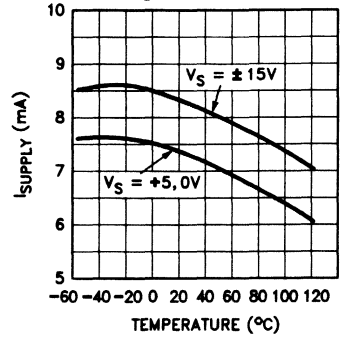
2243-5

Typical Performance Curves — Contd.

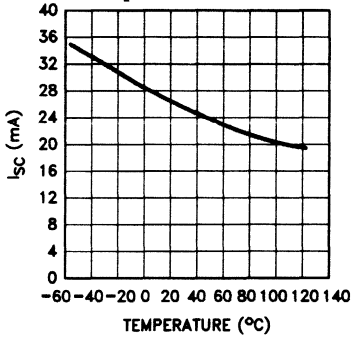
Supply Current vs Supply Voltage— Both Amplifiers



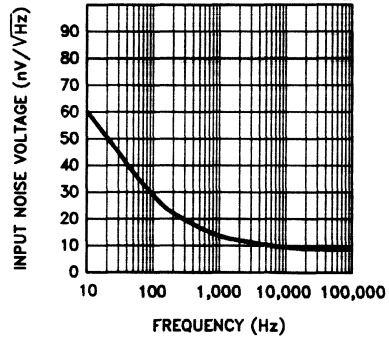
Supply Current vs Temperature— Both Amplifiers



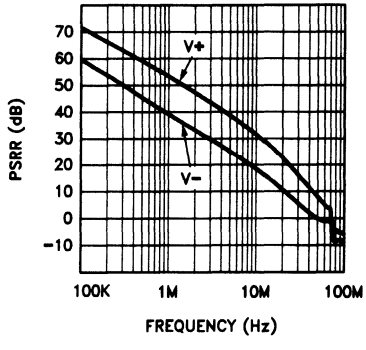
Output Short-Circuit Current vs Temperature



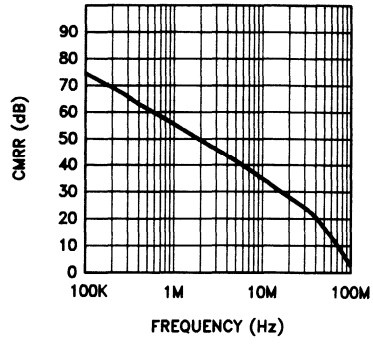
Input Voltage Noise vs Frequency



Power Supply Rejection Ratio vs Frequency



Common-Mode Rejection Ratio vs Frequency

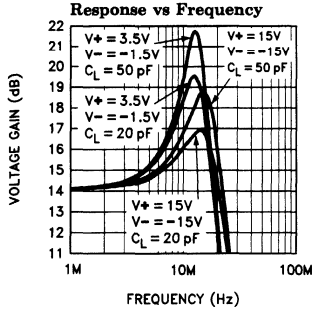


2243-6

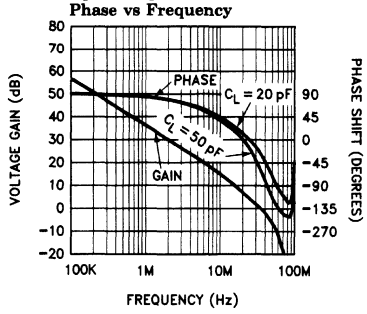
EL2243C
Dual Fast Single-Supply Decompensated Op Amp

Typical Performance Curves — Contd.

Gain of +5 Response vs Frequency

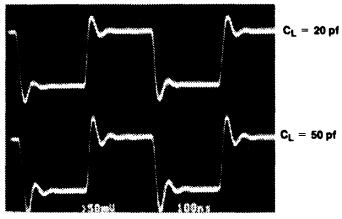


Open-Loop Gain and Phase vs Frequency



2243-7

Pulse Response with V+ = 15V, V− = −15V

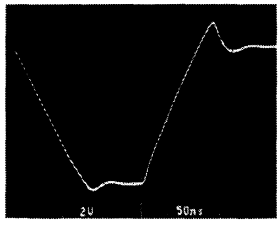


2243-8

Pulse Response with V+ = 3V, V− = −2V

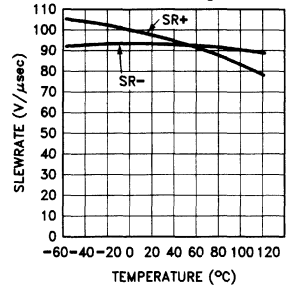
2243-9

Slew Characteristic



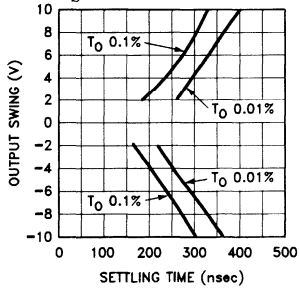
2243-10

Slew Rate vs Temperature

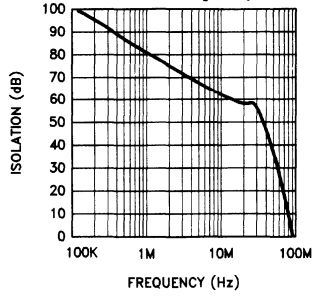


2243-11

Settling Time vs Output Swing $V_S = \pm 15V$



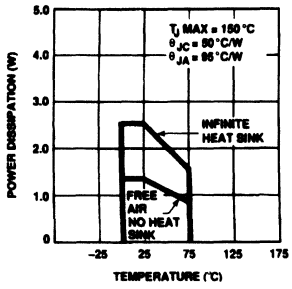
Amplifier-to-Amplifier Isolation vs Frequency



2243-12

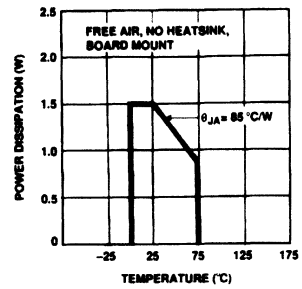
Typical Performance Curves — Contd.

8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



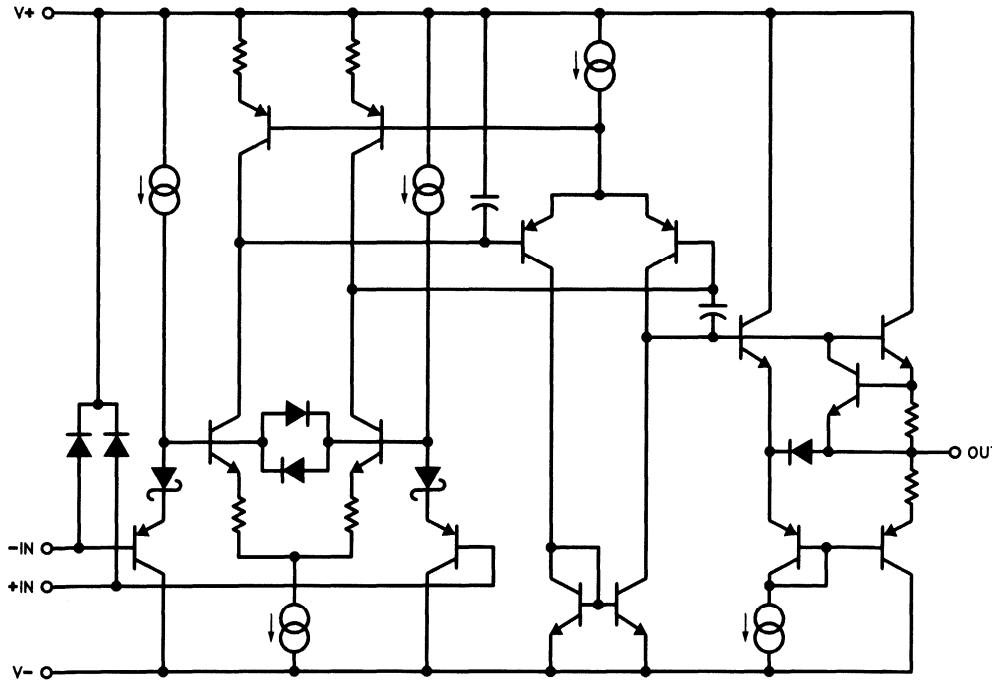
2243-13

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2243-15

Simplified Schematic (One Amplifier)



2243-16

EL2243C
Dual Fast Single-Supply Decompensated Op Amp

Applications Information

The EL2243 is a fast amplifier designed to operate from a very wide range of power supply voltages. The inputs operate all the way to the negative supply (actually about 200 mV below it) and up to typically 2V below the positive supply. The outputs swing a similar range, but some attention is required in practice.

Specifically, while the output NPN transistor can source load current over the full output span (see the simplified schematic), the output PNP device simply turns off at negative swings below about a volt above the negative supply rail. This property is shown in the "Output Voltage vs. Current-Sinking" typical curve. All single-supply amplifiers have this characteristic, and the solution is to provide a load resistor from the output to the negative supply rail.

When the output is in this extreme negative swing region, the bandwidth, gain, and settling properties are all degraded by a factor of about 2. Even so, the AC characteristics are well-behaved in this region.

Electrostatic discharge protection devices clamp the inputs a diode drop above V+ and a diode drop below V−.

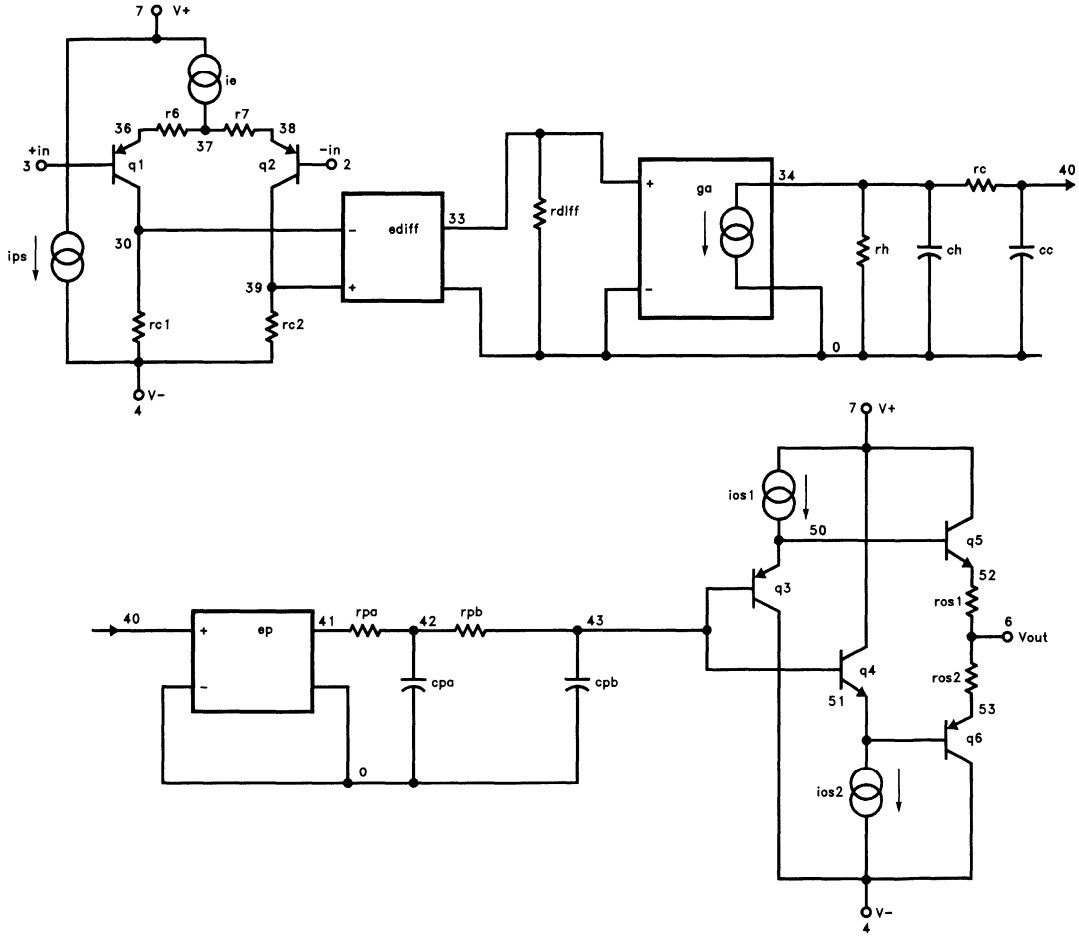
As for all amplifiers, good supply bypassing will optimize settling and amplifier-to-amplifier rejection. 4.7 μF tantalum capacitors seem to be the best, and no additional small capacitor is needed in parallel for very high-frequency bypassing. Reasonably low feedback impedances are important to preserving closed-loop stability, 1k or less being acceptable when capacitive parasitics are minimized. Stability is best when the EL2243 is operated from large supplies, especially when driving capacitive loads.

EL2243 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2243       3     2     7     4     6
* Input stage
ie 7 37 200uA
r6 36 37 1K
r7 38 37 1K
rc1 4 30 3K
rc2 4 39 3K
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 1m
rh 34 0 175Meg
ch 34 0 4pF
rc 34 40 1K
cc 40 0 4pF
* Poles
ep 41 0 40 0 1.0
rpa 41 42 1K
cpa 42 0 4pF
rpb 42 43 1K
cpb 43 0 2pF
* Output Stage
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
* Power Supply Current
ips 7 4 1.5mA
* Models
.model qn npn(is=800e-18 bf=100 tf=0.2nS)
.model qpa pnp(is=864e-18 bf=150 tf=0.2nS)
.model qp pnp(is=800e-18 bf=125 tf=0.2nS)
.ends
```

EL2243C
Dual Fast Single-Supply Decompensated Op Amp

EL2243 Macromodel — Contd.



2243-17

EL2244C/EL2444C

Dual/Quad Low-Power 60 MHz Unity-Gain Stable Op Amp

Features

- 60 MHz gain-bandwidth product
- Unity-gain stable
- Low supply current (per Amplifier) = 5.2 mA at $V_S = \pm 15V$
- Wide supply range = $\pm 2V$ to $\pm 18V$ dual-supply = 2.5V to 36V single-supply
- High slew rate = 325 V/μs
- Fast settling = 80 ns to 0.1% for a 10V step
- Low differential gain = 0.04% at $A_V = +2$, $R_L = 150\Omega$
- Low differential phase = 0.15° at $A_V = +2$, $R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing = $\pm 13.6V$ with $V_S = \pm 15V$, $R_L = 1000\Omega$ = 3.8V/0.3V with $V_S = +5V$, $R_L = 500\Omega$
- Low cost, enhanced replacement for the AD827 and LT1229/LT1230

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
Duals			
EL2244CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2244CS	−40°C to +85°C	8-Lead SO	MDP0027
Quads			
EL2444CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL2444CS	−40°C to +85°C	14-Lead SO	MDP0027

General Description

The EL2244C/EL2444C are dual and quad versions of the popular EL2044C. They are high speed, low power, low cost monolithic operational amplifiers built on Elantec's proprietary complementary bipolar process. The EL2244C/EL2444C are unity-gain stable and feature a 325 V/μs slew rate and 60 MHz gain-bandwidth product while requiring only 5.2 mA of supply current per amplifier.

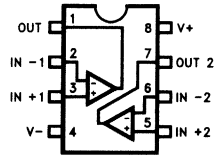
The power supply operating range of the EL2244C/EL2444C is from ±18V down to as little as ±2V. For single-supply operation, the EL2244C/EL2444C operate from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2244C/EL2444C makes them an obvious choice for applications on a single +5V or +3V supply.

The EL2244C/EL2444C also feature an extremely wide output voltage swing of ±13.6V with $V_S = \pm 15V$ and $R_L = 1000\Omega$. At ±5V, output voltage swing is a wide ±3.8V with $R_L = 500\Omega$ and ±3.2V with $R_L = 150\Omega$. Furthermore, for single-supply operation at +5V, output voltage swing is an excellent 0.3V to 3.8V with $R_L = 500\Omega$.

At a gain of +1, the EL2244C/EL2444C have a −3 dB bandwidth of 120 MHz with a phase margin of 50°. They can drive unlimited load capacitance, and because of their conventional voltage-feedback topology, the EL2244C/EL2444C allow the use of reactive or non-linear elements in their feedback network. This versatility combined with low cost and 75 mA of output-current drive make the EL2244C/EL2444C an ideal choice for price-sensitive applications requiring low power and high speed.

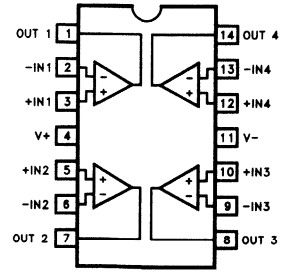
Connection Diagrams

EL2244CN/CS
Dual



2244-1

EL2444CN/CS
Quad



2244-2

EL2244C/EL2444C

Dual/Quad Low-Power 60 MHz Unity-Gain Stable Op Amp

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±18V or 36V	Operating Junction Temperature (T_J)	150°C
Peak Output Current (I_{OP})	Short-Circuit Protected	Storage Temperature (T_{ST})	−65°C to +150°C
Output Short-Circuit Duration (Note 1)	Infinite	Lead Temperature	
Input Voltage (V_{IN})	±V_S	DIP Package (Soldering: < 5 seconds)	300°C
Differential Input Voltage (dV_{IN})	±10V	SO Package	
Power Dissipation (P_D)	See Curves	Vapor Phase (60 seconds)	215°C
Operating Temperature Range (T_A)	−40°C to +85°C	Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		0.5	4.0	I	mV
			T_{MIN}, T_{MAX}			9.0	IV	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)	All		10.0		V	µV/°C
I_B	Input Bias Current	V_S = ±15V	25°C		2.8	8.2	I	µA
			T_{MIN}, T_{MAX}			11.2	IV	µA
		V_S = ±5V	25°C		2.8		V	µA
I_{OS}	Input Offset Current	V_S = ±15V	25°C		50	300	I	nA
			T_{MIN}, T_{MAX}			500	IV	nA
		V_S = ±5V	25°C		50		V	nA
TCI_{OS}	Average Offset Current Drift	(Note 2)	All		0.3		V	nA/°C
A_{VOL}	Open-Loop Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1000Ω	25°C	1000	1500		I	V/V
			T_{MIN}, T_{MAX}	800			IV	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 500Ω	25°C		1200		V	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 150Ω	25°C		1000		V	V/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	25°C	70	80		I	dB
			T_{MIN}, T_{MAX}	65			IV	dB

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±12V, V_{OUT} = 0V	25°C	70	90		I	dB
			T_{MIN}, T_{MAX}	70			IV	dB
CMIR	Common-Mode Input Range	V_S = ±15V	25°C		±14.0		V	V
		V_S = ±5V	25°C		±4.2		V	V
		V_S = +5V	25°C		4.2/0.1		V	V
V_{OUT}	Output Voltage Swing	V_S = ±15V, R_L = 1000Ω	25°C	±13.4	±13.6		I	V
			T_{MIN}, T_{MAX}	±13.1			IV	V
		V_S = ±15V, R_L = 500Ω	25°C	±12.0	±13.4		I	V
		V_S = ±5V, R_L = 500Ω	25°C	±3.4	±3.8		IV	V
		V_S = ±5V, R_L = 150Ω	25°C		±3.2		V	V
		V_S = +5V, R_L = 500Ω	25°C	3.6/0.4	3.8/0.3		I	V
			T_{MIN}, T_{MAX}	3.5/0.5			IV	V
I_{SC}	Output Short Circuit Current		25°C	50	75		I	mA
			T_{MIN}, T_{MAX}	35			IV	mA
I_S	Supply Current (Per Amplifier)	V_S = ±15V, No Load	25°C		5.2	6.3	I	mA
			T_{MIN}			7.6	IV	mA
			T_{MAX}			7.6	IV	mA
		V_S = ±5V, No Load	25°C		5.0		V	mA
R_{IN}	Input Resistance	Differential	25°C		150		V	kΩ
		Common-Mode	25°C		15		V	MΩ
C_{IN}	Input Capacitance	A_V = +1@ 10 MHz	25°C		1.0		V	pF
R_{OUT}	Output Resistance	A_V = +1	25°C		50		V	mΩ
PSOR	Power-Supply Operating Range	Dual-Supply	25°C	±2.0		±18.0	V	V
		Single-Supply	25°C	2.5		36.0	V	V

Closed-Loop AC Electrical Characteristics

V_S = ±15V, A_V = +1, R_L = 1000Ω unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	V_S = ±15V, A_V = +1	25°C		120		V	MHz
		V_S = ±15V, A_V = −1	25°C		60		V	MHz
		V_S = ±15V, A_V = +2	25°C		60		V	MHz
		V_S = ±15V, A_V = +5	25°C		12		V	MHz
		V_S = ±15V, A_V = +10	25°C		6		V	MHz
		V_S = ±5V, A_V = +1	25°C		80		V	MHz
GBWP	Gain-Bandwidth Product	V_S = ±15V	25°C		60		V	MHz
		V_S = ±5V	25°C		45		V	MHz

Closed-Loop AC Electrical Characteristics

V_S = ±15V, A_V = +1, R_L = 1000Ω unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
PM	Phase Margin	R_L = 1 kΩ, C_L = 10 pF	25°C		50		V	°
CS	Channel Separation	f = 5 MHz	25°C		85		V	dB
SR	Slew Rate (Note 3)	V_S = ±15V, R_L = 1000Ω	25°C	250	325		I	V/µs
		V_S = ±5V, R_L = 500Ω	25°C		200		V	V/µs
FPBW	Full-Power Bandwidth (Note 4)	V_S = ±15V	25°C	4.0	5.2		I	MHz
		V_S = ±5V	25°C		12.7		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step	25°C		3.0		V	ns
OS	Overshoot	0.1V Step	25°C		20		V	%
t_{PD}	Propagation Delay		25°C		2.5		V	ns
t_s	Settling to +0.1% (A_V = +1)	V_S = ±15V, 10V Step	25°C		80		V	ns
		V_S = ±5V, 5V Step	25°C		60		V	ns
dG	Differential Gain (Note 5)	NTSC/PAL	25°C		0.04		V	%
dP	Differential Phase (Note 5)	NTSC/PAL	25°C		0.15		V	°
eN	Input Noise Voltage	10 kHz	25°C		15.0		V	nV/√Hz
iN	Input Noise Current	10 kHz	25°C		1.50		V	pA/√Hz
CI STAB	Load Capacitance Stability	A_V = +1	25°C		Infinite		V	pF

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

Note 2: Measured from T_{MIN} to T_{MAX}.

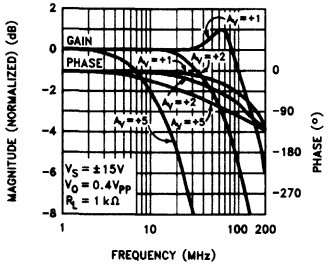
Note 3: Slew rate is measured on rising edge.

Note 4: For V_S = ±15V, V_{OUT} = 20 V_{PP}. For V_S = ±5V, V_{OUT} = 5 V_{PP}. Full-power bandwidth is based on slew rate measurement using: FPBW = SR/(2π * Vpeak).

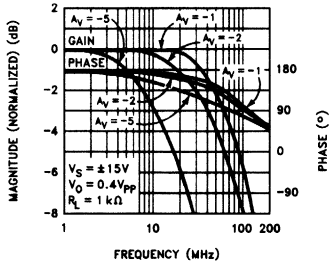
Note 5: Video Performance measured at V_S = ±15V, A_V = +2 with 2 times normal video level across R_L = 150Ω. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L, see curves.

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified)

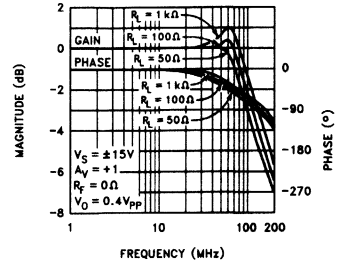
Non-Inverting Frequency Response



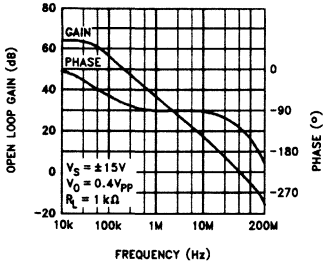
Inverting Frequency Response



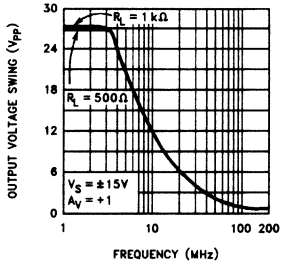
Frequency Response for Various Load Resistances



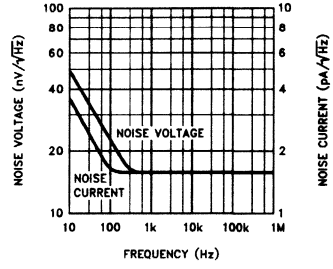
Open-Loop Gain and Phase vs Frequency



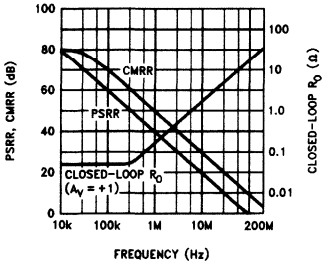
Output Voltage Swing vs Frequency



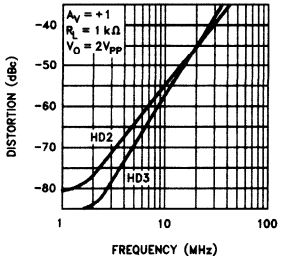
Equivalent Input Noise



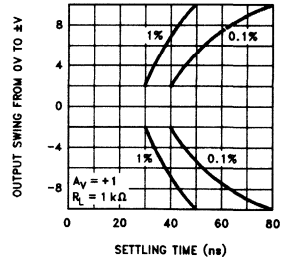
CMRR, PSRR and Closed-Loop Output Resistance vs Frequency



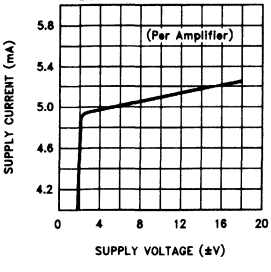
2nd and 3rd Harmonic Distortion vs Frequency



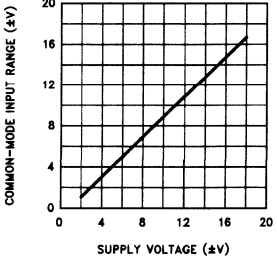
Settling Time vs Output Voltage Change



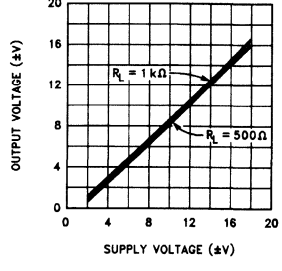
Supply Current vs Supply Voltage



Common-Mode Input Range vs Supply Voltage



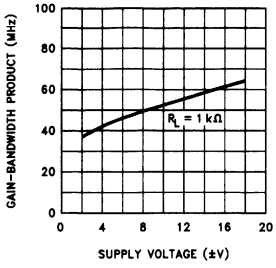
Output Voltage Range vs Supply Voltage



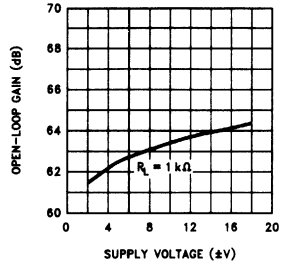
2244-3

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

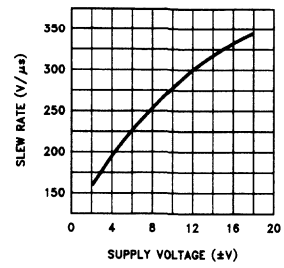
Gain-Bandwidth Product vs Supply Voltage



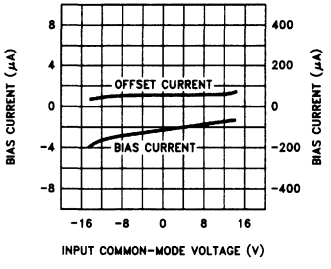
Open-Loop Gain vs Supply Voltage



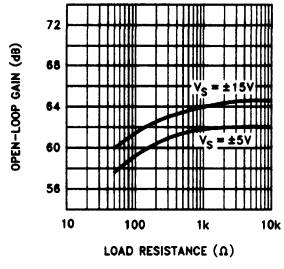
Slew-Rate vs Supply Voltage



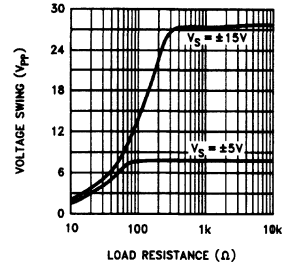
Bias and Offset Current vs Input Common-Mode Voltage



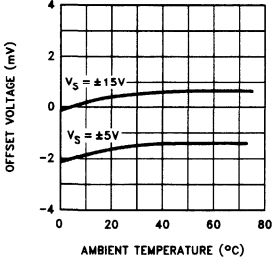
Open-Loop Gain vs Load Resistance



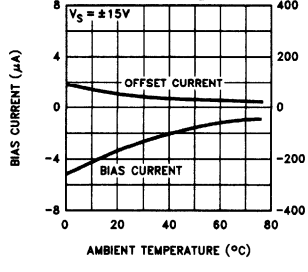
Voltage Swing vs Load Resistance



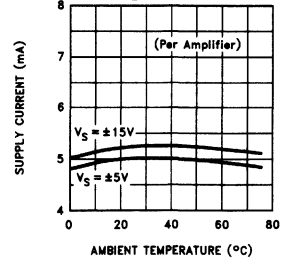
Offset Voltage vs Temperature



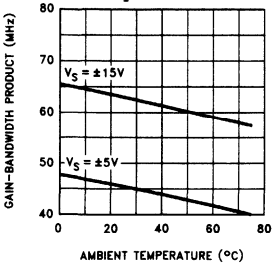
Bias and Offset Current vs Temperature



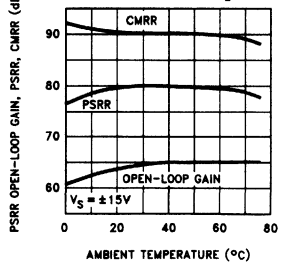
Supply Current vs Temperature



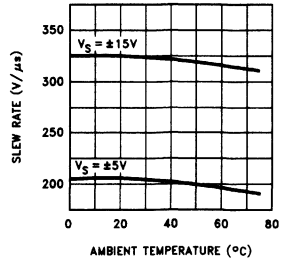
Gain-Bandwidth Product vs Temperature



Open-Loop Gain, PSRR and CMRR vs Temperature



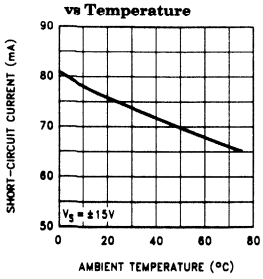
Slew Rate vs Temperature



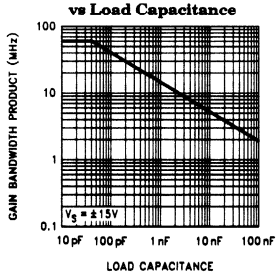
2244-4

Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

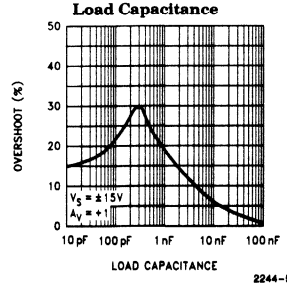
Short-Circuit Current vs Temperature



Gain-Bandwidth Product vs Load Capacitance

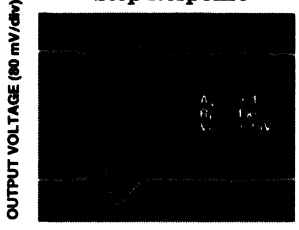


Overshoot vs Load Capacitance



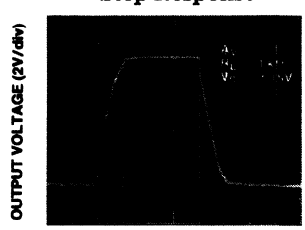
2244-5

Small-Signal Step Response



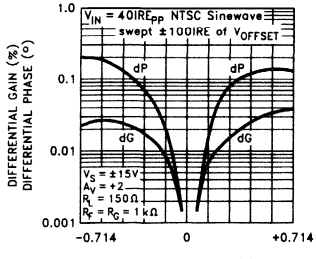
2244-6

Large-Signal Step Response

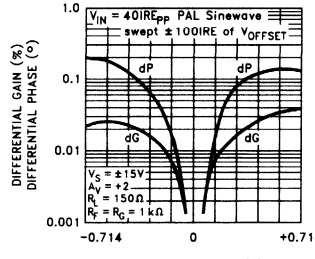


2244-7

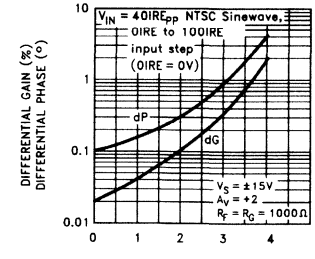
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



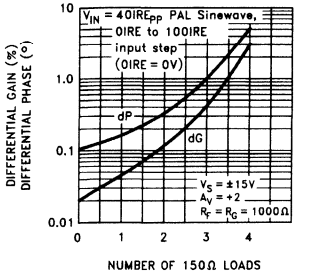
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



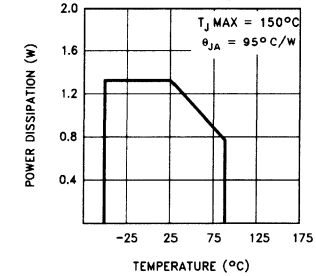
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



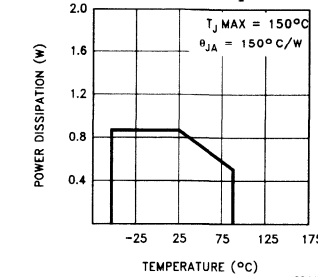
Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature



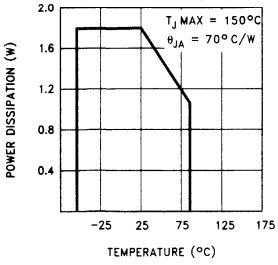
2244-8

EL2244C/EL2444C

Dual/Quad Low-Power 60 MHz Unity-Gain Stable Op Amp

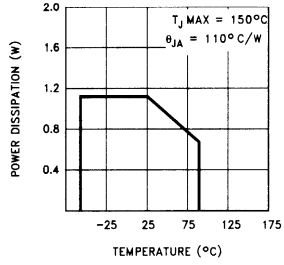
Typical Performance Curves (T_A = 25°C, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



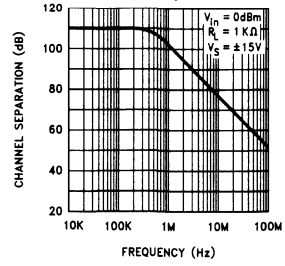
2244-9

14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



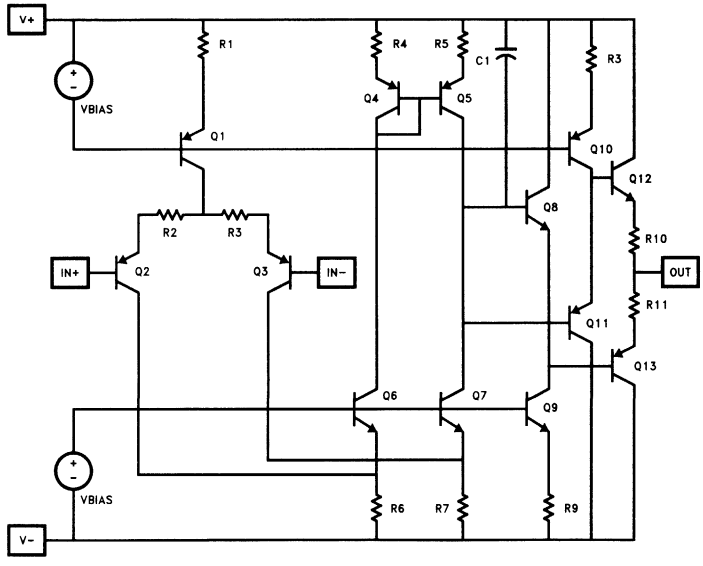
2244-10

Channel Separation
vs Frequency



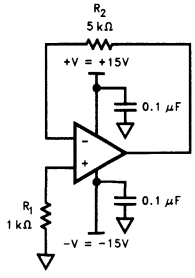
2244-11

Simplified Schematic (Per Amplifier)



2244-12

Burn-In Circuit (Per Amplifier)



2244-13

All Packages Use the Same Schematic

Applications Information

Product Description

The EL2244C/EL2444C are low-power wideband monolithic operational amplifiers built on Elantec's proprietary high-speed complementary bipolar process. The EL2244C/EL2444C use a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2244C/EL2444C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2244C/EL2444C are an excellent choice for applications such as fast log amplifiers.

Power Dissipation

With the wide power supply range and large output drive capability of the EL2244C/EL2444C, it is possible to exceed the 150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{Jmax}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2244C/EL2444C to remain in the safe operating area. These parameters are related as follows:

$$T_{Jmax} = T_{max} + (\theta_{JA} * (PDmaxtotal))$$

where PDmaxtotal is the sum of the maximum power dissipation of each amplifier in the package (PDmax). PDmax for each amplifier can be calculated as follows:

$$PDmax = (2 * V_S * I_{Smax} + (V_S - V_{outmax}) * (V_{outmax}/R_L))$$

where:

T_{max} = Maximum Ambient Temperature

θ_{JA} = Thermal Resistance of the Package

PDmax = Maximum Power Dissipation of 1 Amplifier

V_S = Supply Voltage

I_{Smax} = Maximum Supply Current of 1 Amplifier

V_{outmax} = Maximum Output Voltage Swing of the Application

R_L = Load Resistance

To serve as a guide for the user, we can calculate maximum allowable supply voltages for the example of the video cable-driver below since we know that T_{Jmax} = 150°C, T_{max} = 75°C, I_{Smax} = 7.6 mA, and the package θ_{JA}s are shown in Table 1. If we assume (for this example) that we are driving a back-terminated video cable, then the maximum average value (over duty-cycle) of V_{outmax} is 1.4V, and R_L = 150Ω, giving the results seen in Table 1.

Table 1

Duals	Package	θ_{JA}	Max PDiss @ T_{max}	Max V_S
EL2244CN	PDIP8	95°C/W	0.789W @ 75°C	±16.6V
EL2244CS	SO8	150°C/W	0.500W @ 75°C	±10.7V
QUADS				
EL2444CN	PDIP14	70°C/W	1.071W @ 75°C	±11.5V
EL2444CS	SO14	110°C/W	0.682W @ 75°C	±7.5V

Single-Supply Operation

The EL2244C/EL2444C have been designed to have a wide input and output voltage range. This design also makes the EL2244C/EL2444C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (R_L = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2244C/EL2444C still have 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth

The EL2244C/EL2444C have a gain-bandwidth product of 60 MHz while using only 5.2 mA of supply current per amplifier. For gains greater

EL2244C/EL2444C

Dual/Quad Low-Power 60 MHz Unity-Gain Stable Op Amp

Applications Information — Contd.

than 4, their closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifiers' transfer function contribute to even higher closed loop bandwidths. For example, the EL2244C/EL2444C have a −3 dB bandwidth of 120 MHz at a gain of +1, dropping to 60 MHz at a gain of +2. It is important to note that the EL2244C/EL2444C have been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2244C/EL2444C in a gain of +1 only exhibit 1.0 dB of peaking with a 1000Ω load.

Video Performance

An industry-standard method of measuring the video distortion of components such as the EL2244C/EL2444C is to measure the amount of differential gain (dG) and differential phase (dP) that they introduce. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2244C/EL2444C have been designed as an economical solution for applications requiring low video distortion. They have been thoroughly characterized for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2244C/EL2444C exhibit dG and dP of only 0.04% and 0.15° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2244C/EL2444C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

Output Drive Capability

The EL2244C/EL2444C have been designed to drive low impedance loads. They can easily drive 6 V_{PP} into a 150Ω load. This high output drive capability makes the EL2244C/EL2444C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2244C/EL2444C remains a minimum of 35 mA at low temperatures. The EL2244C/EL2444C are current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2244C/EL2444C have been designed to drive any capacitive load. However, the EL2244C/EL2444C remain stable by automatically reducing their gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2244C/EL2444C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2244C/EL2444C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum

Applications Information — Contd.

performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2244C/EL2444C Macromodel

This macromodel has been developed to assist the user in simulating the EL2244C/EL2444C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

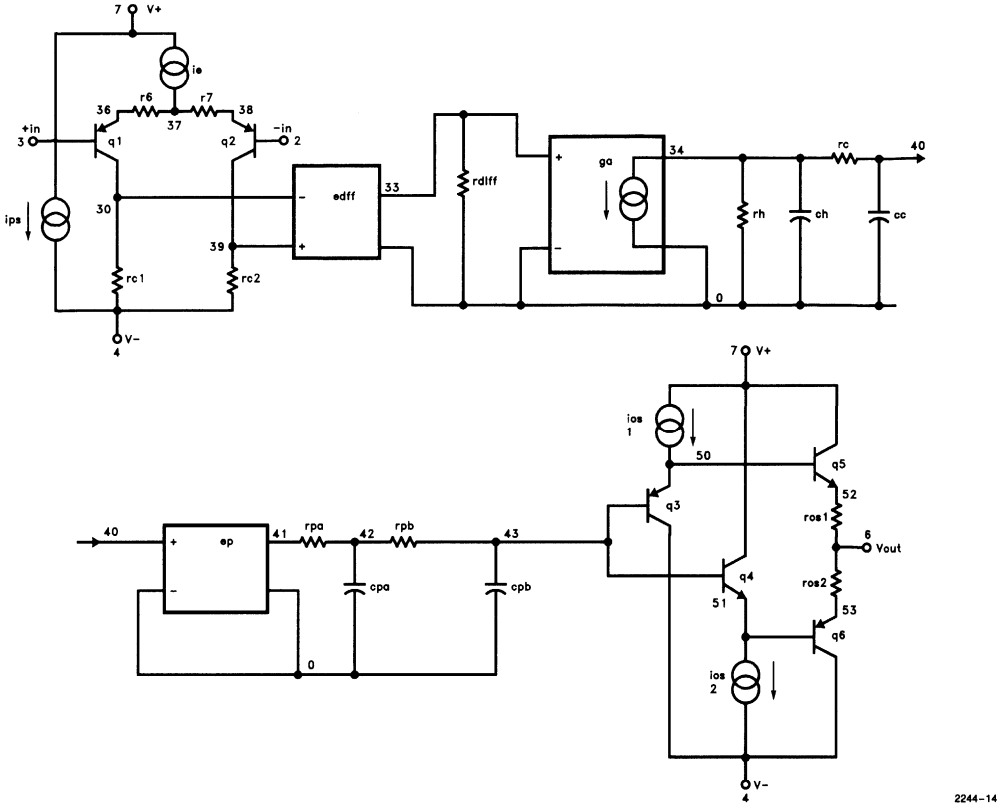
noise	non-linearities
settling-time	temperature effects
CMRR	manufacturing variations
PSRR	

```
* Connections:      +input
*                   |    -input
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    output
*                   |    |    |    |    |
.subckt M2244        3    2    7    4    6
*
* Input stage
*
ie 7 37 1mA
r6 36 37 800
r7 38 37 800
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.3pF
rc 34 40 1K
cc 40 0 1pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 200
cpa 42 0 1pF
rpb 42 43 200
cpb 43 0 1pF
*
* Output Stage
*
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
*
* Power Supply Current
*
ips 7 4 2.7mA
*
* Models
*
.model qn npn(is=800E-18 bf=200 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=100 tf=0.2nS)
.model qp pnp(is=800E-18 bf=125 tf=0.2nS)
.ends
```

EL2244C/EL2444C

Dual/Quad Low-Power 60 MHz Unity-Gain Stable Op Amp

EL2244C/EL2444C Macromodel — Contd.



2244-14

EL2244C/EL2444C Model

EL2245C/EL2445C

Dual/Quad Low-Power 100 MHz Gain-of-2 Stable Op Amp

Features

- 100 MHz gain-bandwidth product
- Gain-of-2 stable
- Low supply current (per Amplifier) = 5.2 mA at $V_S = \pm 15V$
- Wide supply range = $\pm 2V$ to $\pm 18V$ dual-supply = 2.5V to 36V single-supply
- High slew rate = 275 V/μs
- Fast settling = 80 ns to 0.1% for a 10V step
- Low differential gain = 0.02% at $A_V = +2$, $R_L = 150\Omega$
- Low differential phase = 0.07° at $A_V = +2$, $R_L = 150\Omega$
- Stable with unlimited capacitive load
- Wide output voltage swing = $\pm 13.6V$ with $V_S = \pm 15V$, $R_L = 1000\Omega$ = 3.8V/0.3V with $V_S = +5V$, $R_L = 500\Omega$

Applications

- Video amplifier
- Single-supply amplifier
- Active filters/integrators
- High-speed sample-and-hold
- High-speed signal processing
- ADC/DAC buffer
- Pulse/RF amplifier
- Pin diode receiver
- Log amplifier
- Photo multiplier amplifier
- Difference amplifier

Ordering Information

Part No.	Temp. Range	Package	Outline #
Duals			
EL2245CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2245CS	0°C to +75°C	8-Lead SO	MDP0027
Quads			
EL2445CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2445CS	0°C to +75°C	14-Lead SO	MDP0027

General Description

The EL2245C/EL2445C are dual and quad versions of the popular EL2045C. They are high speed, low power, low cost monolithic operational amplifiers built on Elantec's proprietary complementary bipolar process. The EL2245C/EL2445C are unity-gain stable and feature a 275 V/μs slew rate and 100 MHz gain-bandwidth product while requiring only 5.2 mA of supply current per amplifier.

The power supply operating range of the EL2245C/EL2445C is from $\pm 18V$ down to as little as $\pm 2V$. For single-supply operation, the EL2245C/EL2445C operate from 36V down to as little as 2.5V. The excellent power supply operating range of the EL2245C/EL2445C makes them an obvious choice for applications on a single +5V or +3V supply.

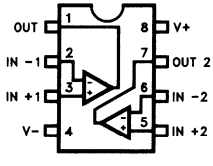
The EL2245C/EL2445C also feature an extremely wide output voltage swing of $\pm 13.6V$ with $V_S = \pm 15V$ and $R_L = 1000\Omega$. At $\pm 5V$, output voltage swing is a wide $\pm 3.8V$ with $R_L = 500\Omega$ and $\pm 3.2V$ with $R_L = 150\Omega$. Furthermore, for single-supply operation at +5V, output voltage swing is an excellent 0.3V to 3.8V with $R_L = 500\Omega$.

At a gain of +2, the EL2245C/EL2445C have a −3 dB bandwidth of 100 MHz with a phase margin of 50°. They can drive unlimited load capacitance, and because of their conventional voltage-feedback topology, the EL2245C/EL2445C allow the use of reactive or non-linear elements in their feedback network. This versatility combined with low cost and 75 mA of output-current drive make the EL2245C/EL2445C an ideal choice for price-sensitive applications requiring low power and high speed.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

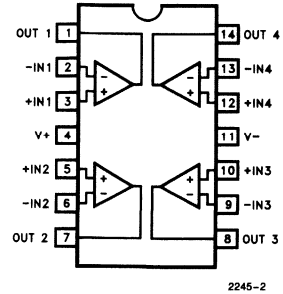
Connection Diagrams

EL2245CN/CS
Dual



2245-1

EL2445CN/CS
Quad



2245-2

EL2245C/EL2445C

Dual/Quad Low-Power 100 MHz Gain-of-2 Stable Op Amp

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±18V or 36V	Operating Junction Temperature (T_J)	150°C
Peak Output Current (I_{OP})	Short-Circuit Protected	Storage Temperature (T_{ST})	−65°C to +150°C
Output Short-Circuit Duration (Note 1)	Infinite	Lead Temperature	
Input Voltage (V_{IN})	$\pm V_S$	DIP Package (Soldering: < 5 seconds)	300°C
Differential Input Voltage (dV_{IN})	±10V	SO Package	
Power Dissipation (P_D)	See Curves	Vapor Phase (60 seconds)	215°C
Operating Temperature Range (T_A)	0°C to +75°C	Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, R_L = 1000Ω, unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	V_S = ±15V	25°C		0.5	4.0	I	mV
			T_{MIN}, T_{MAX}			6.0	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 2)	All		10.0		V	µV/°C
I_B	Input Bias Current	V_S = ±15V	25°C		2.8	8.2	I	µA
			T_{MIN}, T_{MAX}			9.2	III	µA
		V_S = ±5V	25°C		2.8		V	µA
I_{OS}	Input Offset Current	V_S = ±15V	25°C		50	300	I	nA
			T_{MIN}, T_{MAX}			400	III	nA
		V_S = ±5V	25°C		50		V	nA
TCI_{OS}	Average Offset Current Drift	(Note 2)	All		0.3		V	nA/°C
A_{VOL}	Open-Loop Gain	V_S = ±15V, V_{OUT} = ±10V, R_L = 1000Ω	25°C	1500	3000		I	V/V
			T_{MIN}, T_{MAX}	1500			III	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 500Ω	25°C		2500		V	V/V
		V_S = ±5V, V_{OUT} = ±2.5V, R_L = 150Ω	25°C		1750		V	V/V
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	25°C	70	80		I	dB
			T_{MIN}, T_{MAX}	65			III	dB

DC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1000\Omega$, unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$, $V_{OUT} = 0V$	25°C	70	90		I	dB
			T_{MIN}, T_{MAX}	70			III	dB
CMIR	Common-Mode Input Range	$V_S = \pm 15V$	25°C		±14.0		V	V
		$V_S = \pm 5V$	25°C		±4.2		V	V
		$V_S = +5V$	25°C		4.2/0.1		V	V
V_{OUT}	Output Voltage Swing	$V_S = \pm 15V$, $R_L = 1000\Omega$	25°C	±13.4	±13.6		I	V
			T_{MIN}, T_{MAX}	±13.1			III	V
		$V_S = \pm 15V$, $R_L = 500\Omega$	25°C	±12.0	±13.4		I	V
		$V_S = \pm 5V$, $R_L = 500\Omega$	25°C	±3.4	±3.8		IV	V
		$V_S = \pm 5V$, $R_L = 150\Omega$	25°C		±3.2		V	V
		$V_S = +5V$, $R_L = 500\Omega$	25°C	3.6/0.4	3.8/0.3		I	V
			T_{MIN}, T_{MAX}	3.5/0.5			III	V
I_{SC}	Output Short Circuit Current		25°C	50	75		I	mA
			T_{MIN}, T_{MAX}	35			III	mA
I_S	Supply Current (Per Amplifier)	$V_S = \pm 15V$, No Load	25°C		5.2	6.3	I	mA
			T_{MIN}			7.6	III	mA
			T_{MAX}			7.6	III	mA
		$V_S = \pm 5V$, No Load	25°C		5.0		V	mA
R_{IN}	Input Resistance	Differential	25°C		150		V	kΩ
		Common-Mode	25°C		15		V	MΩ
C_{IN}	Input Capacitance	$A_V = +1$@ 10 MHz	25°C		1.0		V	pF
R_{OUT}	Output Resistance	$A_V = +1$	25°C		50		V	mΩ
PSOR	Power-Supply Operating Range	Dual-Supply	25°C	±2.0		±18.0	V	V
		Single-Supply	25°C	2.5		36.0	V	V

Closed-Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +1$, $R_L = 1000\Omega$ unless otherwise specified

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
BW	−3 dB Bandwidth (V_{OUT} = 0.4 V_{PP})	$V_S = \pm 15V$, $A_V = +2$	25°C		100		V	MHz
		$V_S = \pm 15V$, $A_V = -1$	25°C		75		V	MHz
		$V_S = \pm 15V$, $A_V = +5$	25°C		20		V	MHz
		$V_S = \pm 15V$, $A_V = +10$	25°C		10		V	MHz
		$V_S = \pm 15V$, $A_V = +20$	25°C		5		V	MHz
		$V_S = \pm 5V$, $A_V = +2$	25°C		75		V	MHz
GBWP	Gain-Bandwidth Product	$V_S = \pm 15V$	25°C		100		V	MHz
		$V_S = \pm 5V$	25°C		75		V	MHz

Closed-Loop AC Electrical Characteristics

V_S = ±15V, A_V = +2, R_L = 1000Ω unless otherwise specified — Contd.

Parameter	Description	Condition	Temp	Min	Typ	Max	Test Level	Units
PM	Phase Margin	R_L = 1 kΩ, C_L = 10 pF	25°C		50		V	°
CS	Channel Separation	f = 5 MHz	25°C		85		V	dB
SR	Slew Rate (Note 3)	V_S = ±15V, R_L = 1000Ω	25°C	200	275		I	V/µs
		V_S = ±5V, R_L = 500Ω	25°C		200		V	V/µs
FPBW	Full-Power Bandwidth (Note 4)	V_S = ±15V	25°C	3.2	4.4		I	MHz
		V_S = ±5V	25°C		12.7		V	MHz
t_r, t_f	Rise Time, Fall Time	0.1V Step	25°C		3.0		V	ns
OS	Overshoot	0.1V Step	25°C		20		V	%
t_{PD}	Propagation Delay		25°C		2.5		V	ns
t_s	Settling to +0.1% (A_V = +1)	V_S = ±15V, 10V Step	25°C		80		V	ns
		V_S = ±5V, 5V Step	25°C		60		V	ns
dG	Differential Gain (Note 5)	NTSC/PAL	25°C		0.02		V	%
dP	Differential Phase (Note 5)	NTSC/PAL	25°C		0.07		V	°
eN	Input Noise Voltage	10 kHz	25°C		15.0		V	nV/√Hz
iN	Input Noise Current	10 kHz	25°C		1.50		V	pA/√Hz
CI STAB	Load Capacitance Stability	A_V = +1	25°C		Infinite		V	pF

Note 1: A heat-sink is required to keep junction temperature below absolute maximum when an output is shorted.

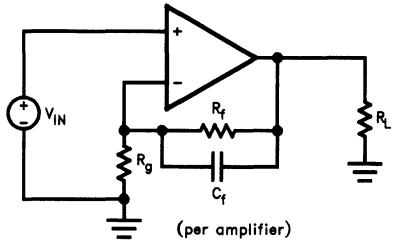
Note 2: Measured from T_{MIN} to T_{MAX}.

Note 3: Slew rate is measured on rising edge.

Note 4: For V_S = ±15V, V_{OUT} = 20 V_{PP}. For V_S = ±5V, V_{OUT} = 5 V_{PP}. Full-power bandwidth is based on slew rate measurement using: FPBW = SR/(2π * Vpeak).

Note 5: Video Performance measured at V_S = ±15V, A_V = +2 with 2 times normal video level across R_L = 150Ω. This corresponds to standard video levels across a back-terminated 75Ω load. For other values of R_L, see curves.

EL2245C/EL2445C Test Circuit

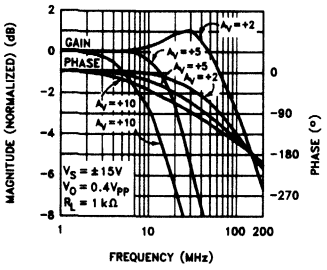


2245-3

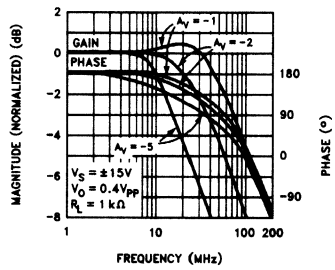
Typical Performance Curves

(T_A = 25°C, R_F = 1 kΩ, C_F = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified)

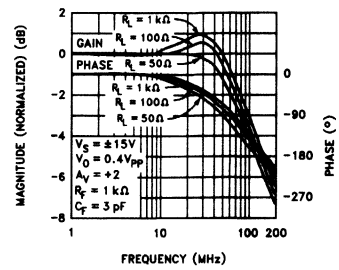
Non-Inverting Frequency Response



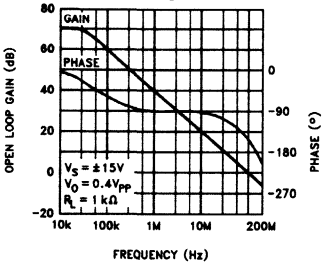
Inverting Frequency Response



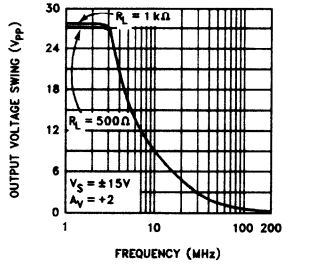
Frequency Response for Various Load Resistances



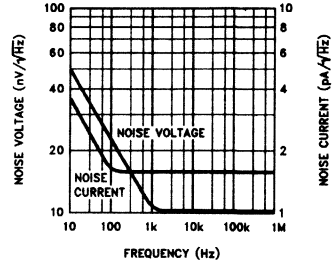
Open-Loop Gain and Phase vs Frequency



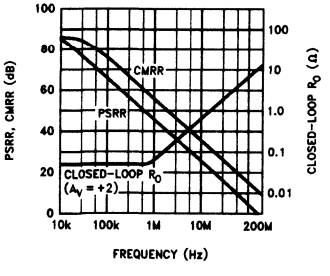
Output Voltage Swing vs Frequency



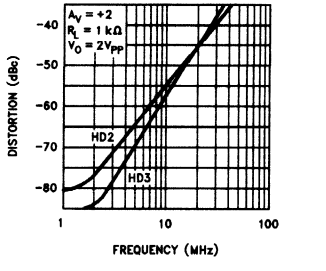
Equivalent Input Noise



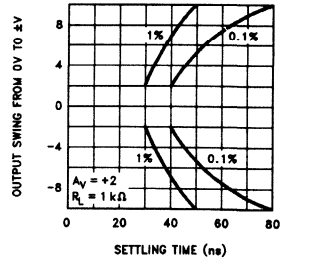
CMRR, PSRR and Closed-Loop Output Resistance vs Frequency



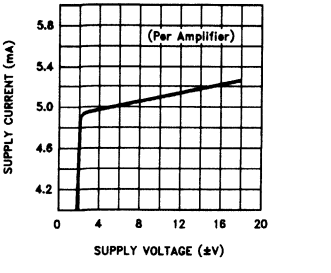
2nd and 3rd Harmonic Distortion vs Frequency



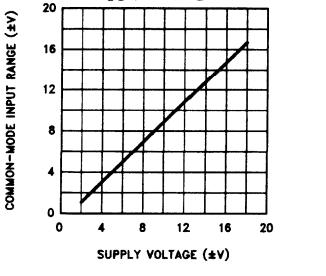
Settling Time vs Output Voltage Change



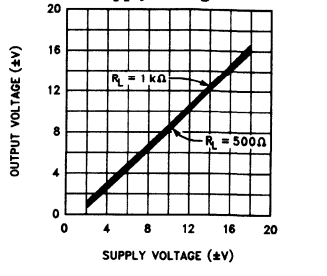
Supply Current vs Supply Voltage



Common-Mode Input Range vs Supply Voltage



Output Voltage Range vs Supply Voltage

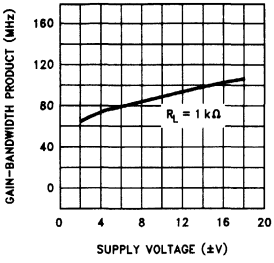


2245-4

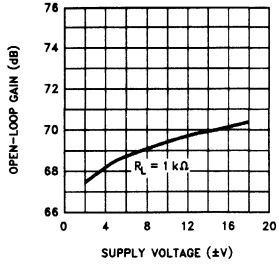
Typical Performance Curves

(T_A = 25°C, R_F = 1 kΩ, C_F = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified) — Contd.

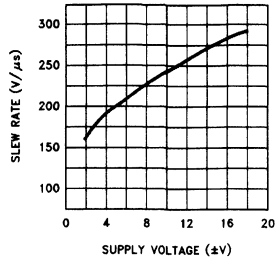
Gain-Bandwidth Product vs Supply Voltage



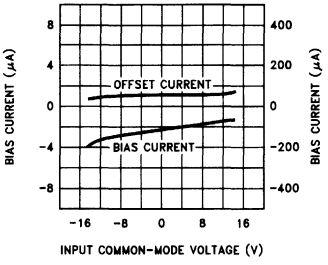
Open-Loop Gain vs Supply Voltage



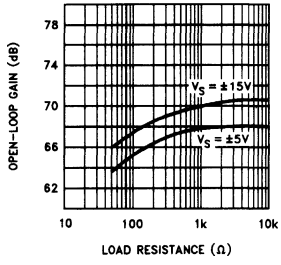
Slew-Rate vs Supply Voltage



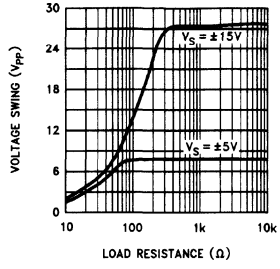
Bias and Offset Current vs Input Common-Mode Voltage



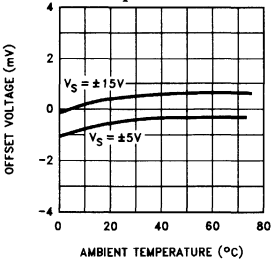
Open-Loop Gain vs Load Resistance



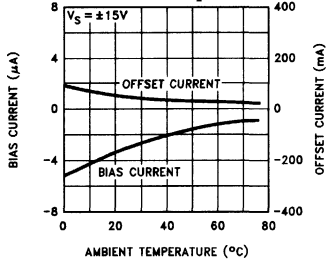
Voltage Swing vs Load Resistance



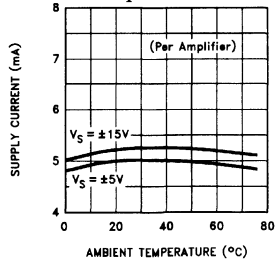
Offset Voltage vs Temperature



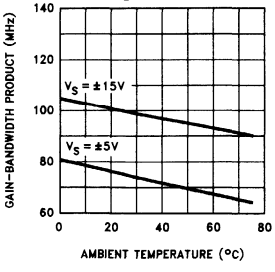
Bias and Offset Current vs Temperature



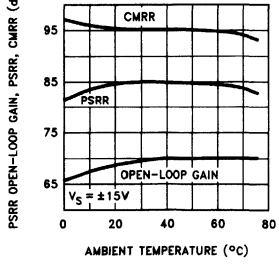
Supply Current vs Temperature



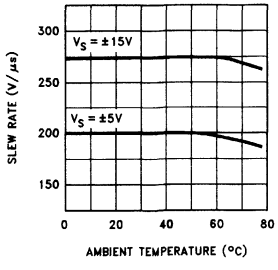
Gain-Bandwidth Product vs Temperature



Open-Loop Gain PSRR and CMRR vs Temperature



Slew Rate vs Temperature

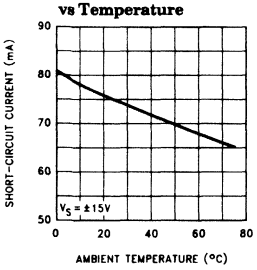


2245-5

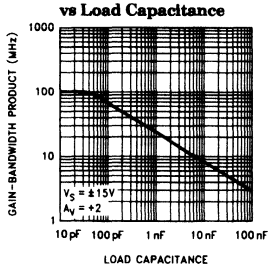
Typical Performance Curves

(T_A = 25°C, R_F = 1 kΩ, C_F = 3 pF, R_L = 1000Ω, A_V = +2 unless otherwise specified) — Contd.

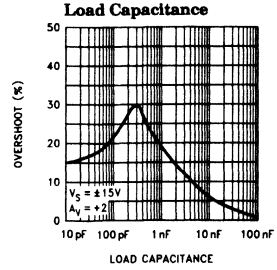
Short-Circuit Current vs Temperature



Gain-Bandwidth Product vs Load Capacitance

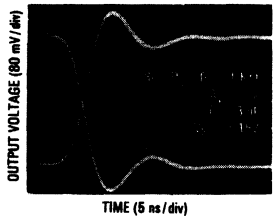


Overshoot vs Load Capacitance

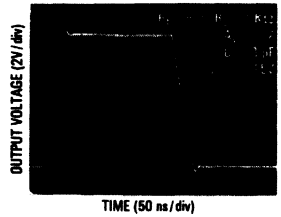


2245-6

Small-Signal Step Response



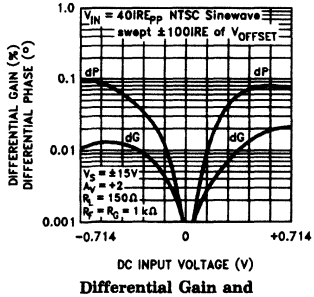
Large-Signal Step Response



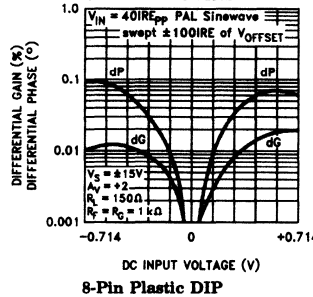
2245-7

2245-8

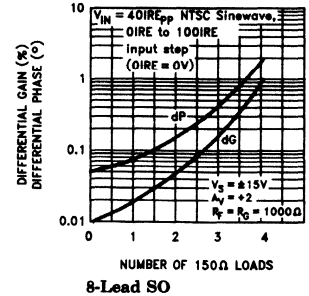
Differential Gain and Phase vs DC Input Offset at 3.58 MHz



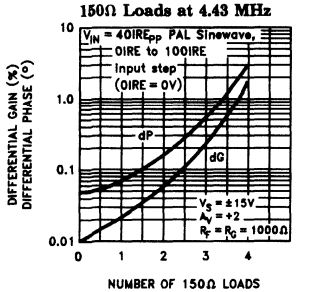
Differential Gain and Phase vs DC Input Offset at 4.43 MHz



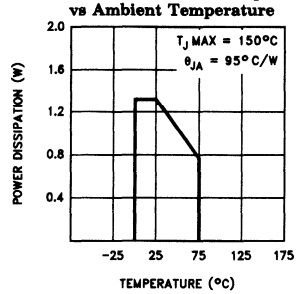
Differential Gain and Phase vs Number of 150Ω Loads at 3.58 MHz



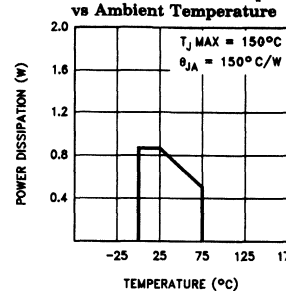
Differential Gain and Phase vs Number of 150Ω Loads at 4.43 MHz



8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead SO Maximum Power Dissipation vs Ambient Temperature



2245-9

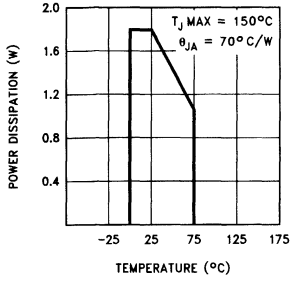
EL2245C/EL2445C

Dual/Quad Low-Power 100 MHz Gain-of-2 Stable Op Amp

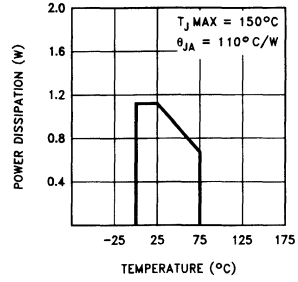
Typical Performance Curves

(T_A = 25°C, R_F = 1 kΩ, C_F = 3 pF, R_L = 1000Ω, A_V = +1 unless otherwise specified) — Contd.

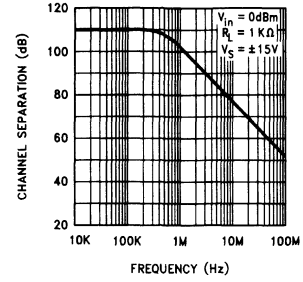
14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature

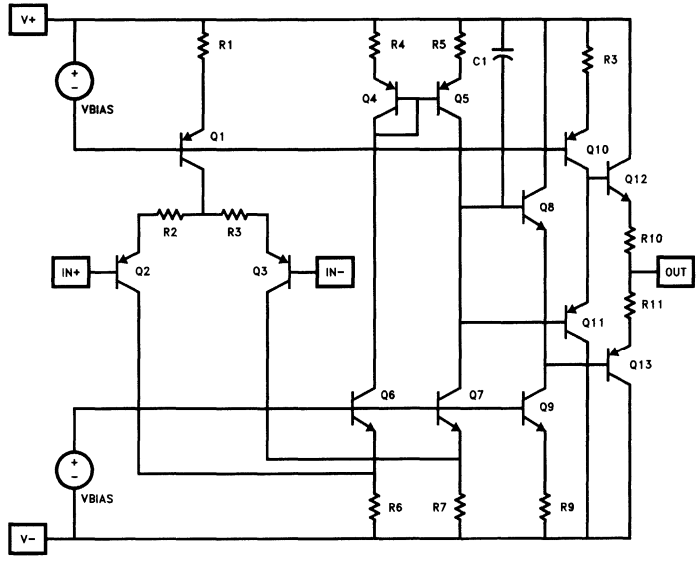


Channel Separation
vs Frequency



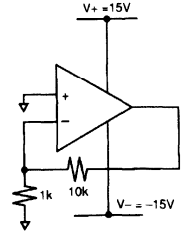
2245-10

Simplified Schematic (Per Amplifier)



2245-11

Burn-In Circuit (Per Amplifier)



2245-12

All Packages Use the Same Schematic

Applications Information

Product Description

The EL2245C/EL2445C are dual and quad low-power wideband monolithic operational amplifiers built on Elantec's proprietary high-speed complementary bipolar process. The EL2245C/EL2445C use a classical voltage-feedback topology which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2245C/EL2445C allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2245C/EL2445C are an excellent choice for applications such as fast log amplifiers.

Power Dissipation

With the wide power supply range and large output drive capability of the EL2245C/EL2445C, it is possible to exceed the 150°C maximum junction temperatures under certain load and power-supply conditions. It is therefore important to calculate the maximum junction temperature (T_{Jmax}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2245C/EL2445C to remain in the safe operating area. These parameters are related as follows:

$$T_{Jmax} = T_{max} + (\theta_{JA} * (PDmaxtotal))$$

where PDmaxtotal is the sum of the maximum power dissipation of each amplifier in the package (PDmax). PDmax for each amplifier can be calculated as follows:

$$PDmax = (2*V_S*I_{Smax} + (V_S - V_{outmax})*(V_{outmax}/R_L))$$

where:

T_{max} = Maximum Ambient Temperature

θ_{JA} = Thermal Resistance of the Package

PDmax = Maximum Power Dissipation of 1 Amplifier

V_S = Supply Voltage

I_{Smax} = Maximum Supply Current of 1 Amplifier

V_{outmax} = Maximum Output Voltage Swing of the Application

R_L = Load Resistance

To serve as a guide for the user, we can calculate maximum allowable supply voltages for the example of the video cable-driver below since we know that T_{Jmax} = 150°C, T_{max} = 75°C, I_{Smax} = 7.6 mA, and the package θ_{JA}s are shown in Table 1. If we assume (for this example) that we are driving a back-terminated video cable, then the maximum average value (over duty-cycle) of V_{outmax} is 1.4V, and R_L = 150Ω, giving the results seen in Table 1.

Table 1

Duals	Package	θ_{JA}	Max PDiss @ T_{max}	Max V_S
EL2245CN	PDIP8	95°C/W	0.789W @ 75°C	±16.6V
EL2245CS	SO8	150°C/W	0.500W @ 75°C	±10.7V
QUADS				
EL2445CN	PDIP14	70°C/W	1.071W @ 75°C	±11.5V
EL2445CS	SO14	110°C/W	0.682W @ 75°C	±7.5V

Single-Supply Operation

The EL2245C/EL2445C have been designed to have a wide input and output voltage range. This design also makes the EL2245C/EL2445C an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 100 mV of ground (R_L = 500Ω), and the lower output voltage range is within 300 mV of ground. Upper input voltage range reaches 4.2V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 3.5V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 36V or as low as 2.5V. On a single 2.5V supply, the EL2245C/EL2445C still have 1V of output swing.

Gain-Bandwidth Product and the −3 dB Bandwidth

The EL2245C/EL2445C have a gain-bandwidth product of 100 MHz while using only 5.2 mA of supply current per amplifier. For gains greater

EL2245C/EL2445C

Dual/Quad Low-Power 100 MHz Gain-of-2 Stable Op Amp

Applications Information — Contd.

than 4, their closed-loop −3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 4, higher-order poles in the amplifiers' transfer function contribute to even higher closed loop bandwidths. For example, the EL2245C/EL2445C have a −3 dB bandwidth of 100 MHz at a gain of +2, dropping to 20 MHz at a gain of +5. It is important to note that the EL2245C/EL2445C have been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2245C/EL2445C in a gain of +2 only exhibit 1.0 dB of peaking with a 1000Ω load.

Video Performance

An industry-standard method of measuring the video distortion of components such as the EL2245C/EL2445C is to measure the amount of differential gain (dG) and differential phase (dP) that they introduce. To make these measurements, a 0.286 V_{PP} (40 IRE) signal is applied to the device with 0V DC offset (0 IRE) at either 3.58 MHz for NTSC or 4.43 MHz for PAL. A second measurement is then made at 0.714V DC offset (100 IRE). Differential gain is a measure of the change in amplitude of the sine wave, and is measured in percent. Differential phase is a measure of the change in phase, and is measured in degrees.

For signal transmission and distribution, a back-terminated cable (75Ω in series at the drive end, and 75Ω to ground at the receiving end) is preferred since the impedance match at both ends will absorb any reflections. However, when double termination is used, the received signal is halved; therefore a gain of 2 configuration is typically used to compensate for the attenuation.

The EL2245C/EL2445C have been designed as an economical solution for applications requiring low video distortion. They have been thoroughly characterized for video performance in the topology described above, and the results have been included as typical dG and dP specifications and as typical performance curves. In a gain of +2, driving 150Ω, with standard video test levels at the input, the EL2245C/EL2445C exhibit dG and dP of only 0.02% and 0.07° at NTSC and PAL. Because dG and dP can vary with different DC offsets, the video performance of the EL2245C/EL2445C has been characterized over the entire DC offset range from −0.714V to +0.714V. For more information, refer to the curves of dG and dP vs DC Input Offset.

Output Drive Capability

The EL2245C/EL2445C have been designed to drive low impedance loads. They can easily drive 6 V_{PP} into a 150Ω load. This high output drive capability makes the EL2245C/EL2445C an ideal choice for RF, IF and video applications. Furthermore, the current drive of the EL2245C/EL2445C remains a minimum of 35 mA at low temperatures. The EL2245C/EL2445C are current-limited at the output, allowing it to withstand shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

For ease of use, the EL2245C/EL2445C have been designed to drive any capacitive load. However, the EL2245C/EL2445C remain stable by automatically reducing their gain-bandwidth product as capacitive load increases. Therefore, for maximum bandwidth, capacitive loads should be reduced as much as possible or isolated via a series output resistor (Rs). Similarly, coax lines can be driven, but best AC performance is obtained when they are terminated with their characteristic impedance so that the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier. Although stable with all capacitive loads, some peaking still occurs as load capacitance increases. A series resistor at the output of the EL2245C/EL2445C can be used to reduce this peaking and further improve stability.

Printed-Circuit Layout

The EL2245C/EL2445C are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum

Applications Information — Contd.

performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1 μF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5 kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

The EL2245C/EL2445C Macromodel

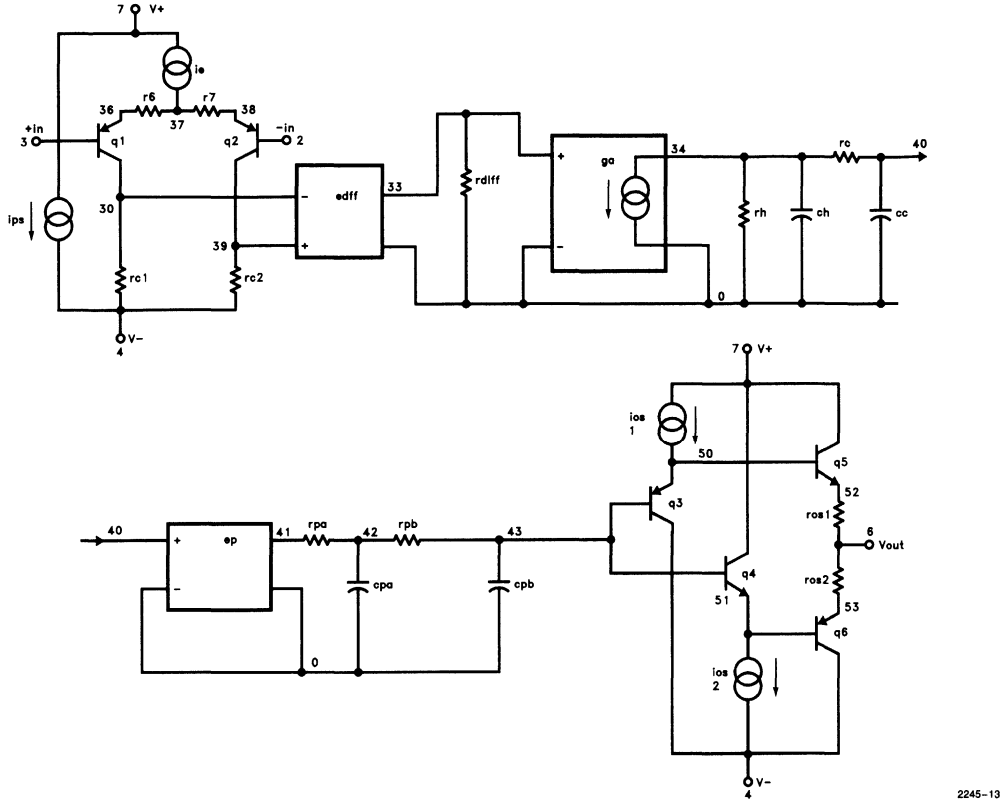
This macromodel has been developed to assist the user in simulating the EL2245C/EL2445C with surrounding circuitry. It has been developed for the PSPICE simulator (copywritten by the Microsim Corporation), and may need to be rearranged for other simulators. It approximates DC, AC, and transient response for resistive loads, but does not accurately model capacitive loading. This model is slightly more complicated than the models used for low-frequency op-amps, but it is much more accurate for AC analysis.

The model does not simulate these characteristics accurately:

noise	non-linearities
settling-time	temperature effects
CMRR	manufacturing variations
PSRR	

```
* Connections:      +input
*                   |    -input
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    output
*                   |    |    |    |    |
.subckt M2245       3    2    7    4    6
*
* Input stage
*
ie 7 37 1mA
r6 36 37 400
r7 38 37 400
rc1 4 30 850
rc2 4 39 850
q1 30 3 36 qp
q2 39 2 38 qpa
ediff 33 0 39 30 1.0
rdiff 33 0 1Meg
*
* Compensation Section
*
ga 0 34 33 0 1m
rh 34 0 2Meg
ch 34 0 1.3pF
rc 34 40 1K
cc 40 0 1pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 200
cpa 42 0 1pF
rpb 42 43 200
cpb 43 0 1pF
*
* Output Stage
*
ios1 7 50 1.0mA
ios2 51 4 1.0mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
*
* Power Supply Current
*
ips 7 4 2.7mA
*
* Models
*
.model qn npn(is=800E-18 bf=200 tf=0.2nS)
.model qpa pnp(is=864E-18 bf=100 tf=0.2nS)
.model qp pnp(is=800E-18 bf=125 tf=0.2nS)
.ends
```

EL2245C/EL2445C Macromodel — Contd.



2245-13

EL2245C/EL2445C Model

EL2260C/EL2460C

Dual/Quad 130 MHz Current Feedback Amplifiers

Features

- 130 MHz 3 dB bandwidth (A_V = +2)
- 180 MHz 3 dB bandwidth (A_V = +1)
- 0.01% differential gain, R_L = 500Ω
- 0.01° differential phase, R_L = 500Ω
- Low supply current, 7.5 mA per amplifier
- Wide supply range, ±2V to ±15V
- 80 mA output current (peak)
- Low cost
- 1500 V/μs slew rate
- Input common mode range to within 1.5V of supplies
- 35 ns settling time to 0.1%

Applications

- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment amplifiers
- Current to voltage converter

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2260CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2260CS	0°C to +75°C	8-Pin SOIC	MDP0027
EL2460CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2460CS	0°C to +75°C	14-Pin SOIC	MDP0027

General Description

The EL2260C/EL2460C are dual/quad current feedback operational amplifiers with −3 dB bandwidth of 130 MHz at a gain of +2. Built using the Elantec proprietary monolithic complementary bipolar process, these amplifers use current mode feedback to achieve more bandwidth at a given gain than a conventional voltage feedback operational amplifier.

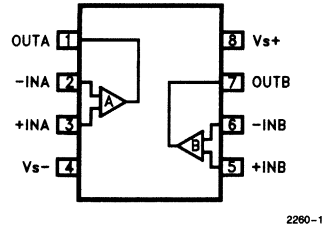
The EL2260C/EL2460C are designed to drive a double terminated 75Ω coax cable to video levels. Differential gain and phase are excellent when driving both loads of 500Ω (<0.01%/<0.01°) and double terminated 75Ω cables (0.025%/0.1°).

The amplifiers can operate on any supply voltage from 4V (±2V) to 33V (±16.5V), yet consume only 7.5 mA per amplifier at any supply voltage. Using industry standard pinouts, the EL2260C is available in 8-pin P-DIP and 8-pin SO packages, while the EL2460C is available in 14-pin P-DIP and 14-pin SO packages.

Elantec's facilities comply with MIL-I-45208A and offer applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing—Monolithic Products.*

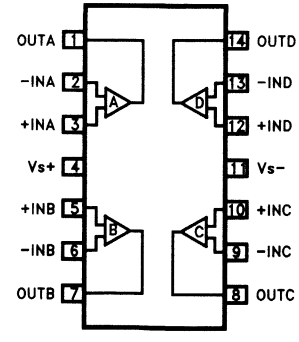
Connection Diagrams

EL2260C SO, P-DIP Packages



Top View

EL2460C SO, P-DIP Packages



Top View

EL2260C/EL2460C
Dual/Quad 130 MHz Current Feedback Amplifiers

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S^+ and V_S^-	+33V	Storage Temperature Range	−65°C to +150°C
Voltage between +IN and −IN	±6V	Lead Temperature	
Current into +IN or −IN	10 mA	DIP Package	
Internal Power Dissipation	See Curves	(Soldering, <10 seconds)	300°C
Operating Ambient Temperature Range	0°C to +75°C	SO Package	
Operating Junction Temperature		Vapor Phase (60 seconds)	215°C
Plastic Packages	150°C	Infrared (15 seconds)	220°C
		Output Current	±50 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2260C EL2460C	
V_{OS}	Input Offset Voltage	V_S = ±5V, ±15V	25°C		2	10	I	mV
			T_{MIN}, T_{MAX}			15	III	mV
TC V_{OS}	Average Offset Voltage Drift (Note 1)		Full		10		V	µV/°C
$+I_{IN}$	+Input Current	V_S = ±5V, ±15V	25°C		0.5	3	I	µA
			T_{MIN}, T_{MAX}			10	III	µA
$-I_{IN}$	−Input Current	V_S = ±5V, ±15V	25°C		5	25	I	µA
			T_{MIN}, T_{MAX}			35	III	µA
CMRR	Common Mode Rejection Ratio (Note 2)	V_S = ±5V, ±15V	Full	50	55		II	dB
−ICMR	−Input Current Common Mode Rejection (Note 2)	V_S = ±5V, ±15V	25°C		0.2	5	I	µA/V
			T_{MIN}, T_{MAX}			5	III	µA/V
PSRR	Power Supply Rejection Ratio (Note 3)		Full	75	95		II	dB
−IPSR	−Input Current Power Supply Rejection (Note 3)		25°C		0.2	5	I	µA/V
			T_{MIN}, T_{MAX}			5	III	µA/V

Open Loop DC Electrical Characteristics — Contd.

V_S = ±15V, R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Conditions	Temp	Limits			Test Level	Units
				Min	Typ	Max	EL2260C EL2460C	
R_{OL}	Transimpedance (Note 4)	V_S = ±15V R_L = 400Ω	25°C T_{MIN}, T_{MAX}	500 250	2000		I III	kΩ kΩ
		V_S = ±5V R_L = 150Ω	25°C T_{MIN}, T_{MAX}	500 250	1800		I III	kΩ kΩ
$+R_{IN}$	+Input Resistance		Full	1.5	3.0		II	MΩ
$+C_{IN}$	+Input Capacitance		25°C		2.5		V	pF
CMIR	Common Mode Input Range	V_S = ±15V	25°C		±13.5		V	V
		V_S = ±5V	25°C		±3.5		V	V
V_O	Output Voltage Swing	R_L = 400Ω, V_S = ±15V	25°C T_{MIN}, T_{MAX}	±12 ±11	±13.5		I III	V V
		R_L = 150Ω, V_S = ±15V	25°C		±12		V	V
		R_L = 150Ω, V_S = ±5V	25°C T_{MIN}, T_{MAX}	±3.0 ±2.5	±3.7		I III	V V
I_{SC}	Output Short Circuit Current (Note 4)	V_S = ±5V, V_S = ±15V	25°C	60	100	150	I	mA
I_S	Supply Current (Per Amplifier)	V_S = ±15V	25°C T_{MIN}, T_{MAX}		7.5	10.0 10.0	I III	mA mA
		V_S = ±5V	25°C T_{MIN}, T_{MAX}		5.4	7.5 7.5	I III	mA mA

EL2260C/EL2460C
Dual/Quad 130 MHz Current Feedback Amplifiers

Closed Loop AC Electrical Characteristics

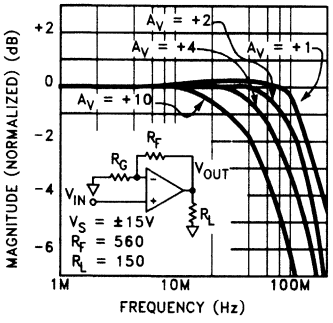
$V_S = \pm 15V$, $A_V = +2$, $R_F = 560\Omega$, $R_L = 150\Omega$, $T_A = 25°C$ unless otherwise noted

Parameter	Description	Test Conditions	Limits			Test Level	Units
			Min	Typ	Max	EL2260C EL2460C	
BW	−3 dB Bandwidth (Note 8)	$V_S = \pm 15V$, $A_V = +2$		130		V	MHz
		$V_S = \pm 15V$, $A_V = +1$		180		V	MHz
		$V_S = \pm 5V$, $A_V = +2$		100		V	MHz
		$V_S = \pm 5V$, $A_V = +1$		110		V	MHz
SR	Slew Rate (Notes 6, 8)	$R_L = 400\Omega$	1000	1500		IV	V/μs
		$R_F = 1K\Omega$, $R_G = 110\Omega$, $R_L = 400\Omega$		1500		V	V/μs
t_r, t_f	Rise Time, Fall Time, (Note 8)	$V_{OUT} = \pm 500mV$		2.7		V	ns
t_{pd}	Propagation Delay (Note 8)			3.2		V	ns
OS	Overshoot (Note 8)	$V_{OUT} = \pm 500$ mV		0		V	%
t_s	0.1% Settling Time (Note 8)	$V_{OUT} = \pm 10V$, $A_V = -1$, $R_L = 1K$		35		V	ns
dG	Differential Gain (Notes 7, 8)	$R_L = 150\Omega$		0.025		V	%
		$R_L = 500\Omega$		0.006		V	%
dP	Differential Phase (Notes 7, 8)	$R_L = 150\Omega$		0.1		V	deg (°)
		$R_L = 500\Omega$		0.005		V	deg (°)

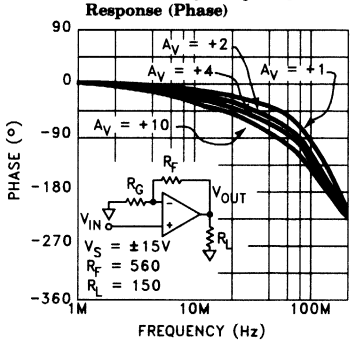
Note 1: Measured from T_{MIN} to T_{MAX}.
Note 2: $V_{CM} = \pm 13V$ for $V_S = \pm 15V$ and $T_A = 25°C$
$V_{CM} = \pm 12V$ for $V_S = \pm 15V$ and $T_A = T_{MIN}$, T_{MAX}
$V_{CM} = \pm 3V$ for $V_S = \pm 5V$ and $T_A = 25°C$
$V_{CM} = \pm 2V$ for $V_S = \pm 5V$ and $T_A = T_{MIN}$, T_{MAX}
Note 3: The supplies are moved from $\pm 2.5V$ to $\pm 15V$.
Note 4: $V_{OUT} = \pm 7V$ for $V_S = \pm 15V$, and $V_{OUT} = \pm 2V$ for $V_S = \pm 5V$.
Note 5: A heat sink is required to keep junction temperature below absolute maximum when an output is shorted.
Note 6: Slew Rate is with V_{OUT} from $+10V$ to $-10V$ and measured at the 25% and 75% points.
Note 7: DC offset from $-0.714V$ through $+0.714V$, AC amplitude 286 mV_{p-p}, f = 3.58 MHz.
Note 8: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

Typical Performance Curves

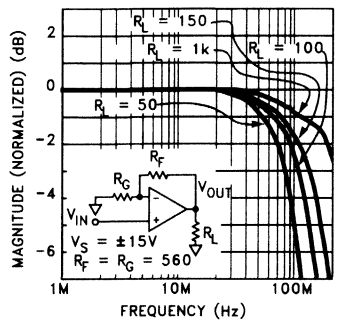
Non-Inverting Frequency Response (Gain)



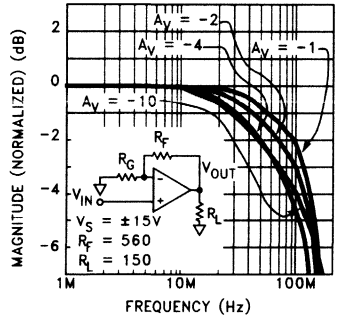
Non-Inverting Frequency Response (Phase)



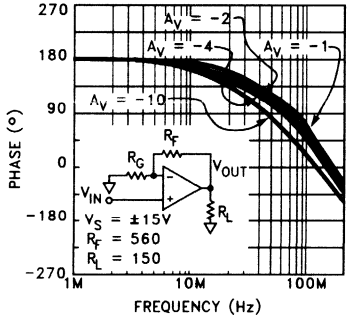
Frequency Response for Various R_L



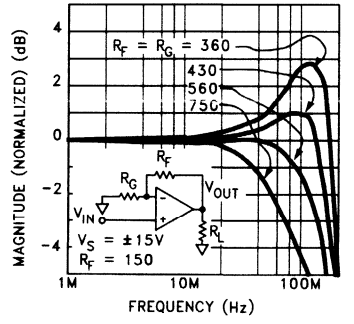
Inverting Frequency Response (Gain)



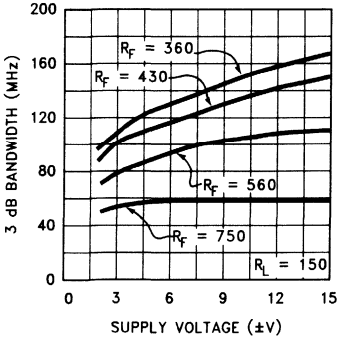
Inverting Frequency Response (Phase)



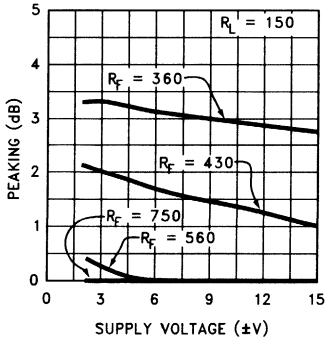
Frequency Response for Various R_F and R_G



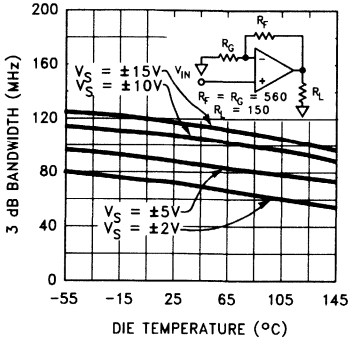
3 dB Bandwidth vs Supply Voltage for $A_V = -1$



Peaking vs Supply Voltage for $A_V = -1$



3 dB Bandwidth vs Temperature for $A_V = -1$



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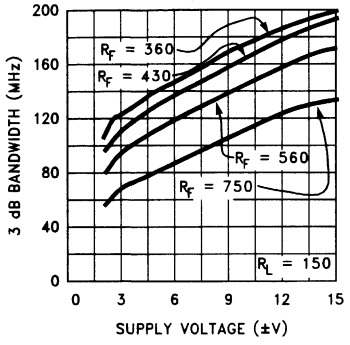
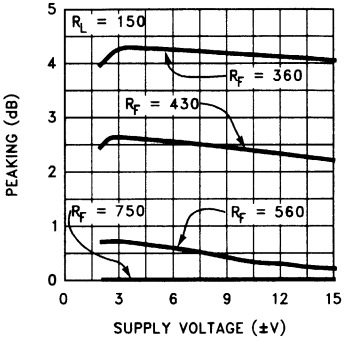
Typical Performance Curves — Contd.

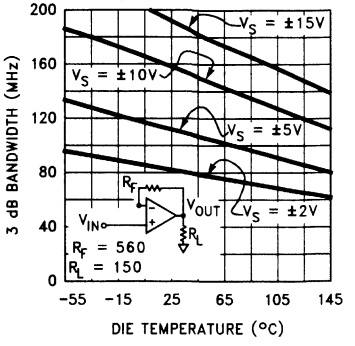
3 dB Bandwidth vs Supply Voltage for A_V = +1



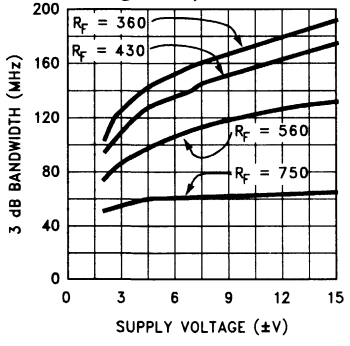
Peaking vs Supply Voltage for A_V = +1



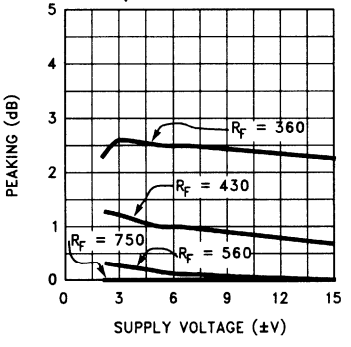
3 dB Bandwidth vs Temperature for A_V = +1



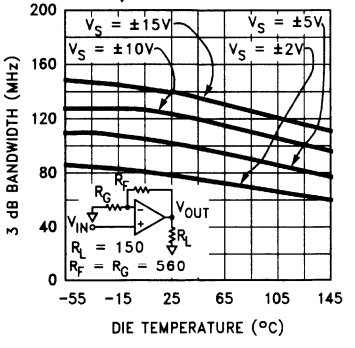
3 dB Bandwidth vs Supply Voltage for A_V = +2



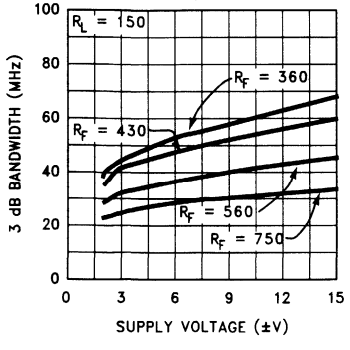
Peaking vs Supply Voltage for A_V = +2



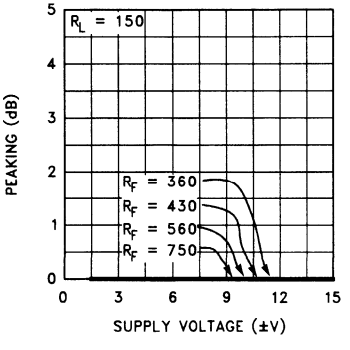
3 dB Bandwidth vs Temperature for A_V = +2



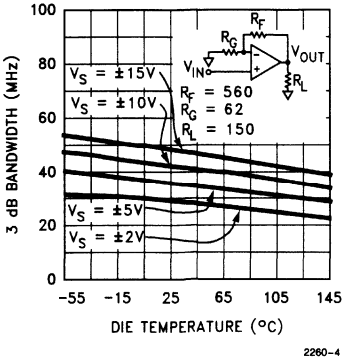
3 dB Bandwidth vs Supply Voltage for A_V = +10



Peaking vs Supply Voltage for A_V = +10



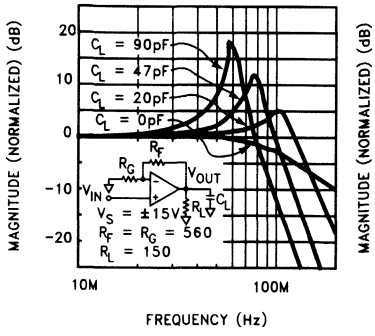
3 dB Bandwidth vs Temperature for A_V = +10



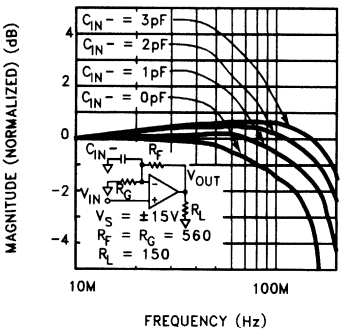
2260-4

Typical Performance Curves — Contd.

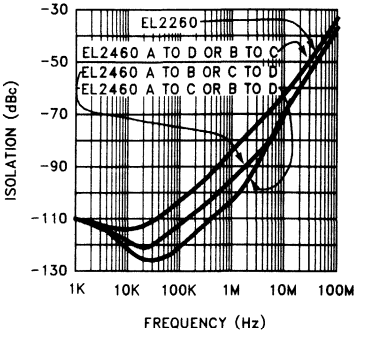
Frequency Response for Various C_L



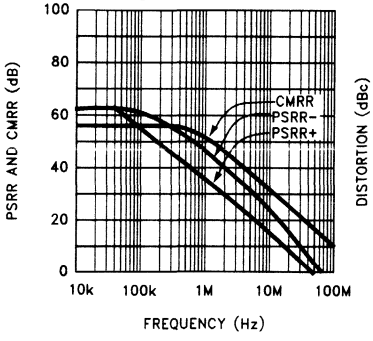
Frequency Response for Various C_{IN-}



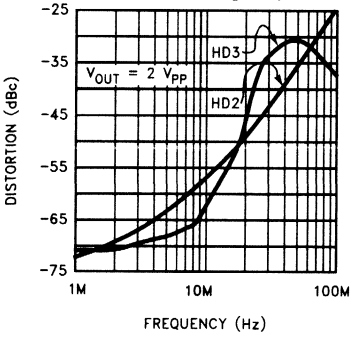
Channel to Channel Isolation vs Frequency



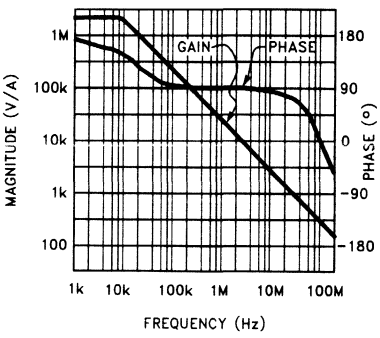
PSRR and CMRR vs Frequency



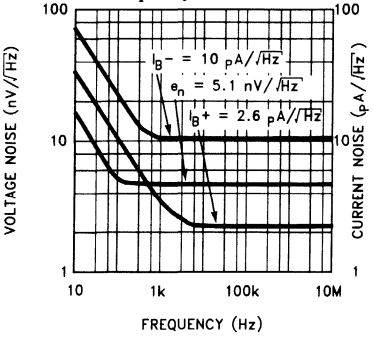
2nd and 3rd Harmonic Distortion vs Frequency



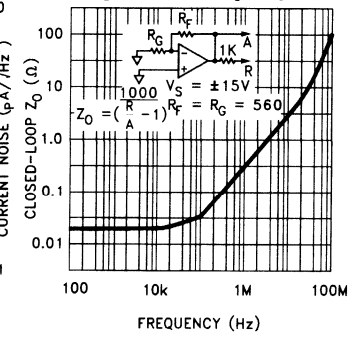
Transimpedance (R_{OL}) vs Frequency



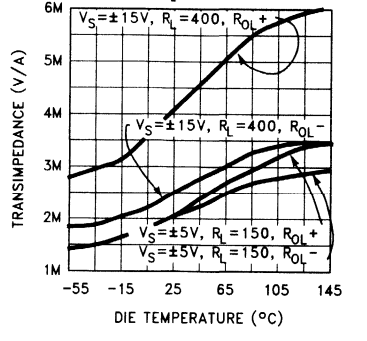
Voltage and Current Noise vs Frequency



Closed-Loop Output Impedance vs Frequency



Transimpedance (R_{OL}) vs Die Temperature

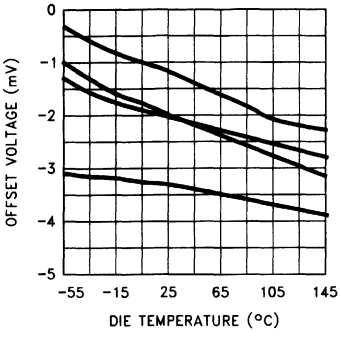


2260-5

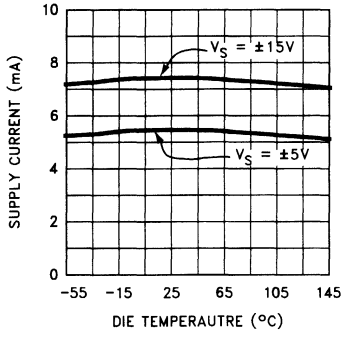
EL2260C/EL2460C
Dual/Quad 130 MHz Current Feedback Amplifiers

Typical Performance Curves — Contd.

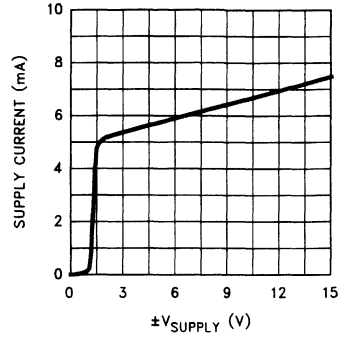
Offset Voltage vs Die Temperature (4 Samples)



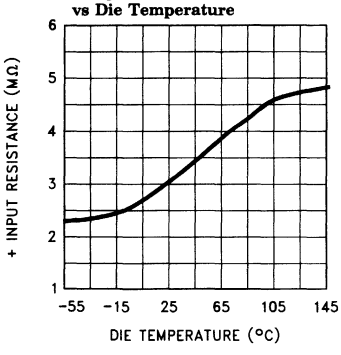
Supply Current vs Die Temperature (Per Amplifier)



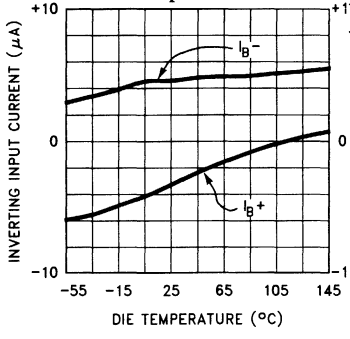
Supply Current vs Supply Voltage (Per Amplifier)



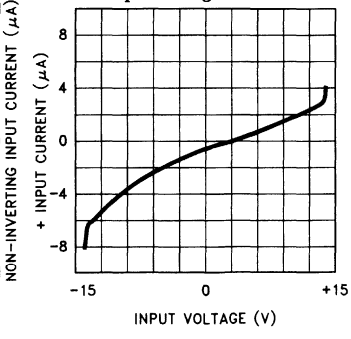
+Input Resistance vs Die Temperature



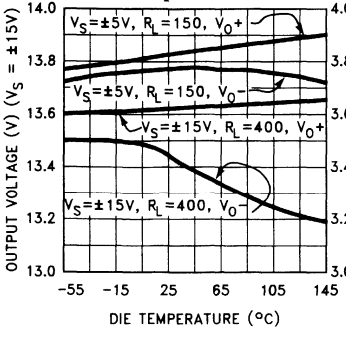
Input Current vs Die Temperature



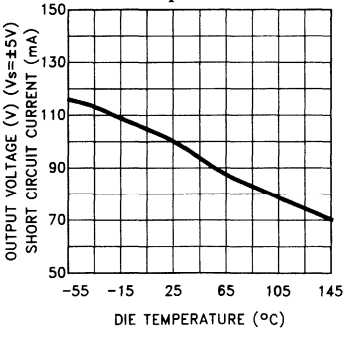
+Input Bias Current vs Input Voltage



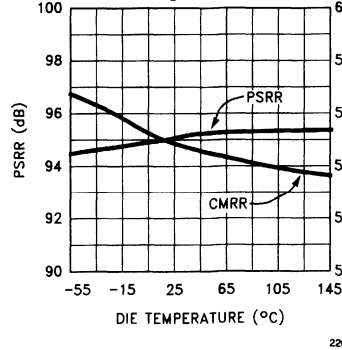
Output Voltage Swing vs Die Temperature



Short Circuit Current vs Die Temperature



PSRR & CMRR vs Die Temperature



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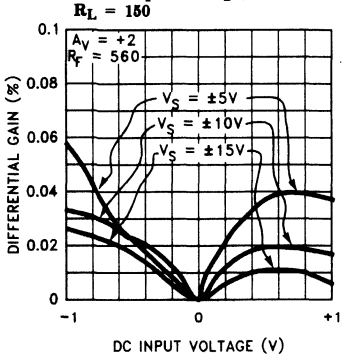
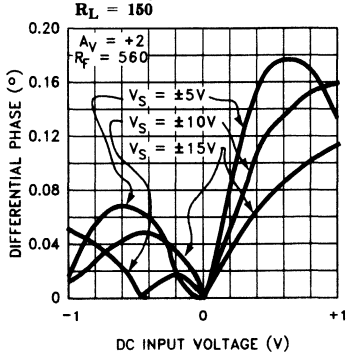
Typical Performance Curves — Contd.

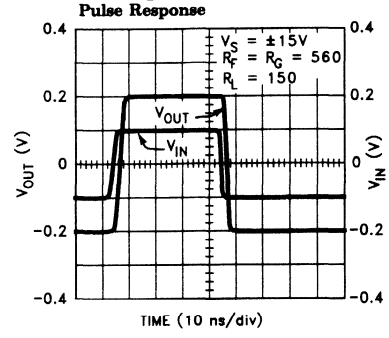
Differential Gain vs DC Input Voltage, R_L = 150



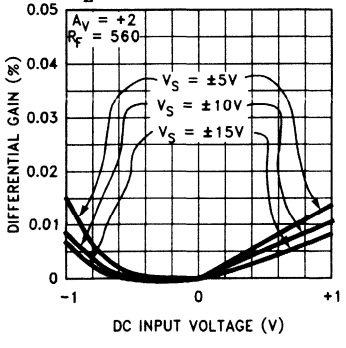
Differential Phase vs DC Input Voltage, R_L = 150



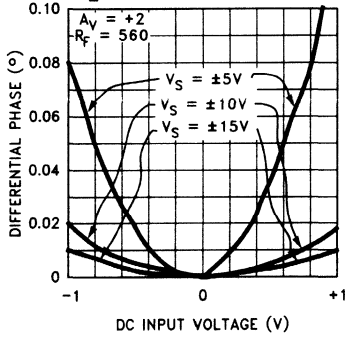
Small Signal Pulse Response



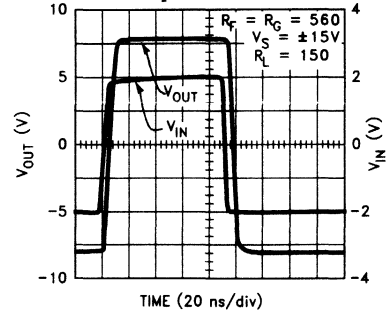
Differential Gain vs DC Input Voltage, R_L = 500



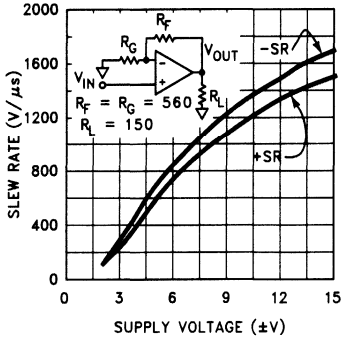
Differential Phase vs DC Input Voltage, R_L = 500



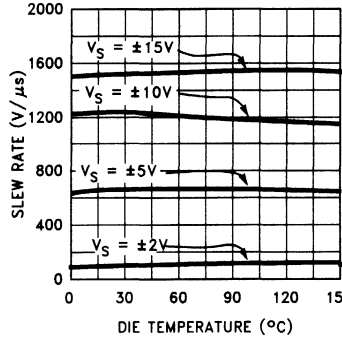
Large Signal Pulse Response



Slew Rate vs Supply Voltage



Slew Rate vs Temperature

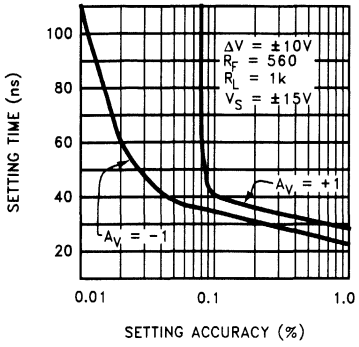


2260-7

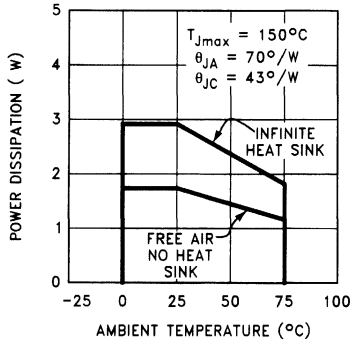
EL2260C/EL2460C
Dual/Quad 130 MHz Current Feedback Amplifiers

Typical Performance Curves — Contd.

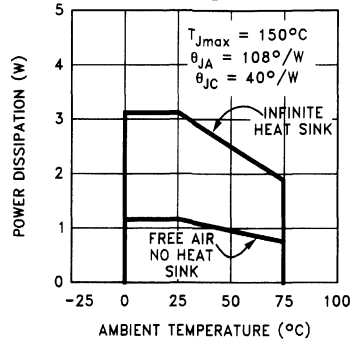
Settling Time vs Settling Accuracy



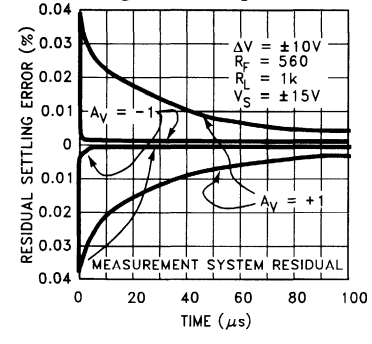
14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



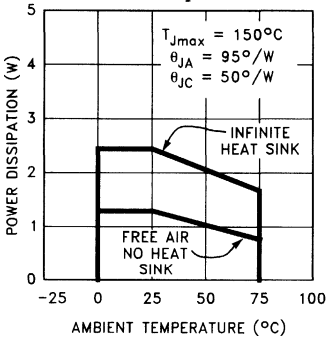
14-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature



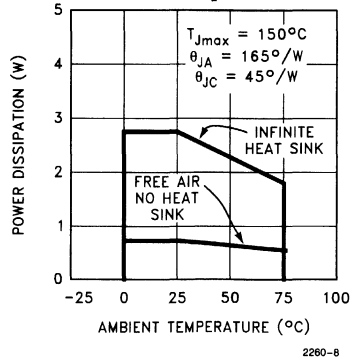
Long Term Settling Error



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



8-Lead Plastic SO Maximum Power Dissipation vs Ambient Temperature



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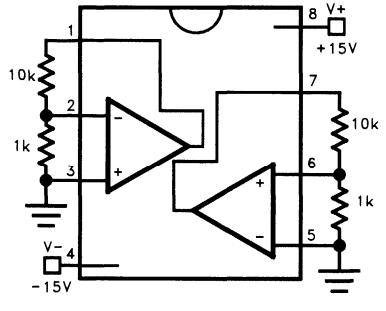
Burn-In Circuits

EL2260C



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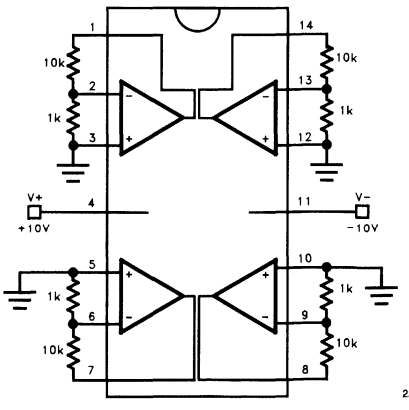
EL2460C



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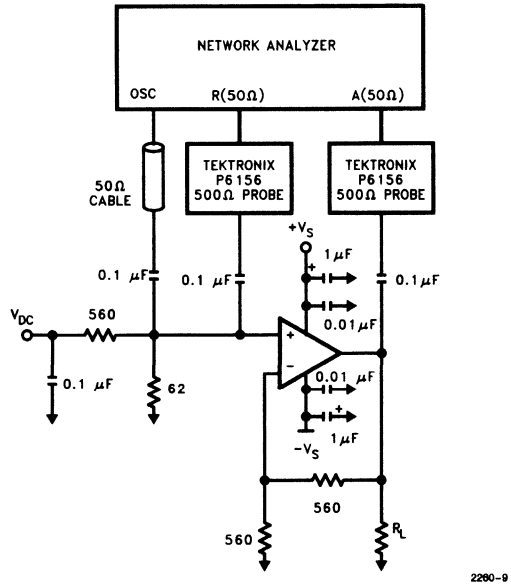
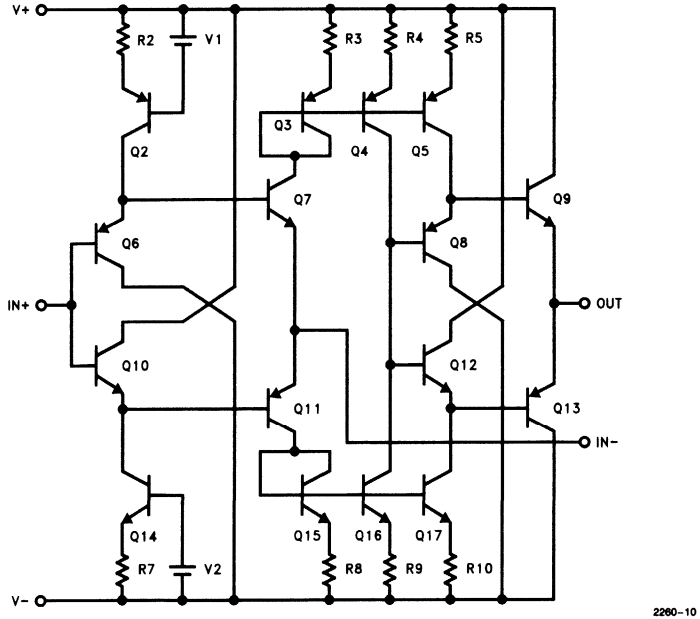
Differential Gain and Phase Test Circuit



Simplified Schematic (One Amplifier)



EL2260C/EL2460C
Dual/Quad 130 MHz Current Feedback Amplifiers

Applications Information

Product Description

The EL2260C/EL2460C are dual and quad current mode feedback amplifiers that offer wide bandwidths and good video specifications at moderately low supply currents. They are built using Elantec's proprietary complimentary bipolar process and are offered in industry standard pin-outs. Due to the current feedback architecture, the EL2260C/EL2460C closed-loop 3 dB bandwidth is dependent on the value of the feedback resistor. First the desired bandwidth is selected by choosing the feedback resistor, R_F, and then the gain is set by picking the gain resistor, R_G. The curves at the beginning of the Typical Performance Curves section show the effect of varying both R_F and R_G. The 3 dB bandwidth is somewhat dependent on the power supply voltage. As the supply voltage is decreased, internal junction capacitances increase, causing a reduction in closed loop bandwidth. To compensate for this, smaller values of feedback resistor can be used at lower supply voltages.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible, below ¼". The power supply pins must be well bypassed to reduce the risk of oscillation. A 1.0 μF tantalum capacitor in parallel with a 0.01 μF ceramic capacitor is adequate for each supply pin.

For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input (see Capacitance at the Inverting Input section). This implies keeping the ground plane away from this pin. Carbon resistors are acceptable, while use of wire-wound resistors should not be used because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance. Use of sockets, particularly for the SO packages, should be avoided. Sockets add parasitic inductance and capacitance which will result in peaking and overshoot.

Capacitance at the Inverting Input

Due to the topology of the current feedback amplifier, stray capacitance at the inverting input will affect the AC and transient performance of the EL2260C/EL2460C when operating in the non-inverting configuration. The characteristic curve of gain vs. frequency with variations of $C_{IN}-$ emphasizes this effect. The curve illustrates how the bandwidth can be extended to beyond 200 MHz with some additional peaking with an additional 2 pF of capacitance at the $V_{IN}-$ pin for the case of $A_V = +2$. Higher values of capacitance will be required to obtain similar effects at higher gains.

In the inverting gain mode, added capacitance at the inverting input has little effect since this point is at a virtual ground and stray capacitance is therefore not "seen" by the amplifier.

Feedback Resistor Values

The EL2260C and EL2460C have been designed and specified with $R_F = 560\Omega$ for $A_V = +2$. This value of feedback resistor yields extremely flat frequency response with little to no peaking out to 130 MHz. As is the case with all current feedback amplifiers, wider bandwidth, at the expense of slight peaking, can be obtained by reducing the value of the feedback resistor. Inversely, larger values of feedback resistor will cause rolloff to occur at a lower frequency. By reducing R_F to 430Ω, bandwidth can be extended to 170 MHz with under 1 dB of peaking. Further reduction of R_F to 360Ω increases the bandwidth to 195 MHz with about 2.5 dB of peaking. See the curves in the Typical Performance Curves section which show 3 dB bandwidth and peaking vs. frequency for various feedback resistors and various supply voltages.

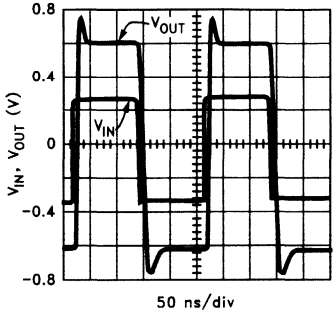
Bandwidth vs Temperature

Whereas many amplifier's supply current and consequently 3 dB bandwidth drop off at high temperature, the EL2260C/EL2460C were designed to have little supply current variations with temperature. An immediate benefit from this is that the 3 dB bandwidth does not drop off drastically with temperature. With $V_S = \pm 15V$ and $A_V = +2$, the bandwidth only varies from 150 MHz to 110 MHz over the entire die junction temperature range of $0°C < T < 150°C$.

Applications Information — Contd.

Supply Voltage Range

The EL2260C/EL2460C has been designed to operate with supply voltages from ±2V to ±15V. Optimum bandwidth, slew rate, and video characteristics are obtained at higher supply voltages. However, at ±2V supplies, the 3 dB bandwidth at $A_V = +2$ is a respectable 70 MHz. The following figure is an oscilloscope plot of the EL2260C at ±2V supplies, $A_V = +2$, $R_F = R_G = 560\Omega$, driving a load of 150Ω, showing a clean ±600 mV signal at the output.



If a single supply is desired, values from +4V to +30V can be used as long as the input common mode range is not exceeded. When using a single supply, be sure to either 1) DC bias the inputs at an appropriate common mode voltage and AC couple the signal, or 2) ensure the driving signal is within the common mode range of the EL2260C/EL2460C.

Settling Characteristics

The EL2260C/EL2460C offer superb settling characteristics to 0.1%, typically in the 35 ns to 40 ns range. There are no aberrations created from the input stage which often cause longer settling times in other current feedback amplifiers. The EL2260/EL2460 are not slew rate limited, therefore any size step up to ±10V gives approximately the same settling time.

As can be seen from the Long Term Settling Error curve, for $A_V = +1$, there is approximately a 0.035% residual which tails away to 0.01% in about 40 μs. This is a thermal settling error caused by a power dissipation differential (before and after the voltage step). For $A_V = -1$, due to the inverting mode configuration, this tail does not appear since the input stage does not experience the large voltage change as in the non-inverting mode. With $A_V = -1$, 0.01% settling time is slightly greater than 100 ns.

Power Dissipation

The EL2260C/EL2460C amplifiers combine both high speed and large output current drive capability at a moderate supply current in very small packages. It is possible to exceed the maximum junction temperature allowed under certain supply voltage, temperature, and loading conditions. To ensure that the EL2260C/EL2460C remain within their absolute maximum ratings, the following discussion will help to avoid exceeding the maximum junction temperature.

The maximum power dissipation allowed in a package is determined by its thermal resistance and the amount of temperature rise according to

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage plus the power in the IC due to the load, or

$$P_{DMAX} = N * \left(2 * V_S * I_S + (V_S - V_{OUT}) * \frac{V_{OUT}}{R_L} \right)$$

where N is the number of amplifiers per package, and I_S is the current per amplifier. (To be more accurate, the quiescent supply current flowing in the output driver transistor should be subtracted from the first term because, under loading and due to the class AB nature of the output stage, the output driver current is now included in the second term.)

In general, an amplifier's AC performance degrades at higher operating temperature and lower supply current. Unlike some amplifiers, such as the LT1229 and LT1230, the EL2260C/EL2460C

EL2260C/EL2460C
Dual/Quad 130 MHz Current Feedback Amplifiers

Applications Information — Contd.

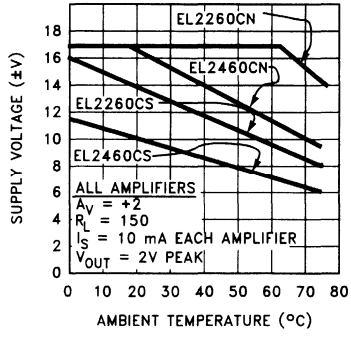
maintain almost constant supply current over temperature so that AC performance is not degraded as much over the entire operating temperature range. Of course, this increase in performance doesn't come for free. Since the current has increased, supply voltages must be limited so that maximum power ratings are not exceeded.

Each amplifier in the EL2260C/EL2460C consume typically 7.5 mA and maximum 10.0 mA. The worst case power in an IC occurs when the output voltage is at half supply, if it can go that far, or its maximum value if it cannot reach half supply. If we assume that the EL2260C/EL2460C is used for double terminated video cable driving applications (R_L = 150Ω), and the gain = +2, then the maximum output voltage is 2V, and the average output voltage is 1.4V. If we set the two P_{Dmax} equations equal to each other, and solve for V_S, we can get a family of curves for various packages and conditions according to:

$$V_S = \frac{\frac{R_L * (T_{JMAX} - T_{AMAX})}{N * \theta_{JA}} + (V_{OUT})^2}{(2 * I_S * R_L) + V_{OUT}}$$

The following curve shows supply voltage ($\pm V_S$) vs. temperature for the various packages assuming A_V = + 2, R_L = 150, and V_{OUT} peak = 2V. The curves include worst case conditions (I_S = 10 mA and all amplifiers operating at V_{OUT} peak = 2V).

Supply Voltage vs Ambient Temperature for All Packages of EL2260C/EL2460C



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The curves do not include heat removal or forcing air, or the simple fact that the package will probably be attached to a circuit board, which can also provide some form of heat removal. Larger temperature and voltage ranges are possible with heat removal and forcing air past the part.

Current Limit

The EL2260C/EL2460C have internal current limits that protect the circuit in the event of the output being shorted to ground. This limit is set at 100 mA nominally and reduces with junction temperature. At a junction temperature of 150°C, the current limits at about 65 mA. If any one output is shorted to ground, the power dissipation could be well over 1W, and much greater if all outputs are shorted. Heat removal is required in order for the EL2260C/EL2460C to survive an indefinite short.

Channel to Channel Isolation

Due to careful biasing connections within the internal circuitry of the EL2260C/EL2460C, exceptionally good channel to channel isolation is obtained. Isolation is over 70 dB at video frequencies of 4 MHz, and over 65 dB up to 10 MHz. The EL2460C isolation is improved an additional 10 dB, up to about 5 MHz, for amplifiers A to B and amplifiers C to D. Isolation is improved another 8 dB for amplifiers A to C and amplifiers B to D. See the curve in the Typical Performance Curves section for more detail.

Driving Cables and Capacitive Loads

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2260C and EL2460C from the capacitive cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking. The gain resistor, R_G, can be chosen to make up for the gain loss created by this additional series resistor at the output.

EL2260C/EL2460C Macromodel

```
* Revision A, March 1993
* AC Characteristics used C_IN− (pin 2) = 1 pF; R_F = 560Ω
* Connections:          +input
*                       |     −input
*                       |     |     +Vsupply
*                       |     |     |     −Vsupply
*                       |     |     |     |     output
*                       |     |     |     |     |
.subckt EL2260C/EL  3     2     7     4     6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 130
l1 11 12 25nH
iinp 3 0 0.5µA
iinm 2 0 5µA
r12 3 0 2Meg
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.00166666666
l3 30 17 0.43µH
c5 17 0 0.27pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
ro1 18 0 2Meg
cdp 18 0 2.285pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2mA
ios2 20 4 2mA
*
```

EL2260C/EL2460C Macromodel — Contd.

```
* Supply Current
*
ips 7 4 2mA
*
* Error Terms
*
ivos 0 23 2mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 562
r10 25 23 1K
r11 26 23 1K
*
* Models
*
.model qn npn (is=5e-15 bf=100 tf=0.1ns)
.model qp pnp (is=5e-15 bf=100 tf=0.1ns)
.model dclamp d (is=1e-30 ibv=0.266 bv=2.24 n=4)
.ends
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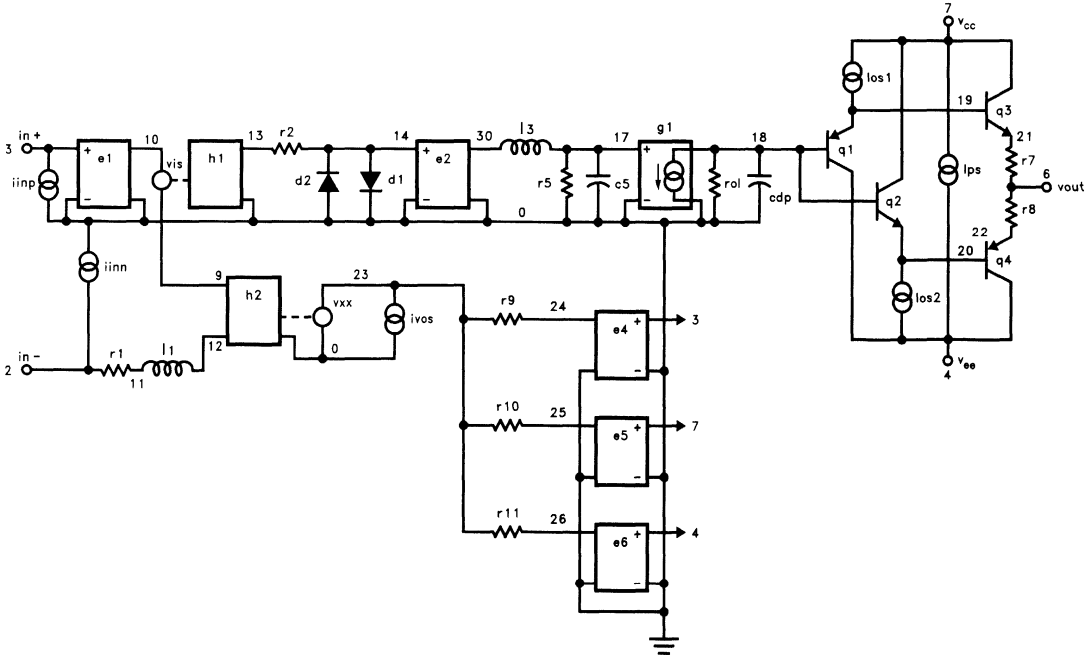


2260-15

EL2423C

Quad De-Compensated High Speed Operational Amplifier

Features

- Stable for gains > 10
- Wide bandwidth—500 MHz
- High slew rate—350 V/μs
- Wide supply range—
  ±5V to ±15V
- Output short circuit protected
- Low supply current—4 mA per amplifier

Applications

- High frequency active filters
- Video amplifiers
- Pulse amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline*
EL2423CN	0°C to +75°C	P-DIP	MDP0006
EL2423CM	0°C to +75°C	SOL	MDP0027

General Description

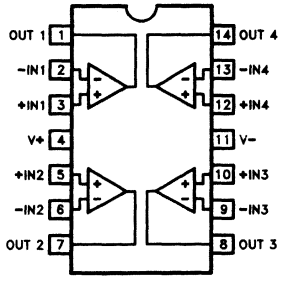
The EL2423 monolithic quad operational amplifier is an example of Elantec's commitment to high speed low power consumption products. This amplifier is stable for gains of 10 or greater, exhibits Slew Rates of 350V per microsecond, and a Gain Bandwidth of 500 MHz while drawing supply currents of 4 mA per amplifier. The output provides short circuit protection but is capable of delivering currents in excess of 50 mA. The device is manufactured using Elantec's advanced Complementary Bipolar process.

The EL2423 is available in 14-lead Plastic DIP, and 20-pad SOL.

Elantec's products and facilities comply with MIL-I-45082A, and other applicable quality specifications. For information on Elantec's processing, see QRA-1, "*Processing Monolithic Integrated Circuits*".

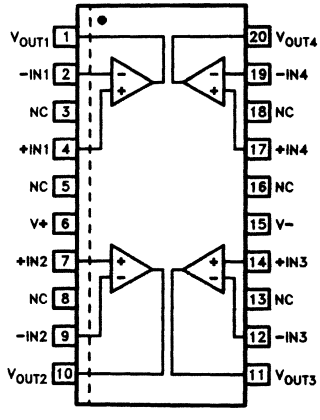
Connection Diagrams

EL2423CN



2423-1

EL2423CM



2423-2

EL2423C
Quad De-Compensated High Speed Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Storage Temperature Range	−65°C to 150°C
Differential Input Voltage	6V	Maximum Junction Temperature	
Peak Output Current	Short Circuit Protected	CerDIP, LCC	175°C
Output Short Circuit Duration (Note 1)	Continuous	Plastic DIP, SOL	150°C
Internal Power Dissipation	See Curves	Lead Temperature	
Operating Temperature Range	0°C to +75°C	DIP Package	300°C
		SOL Package	
		Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2423C				Units
			Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	25°C		1.0	6	I	mV
		Full			10	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		10		V	µV/°C
I_B	Bias Current	25°C		1.0	4	I	µA
		Full			6	III	µA
I_{OS}	Offset Current	25°C		0.5	2	I	µA
		Full			3	III	µA
R_{IN}	Input Resistance	25°C		20		V	kΩ
C_{IN}	Input Capacitance	25°C		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±11		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		7		V	nV/$\sqrt{Hz}$
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	25°C	20k	40k		I	V/V
		Full	10k			IIII	V/V
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	80		II	dB

DC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\ k\Omega$, unless otherwise specified — Contd.

Parameter	Description	Temp	EL2423C				Units
			Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	Full	±11	±12		II	V
I_{SC}	Short Circuit Current	25°C	±10	+50	±85	I	mA
R_O	Output Resistance	25°C		40		V	Ω
I_S	Supply Current	Full		16	18	II	mA
PSRR	Power Supply Rejection Ration (Note 5)	Full	70	80		II	dB

AC Electrical Characteristics $V_S = \pm 15V$; $R_L = 2\ k\Omega$, unless otherwise specified

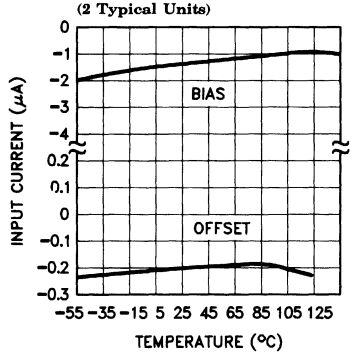
Parameter	Description	Temp	EL2423C				Units
			Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	25°C		200		V	MHz
FPBW	Full Power Bandwidth (Note 7)	25°C	3.48	5.5		I	MHz
t_r	Rise Time (Note 6)	25°C		7		V	ns
OS	Overshoot (Note 6)	25°C		20		V	%
SR	Slew Rate (Note 6)	25°C	250	350		I	V/μs
t_s	Settling Time (Note 9) 10V Step to 0.05%	25°C		330		V	ns
CHSp	Channel Separation f = 1 MHz	25°C		65		V	dB

Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: $V_O = \pm 10V$.
Note 3: $R_L = 2k\Omega$.
Note 4: Two tests are performed. $V_{CM} = 0V$ to $+10V$ and $V_{CM} = 0V$ to $-10V$.
Note 5: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 6: $V_O = 100$ mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/2π V_{peak}.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurements are made with techniques in the following reference: "*Take The Guesswork Out of Settling-Time Measurements*," EDN September 19, 1985.

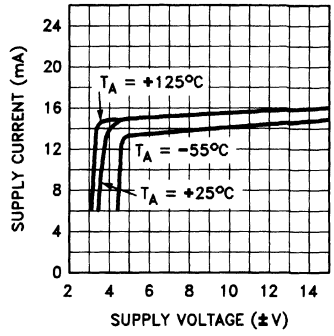
EL2423C
Quad De-Compensated High Speed Operational Amplifier

Typical Performance Curves

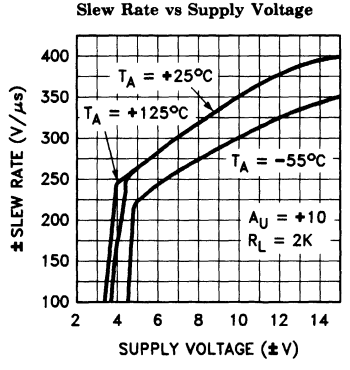
Input Current vs Temperature (2 Typical Units)



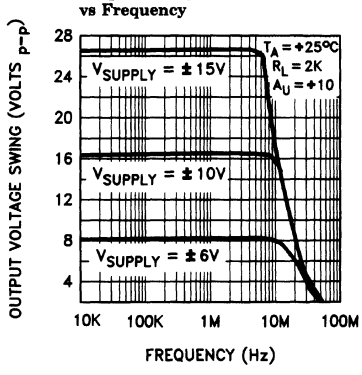
Supply Current vs Supply Voltage



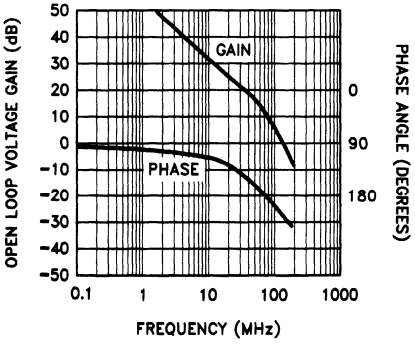
Slew Rate vs Supply Voltage



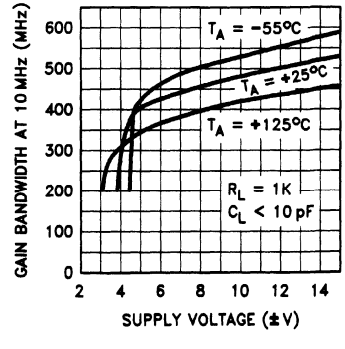
Output Voltage Swing vs Frequency



Open Loop Voltage Gain vs Frequency



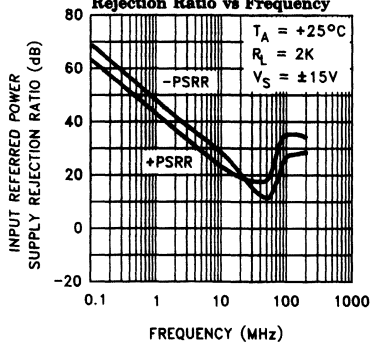
Gain Bandwidth at 10 MHz vs Supply Voltage



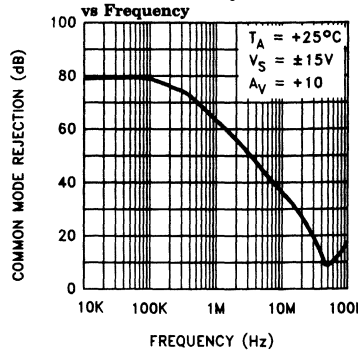
2423-4

Typical Performance Curves — Contd.

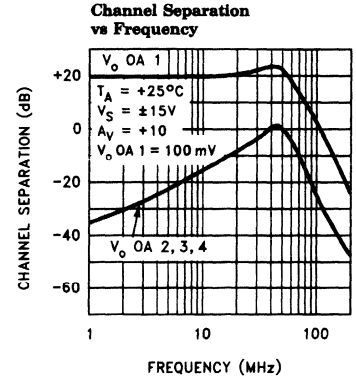
Input Referred Power Supply Rejection Ratio vs Frequency



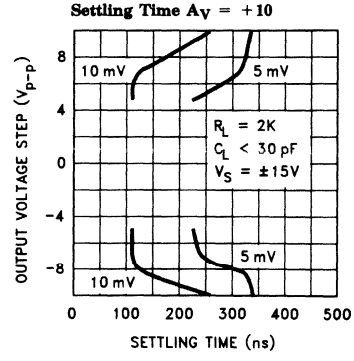
Common Mode Rejection vs Frequency



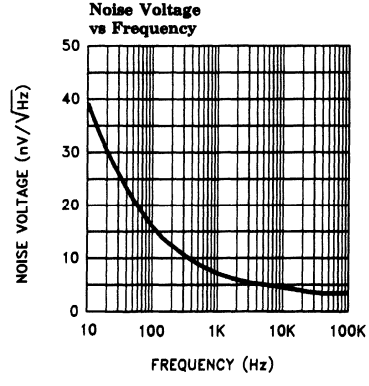
Channel Separation vs Frequency



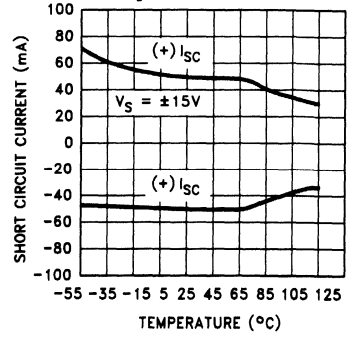
Settling Time A_V = +10



Noise Voltage vs Frequency



Short Circuit Current vs Temperature

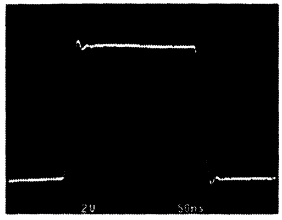


2423-5

EL2423C
Quad De-Compensated High Speed Operational Amplifier

Typical Performance Curves — Contd.

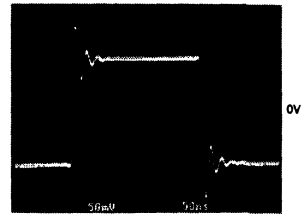
Large Signal Response



A_V = +10
V_{IN} = ±0.5V
V_O = ±5V
R_L = 2k

2423-6

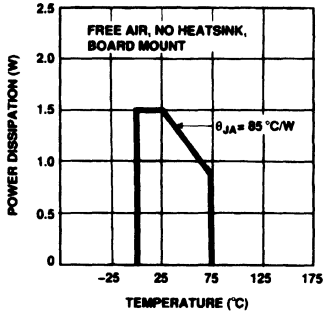
Small Signal Response



A_V = +10
V_{IN} = ±10 mV
V_O = ±100 mV
R_L = 2k

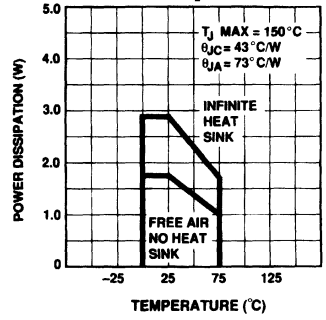
2423-7

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



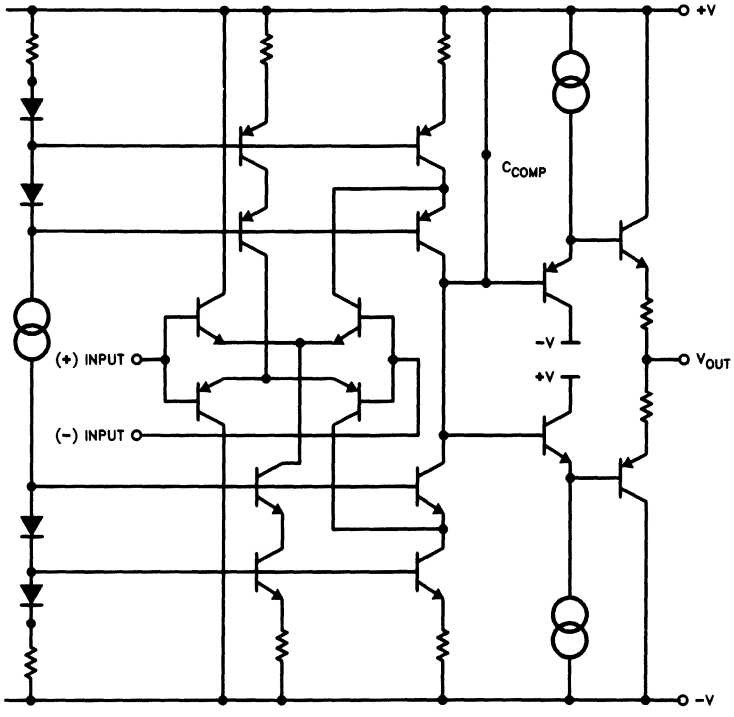
2423-8

14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

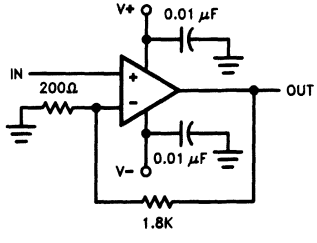


2423-9

Simplified Schematic (One Amplifier)

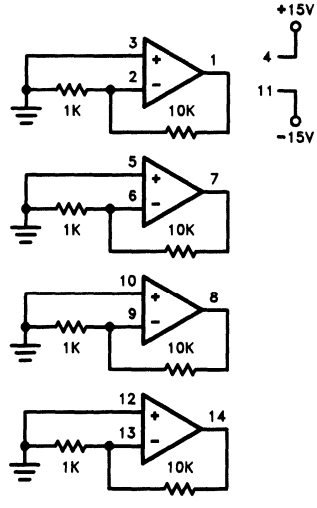


Test Circuit



Pin numbers indicated are for the 14-lead DIP. Circuit is identical for all package types.

Burn In Circuit

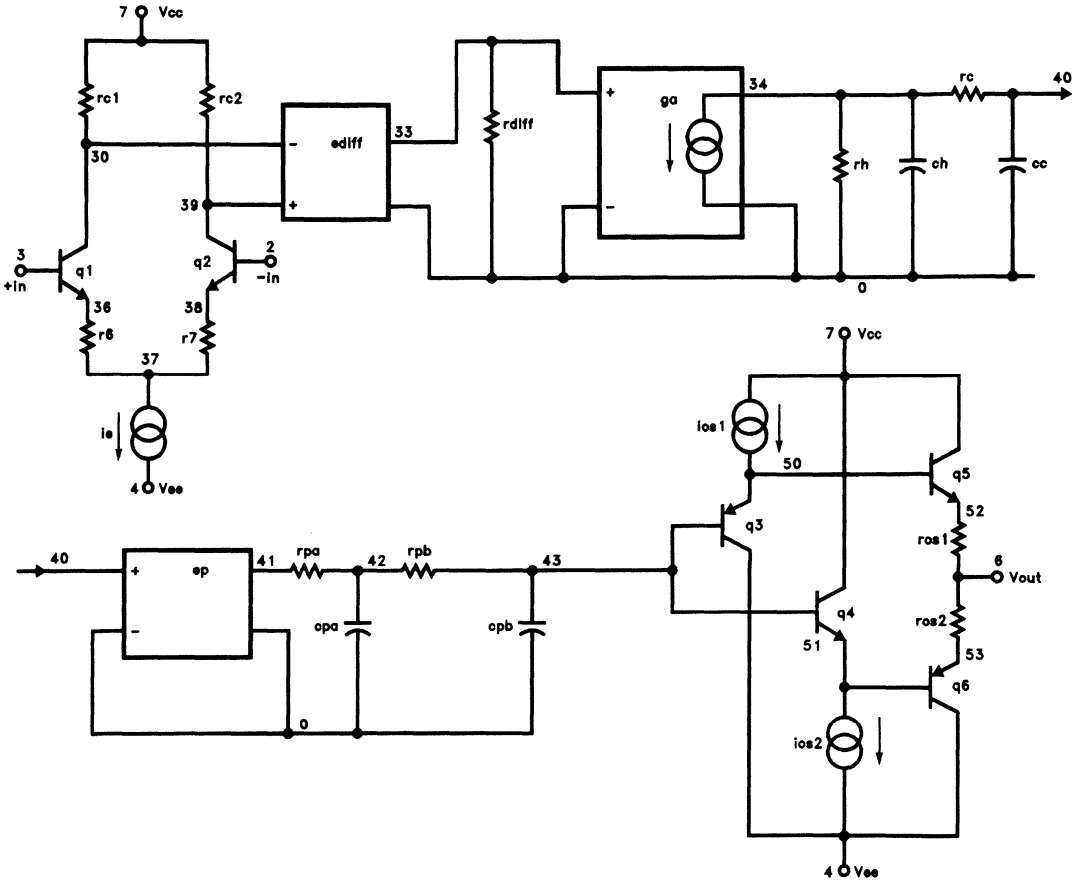


EL2423C
Quad De-Compensated High Speed Operational Amplifier

EL2423 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2423       3     2     7     4     6
* Input stage
ie 37 4 2mA
r6 36 37 60
r7 38 37 60
rc1 7 30 75
rc2 7 39 75
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 7.25
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 2.6m
rh 34 0 3Meg
ch 34 0 1.5pF
rc 34 40 600
cc 40 0 7pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 25pF
rpb 42 43 50
cpb 43 0 15pF
* Output Stage
ios1 7 50 1.25mA
ios2 51 4 1.25mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
* models
.model qn npn(is=800.0E-18 bf=250 tf=0.2nS)
.model qna npn(is=864E-18 bf=300 tf=0.2nS)
.model qp pnp(is=800E-18 bf=60 tf=0.2nS)
.ends
```

EL2423 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2424C

Quad 60 MHz High Speed Operational Amplifier

Features

- Unity-gain stable
- Wide bandwidth—60 MHz
- High slew rate—200 V/μs
- Wide supply range—
  $\pm$5V to $\pm$15V
- Output short circuit protected
- Low supply current—4 mA per amplifier

Applications

- High frequency active filters
- Video amplifiers
- Pulse amplifiers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2424CN	0°C to +75°C	P-DIP	MDP0031
EL2424CM	0°C to +75°C	SOL	MDP0027

General Description

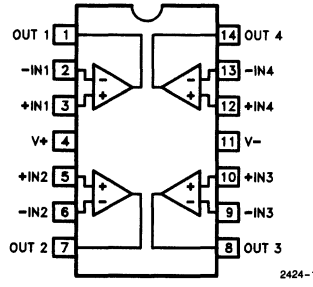
The EL2424 monolithic quad operational amplifier is an example of Elantec's commitment to high speed low power consumption products. This amplifier is unity-gain stable, exhibits Slew Rates of 200V per microsecond, and a Gain Bandwidth of 60 MHz while drawing supply currents of 4 mA per amplifier. The output provides short circuit protection but is capable of delivering currents in excess of 50 mA. The device is manufactured using Elantec's advanced Complementary Bipolar process.

The EL2424 is available in 14-lead Plastic DIP, and 20-pad SOL.

Elantec's products and facilities comply with MIL-I-45082A, and other applicable quality assurance specifications. For information on Elantec's Commercial processing, see QRA-1, "*Summary of Elantec's Reliability and Quality Assurance Policy*".

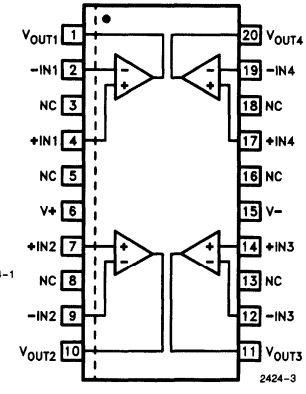
Connection Diagrams

EL2424CN



2424-1

EL2424CM



2424-3

EL2424C
Quad 60 MHz High Speed Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	35V	Storage Temperature Range	−65°C to 150°C
Differential Input Voltage	6V	Maximum Junction Temperature	
Peak Output Current	Short Circuit Protected	Plastic DIP, SOL	150°C
Output Short Circuit Duration (Note 1)	Continuous	Lead Temperature	
Internal Power Dissipation	See Curves	DIP Package	300°C
Operating Temperature Range	0°C to +75°C	SOL Package	
		Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level
I — 100% production tested and QA sample tested per QA test plan QCX0002.
II — 100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III — QA sample tested per QA test plan QCX0002.
IV — Parameter is guaranteed (but not tested) by Design and Characterization Data.
V — Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2424C Min	EL2424C Typ	EL2424C Max	EL2424C Test Level	Units
V_{OS}	Offset Voltage	25°C		6	15	I	mV
		Full			20	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		50		V	µV/°C
I_B	Bias Current	25°C		1.0	4	I	µA
		Full			6	III	µA
I_{OS}	Offset Current	25°C		0.5	2	I	µA
		Full			3	III	µA
R_{IN}	Input Resistance	25°C		20		V	kΩ
C_{IN}	Input Capacitance	25°C		1		V	pF
V_{CM}	Common Mode Input Range	Full	±10	±11		II	V
e_{IN}	Input Noise Voltage (f = 1 kHz, R_G = 0Ω)	25°C		7		V	nV/√Hz
A_{VOL}	Large Signal Voltage Gain (Notes 2, 3)	25°C	5k	13k		I	V/V
		Full	4k			III	V/V
CMRR	Common-Mode Rejection Ratio (Note 4)	Full	70	87		II	dB

EL2424C
Quad 60 MHz High Speed Operational Amplifier

DC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified — Contd.

Parameter	Description	Temp	EL2424C				Units
			Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	Full	±11	±13		II	V
I_{SC}	Short Circuit Current	25°C	±10	±50	±85	I	mA
R_O	Output Resistance	25°C		40		V	Ω
I_S	Supply Current	Full		14	18	II	mA
PSRR	Power Supply Rejection Ratio (Note 5)	Full	60	80		II	dB

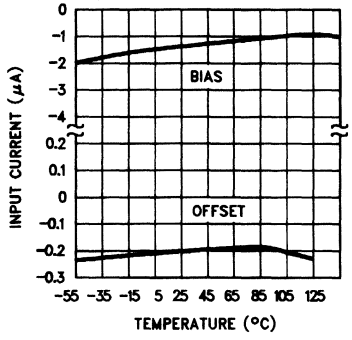
AC Electrical Characteristics V_S = ±15V; R_L = 2 kΩ, unless otherwise specified

Parameter	Description	Temp	EL2424C				Units
			Min	Typ	Max	Test Level	
f_u	Open Loop Unity Bandwidth (Note 6)	25°C		60		V	MHz
FPBW	Full Power Bandwidth (Note 7)	25°C	2.4	3.2		I	MHz
t_r	Rise Time (Note 6)	25°C		7		V	ns
OS	Overshoot (Note 6)	25°C		20		V	%
SR	Slew Rate (Note 10)	25°C	150	200		I	V/μs
t_s	Settling Time (Note 9) 10V Step to 0.05%	25°C		330		V	ns
CHSp	Channel Separation f = 1 MHz	25°C		65		V	dB

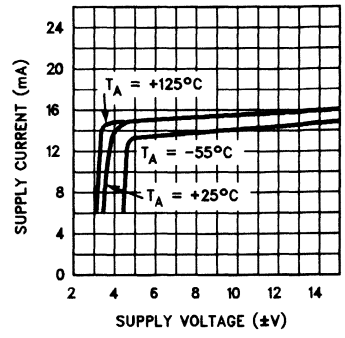
Note 1: A heat sink is required to keep the junction temperature below absolute maximum when the output is shorted.
Note 2: V_O = ±10V.
Note 3: R_L = 2kΩ.
Note 4: Two tests are performed. V_{CM} = 0V to +10V and V_{CM} = 0V to −10V.
Note 5: Two tests are performed. V+ = 15V, and V− is changed from −5V to −15V. V− = −15V, and V+ is changed from +5V to +15V.
Note 6: V_O = 100 mV.
Note 7: Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = Slew Rate/2π V_{peak}.
Note 8: Refer to Test Circuit section of data sheet.
Note 9: Settling time measurements are made with techniques in the following reference: "*Take The Guesswork Out of Settling-Time Measurements,*" EDN September 19, 1985.
Note 10: V_O = ±10V.

Typical Performance Curves

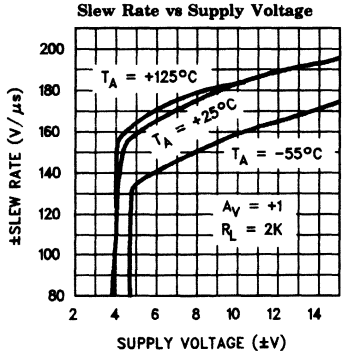
Input Current vs Temperature



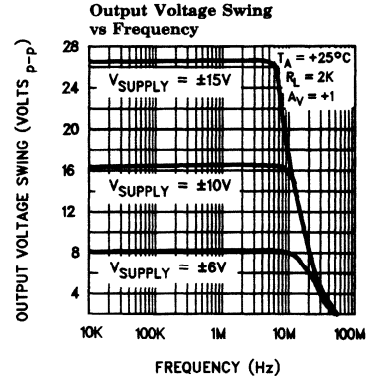
Supply Current vs Supply Voltage



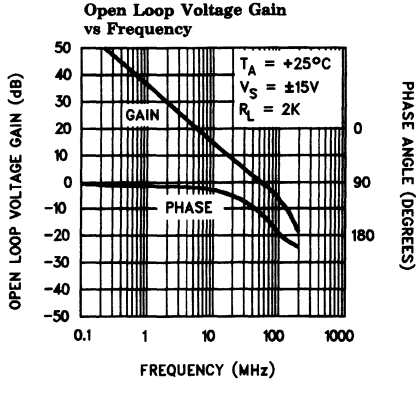
Slew Rate vs Supply Voltage



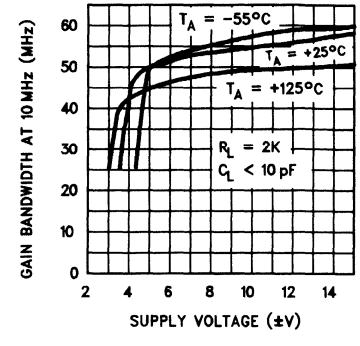
Output Voltage Swing vs Frequency



Open Loop Voltage Gain vs Frequency



Gain Bandwidth at 10 MHz vs Supply Voltage

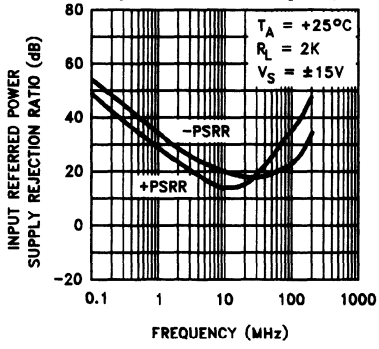


2424-4

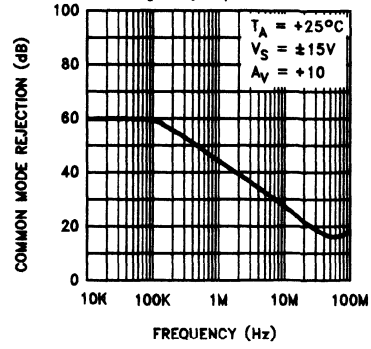
EL2424C
Quad 60 MHz High Speed Operational Amplifier

Typical Performance Curves — Contd.

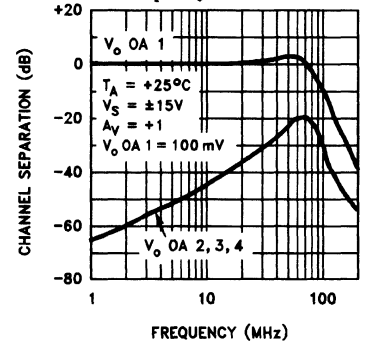
Input Referred Power Supply Rejection Ratio vs Frequency



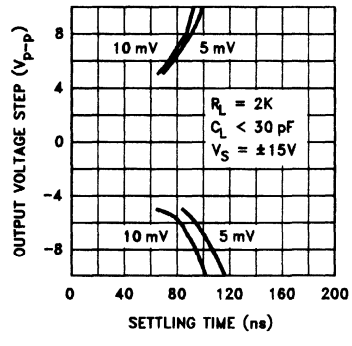
Common Mode Rejection vs Frequency A_V = +10



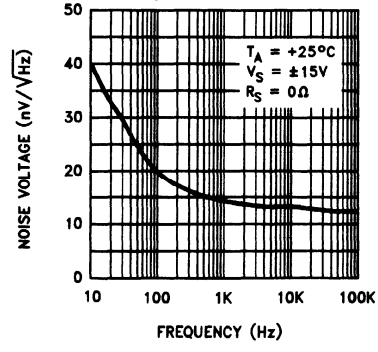
Channel Separation vs Frequency



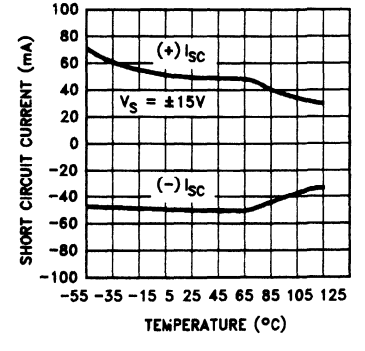
Settling Time A_V = +1



Noise Voltage vs Frequency



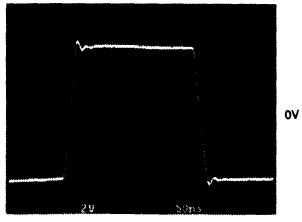
Short Circuit Current vs Temperature



2424-5

Typical Performance Curves — Contd.

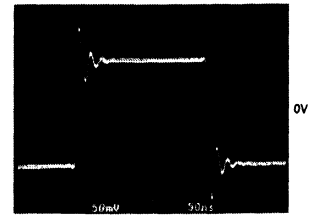
Large Signal Response



$A_V = +1$
$V_{IN} = \pm 5V$
$V_O = \pm 5V$
$R_L = 2k$

2424-6

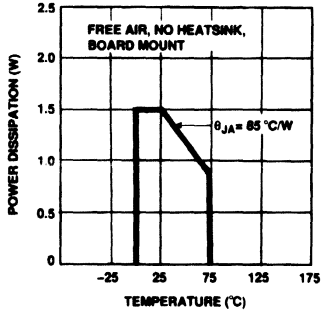
Small Signal Response



$A_V = +1$
$V_{IN} = \pm 100$ mV
$V_O = \pm 100$ mV
$R_L = 2k$

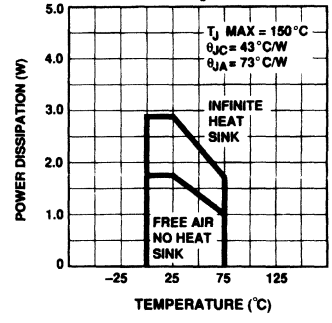
2424-7

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



2424-8

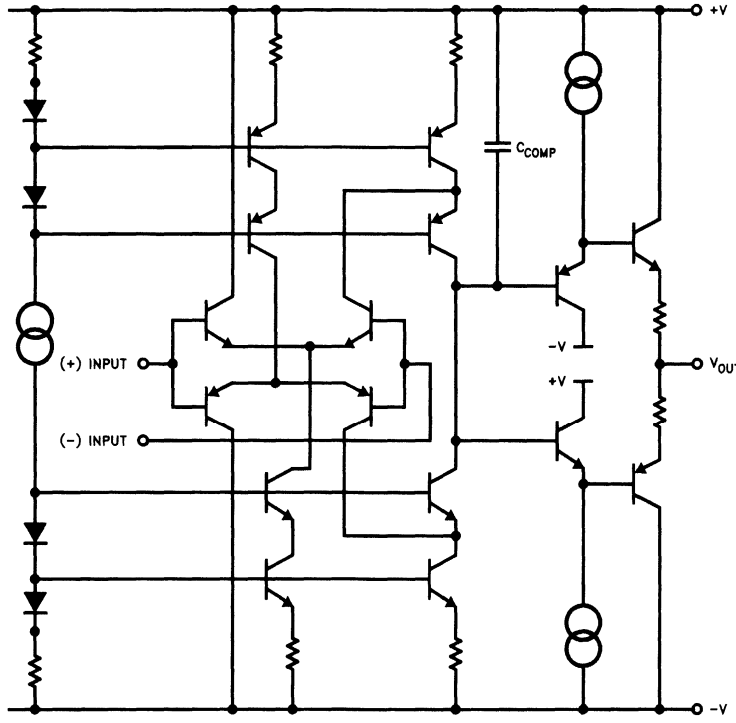
14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



2424-9

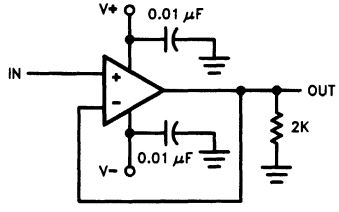
EL2424C
Quad 60 MHz High Speed Operational Amplifier

Simplified Schematic (One Amplifier)



2424-11

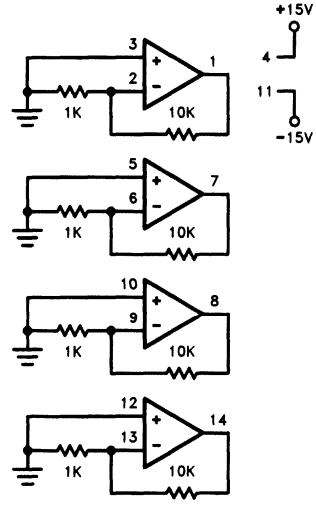
Test Circuit



2424-12

Pin numbers indicated are for the 14-lead DIP. Circuit is identical for all package types.

Burn In Circuit



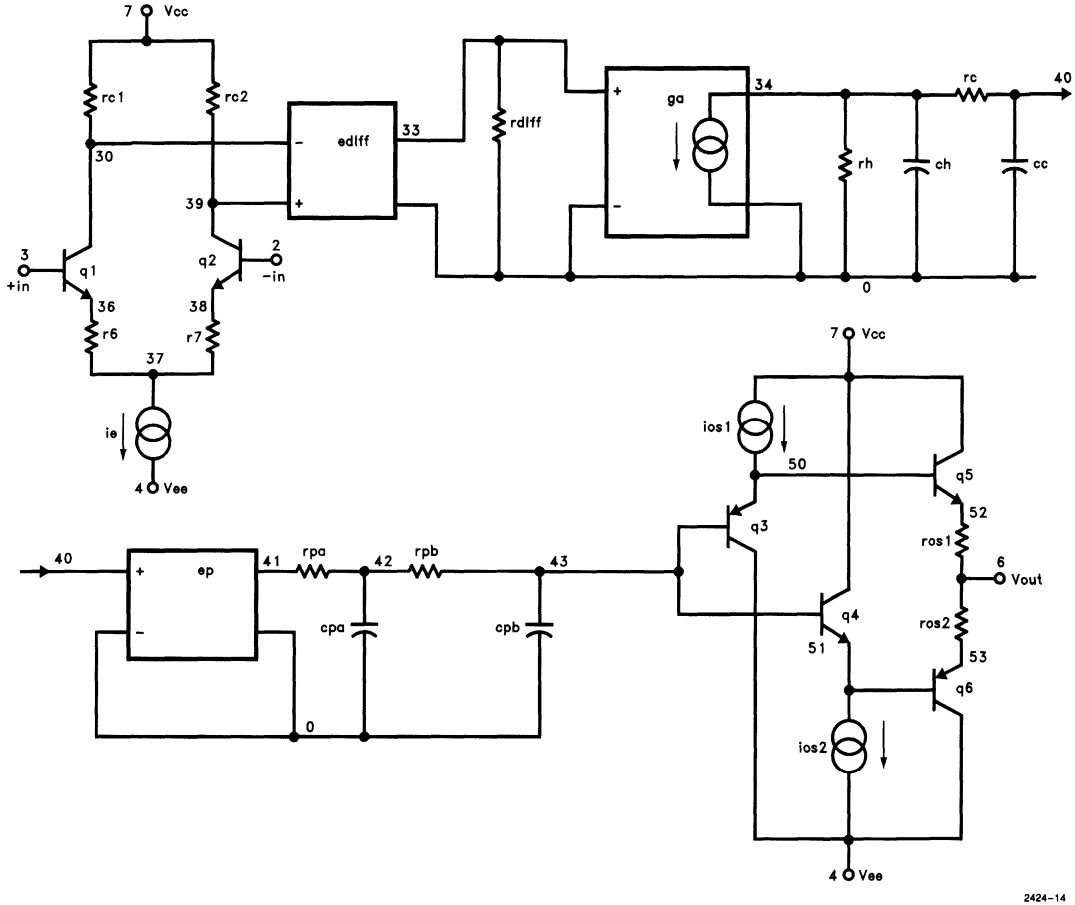
2424-13

EL2424C Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2424       3     2     7     4     6
* Input stage
ie 37 4 4.5mA
r6 36 37 75
r7 38 37 75
rc1 7 30 75
rc2 7 39 75
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 2.6
rdiff 33 0 1Meg
* Compensation Section
ga 0 34 33 0 3m
rh 34 0 1Meg
ch 34 0 15pF
rc 34 40 300
cc 40 0 1pF
* Poles
ep 41 0 40 0 1
rpa 41 42 75
cpa 42 0 3pF
rpb 42 43 50
cpb 43 0 3pF
* Output Stage
ios1 7 50 0.5mA
ios2 51 4 0.5mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 25
ros2 6 53 25
* models
.model qn npn(is=800.0E-18 bf=350 tf=0.2nS)
.model qna npn(is=864E-18 bf=400 tf=0.2nS)
.model qp pnp(is=800E-18 bf=60 tf=0.2nS)
.ends
```

EL2424C
Quad 60 MHz High Speed Operational Amplifier

EL2424C Macromodel — Contd.



EL8001E

High Temperature Instrumentation Amplifier

Features

- Wide temperature range −40°C to +150°C
- Single-supply operation +4.0V to +36V
- Low offset voltage 400 μV
- Low offset voltage drift 1 μV/°C (G = 1k)
- Capacitive load stability to 0.3 μF
- Gain range 10 to 10,000
- Excellent gain nonlinearity 0.1% at G = 1000

Applications

- DownHole measurements
- High-temperature sensors
- Strain-gauge amplifiers

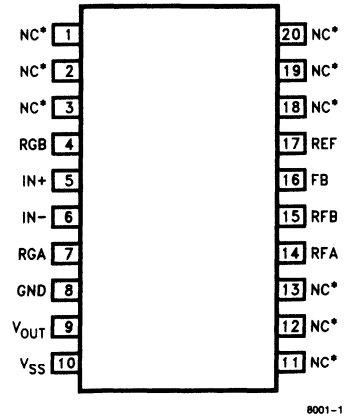
Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL8001EB	−40°C to +150°C	20-Pin Sidebraze	MDP0033

General Description

The EL8001 is a precision low-noise instrumentation amplifier which has been designed for use in high temperature applications. Specifications are guaranteed to 150°C, with functionality extending beyond 175°C. This part operates from a single supply voltage ranging from 4.0V to 36V. Gain is set over a range of 10 to 10,000 using external resistor ratios.

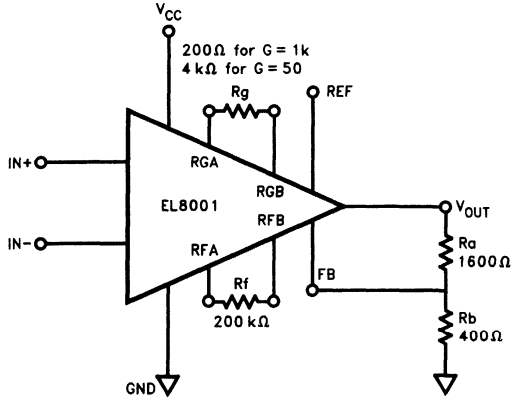
Connection Diagram



8001-1

*Do not connect. These pins must float.

Block Diagram



8001-2

$$\text{Gain} = \left(\frac{Rf}{Rg}\right)\left(\frac{Ra + Rb}{Rb}\right)$$

EL8001E
High Temperature Instrumentation Amplifier

Absolute Maximum Ratings

Supply (V+ to GND)	36V	Operating Temperature Range	−40°C to +175°C
Differential Input Voltage	7V	Storage Temperature Range	−40°C to +175°C
Common-Mode Input Voltage	−0.3 to 36V	Internal Power Dissipation Sidebraze	250 mW
Output Short-Circuit Duration "V_{OUT}" shorted to GND V_{CC} = 5V	Inf.		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

V_{CC} = 5V, Ra + Rb = 2k, Rf = 200k, IN+ = IN− = 2.5V, REF = 0.5., Gain = 1k unless otherwise specified

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
OFFSET VOLTAGE SPECIFICATIONS (IN+ to IN− when "FB" = "REF")								
V_{OS}	Input Offset Voltage	Note 1	All			400	II	µV
TCV_{OS}	Input Offset Voltage Drift	Note 1 25°C to 150°C G = 1k	All			1	II	µV/°C
		Note 1 25°C to 150°C G = 50	All			4	IV	µV/°C
PSRR	Power Supply Rejection Ratio	V_{CC} = 4.0V to 5.5V	25°C	100			I	dB
			−40°C to +150°C	90			III	dB
INPUT CURRENT SPECIFICATIONS (IN+ and IN−)								
Ib	Input Bias Current		All			500	II	nA
Iio	Input Offset Current		All			50	II	nA
TCIio	Input Offset Current Drift	25°C to 150°C	All			160	II	pA/°C
GENERAL INPUT SPECIFICATIONS (IN+ and IN−)								
IVR	Input Voltage Range			0.3		3.8	IV	V
CMRR	Common-Mode Rejection Ratio	Vcm = 1V, 3V G = 1k		90			II	dB
		Vcm = 1V, 3V G = 50		74			IV	dB
GAIN SPECIFICATIONS ("V_{OUT}" − ("REF" * (Ra + Rb)/Rb))/("IN+" − "IN−"). Ra + Rb = 2k, Gain = Rf/Rg								
G	Gain Range		All	10		10,000	IV	V/V
GNL	Gain Nonlinearity	OUT = 1V, 3V G = 1k	25°C			0.1	I	%
		OUT = 1V, 3V G = 1k	−40°C to +150°C			0.2	III	%
		OUT = 1V, 3V G = 50	All			0.1	II	%
GA	Gain Accuracy					8	II	%

Electrical Characteristics — Contd.

V_{CC} = 5V, Ra + Rb = 2k, Rf = 200k, IN+ = IN− = 2.5V, REF = 0.5., Gain = 1k unless otherwise specified

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
OUTPUT SPECIFICATIONS (at "V_{OUT}")								
V_{OUT}	Output Voltage Swing	Output Low	All			0.4	II	V
		Output High	All	3.8			II	V
CStab	Capacitive Load Stability	G = 2k, No Oscillations	All	0.3			IV	µF
NOISE SPECIFICATIONS (referred to IN+ and IN−)								
eN(pp)	Input Noise Voltage	f = 0.2Hz–20 Hz, Rs = 50	All		0.5	2	V	μV_{PP}
iN(pp)	Input Noise Current	f = 0.2Hz–20 Hz, Rs = BIG	All			500	V	pA_{PP}
DYNAMIC RESPONSE (at "V_{OUT}")								
SR	Slew Rate	0.4V to 3.8V 25%–75%	25°C	17			I	V/ms
			−40°C to +150°C	14			III	V/ms
*"REF" and "FB" INPUT SPECIFICATIONS								
I_{REF}	Input Bias Current		All			500	II	n/A
V_{REF}	Input Voltage Range		All	0		3	IV	V
*POWER SUPPLY SPECIFICATIONS								
V_{CC}	Supply Voltage Range		All	4		36	IV	V
I_{CC}	Supply Current	No Load	All			4	II	mA

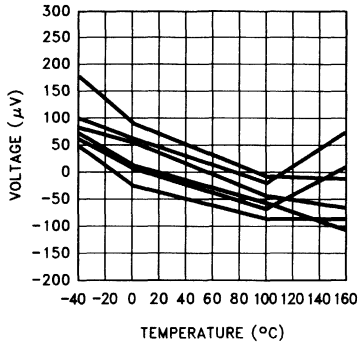
Note 1: V_{OS} and TCV_{OS} Specifications are with Ra = 1600, Rb = 400.

Note 2: Typically, Ra = 1600, Rb = 400, but Ra and Rb may vary according to test (Ra + Rb = 2k).

EL8001E
High Temperature Instrumentation Amplifier

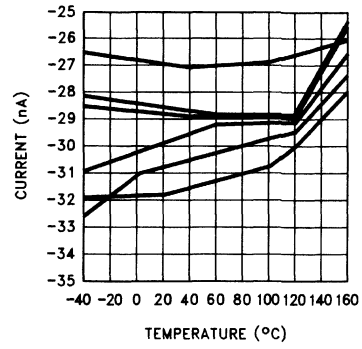
Typical Performance Curves

Input Voltage Offset



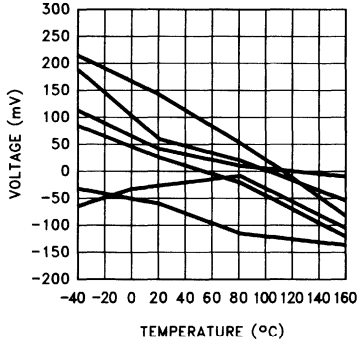
8001-3

Input Bias Current



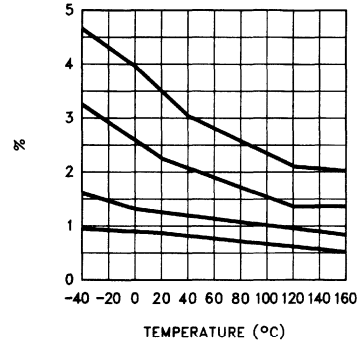
8001-4

Output Voltage Offset



8001-5

Gain Accuracy @1k



8001-6

Buffers

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

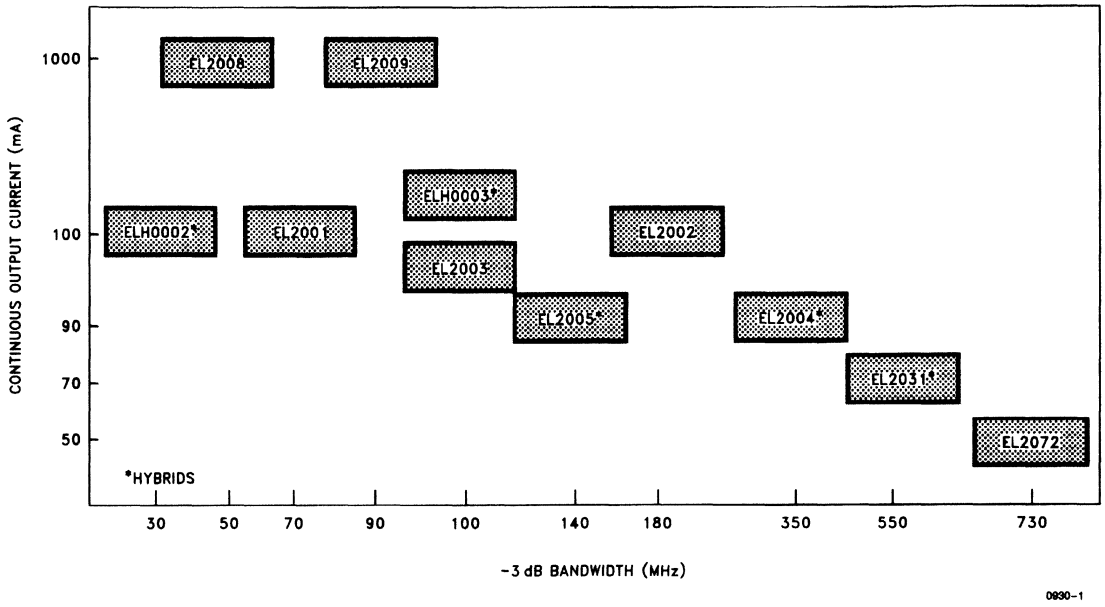
élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec Buffers

***Listed in order of decreasing bandwidth.**

ELANTEC Part Number	Description	Full Temp Warmed Up Input Current (Input Impedance)	Continuous Output Current Drive (Peak Output Current)	Typical −3 dB* Bandwidth (Risetime)	Typical Slew Rate	Max Supply Current	Packages
EL2072C	730 MHz, Closed Loop Buffer	±50 μA Max (100 kΩ Min)	±50 mA (±70 mA)	730 MHz (0.4 ns)	800 V/μs	20 mA	8-Pin P-DIP 8-Pin SO
EL2031C	500 MHz, 5000 V/μs (Min) FET Input, Internal Bypass Cap., Hybrid, Next Generation EL2004	1 μA Max (4000 MΩ Typ)	±70 mA (±100 mA)	550 MHz (650 ps into 100Ω Load)	7000 V/μs	26 mA	12-Pin TO-8
EL2002C	Monolithic, Low Cost, Low Power, 180 MHz BW, Current Limited	20 μA Max (1 MΩ Min) 100k Min	100 mA Out ±100 mA Min Current Limits at ±130 mA Typical	180 MHz (2.8 ns Typ)	2000 V/μs	5 mA 5 mA Typ	8-Pin P-DIP 20-Lead SOL
EL2003C	Monolithic, Excellent Video Buffer. Improved ELH0002, HA2-5002 & HA4-5002	50 μA Max (1 MΩ Min)	±105 mA Min (±230 mA)	100 MHz (4 ns)	1200 V/μs	15 mA	TO-99 8-Pin P-DIP 20-Lead SOL
EL2033C	Monolithic, C.B., Improved Pin-for-Pin with DIP HA-5002, HA-5033, OPA633	±50 μA Max (1 MΩ Min)	±105 mA Min (±230 mA)	100 MHz (4 ns)	1200 V/μs	15 mA	8-Pin P-DIP
EL2009C	Monolithic, 90 MHz, 1A Out Video Buffer	±200 μA Max (250 kΩ Min)	±1A Min	90 MHz (3.9 ns)	2000 V/μs	65 mA	TO-220
EL2001C	Monolithic, Low Cost Very Low Power, 70 MHz BW, Current Limited	10 μA Max (1 MΩ Min)	100 mA Out ±100 mA Min Current Limits at ±130 mA Typical	70 MHz (4.2 ns)	2000 V/μs	1.3 mA Typ 1 mA	8-Pin P-DIP 20-Pin SOL
EL2008C	Monolithic, 55 MHz, 1A Out Video Buffer	±50 μA Max (500 kΩ Min)	±1A Min	55 MHz (7 ns)	2000 V/μs	22 mA	TO-220

Buffers


CONTINUOUS OUTPUT CURRENT (mA)
1000
100
90
70
50
EL2008
EL2009
ELH0003*
ELH0002*
EL2001
EL2003
EL2002
EL2005*
EL2004*
EL2031*
EL2072
*HYBRIDS
30
50
70
90
100
140
180
350
550
730
-3 dB BANDWIDTH (MHz)
0690-1

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2001C
Low Power, 70 MHz Buffer Amplifier

Features

- 1.3 mA supply current
- 70 MHz bandwidth
- 2000 V/μs slew rate
- Low bias current, 1 μA typical
- 100 mA output current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range $\pm$5V to $\pm$15V
- No thermal runaway

Applications

- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Low standby current systems

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2001ACN	0°C to +75°C	P-DIP	MDP0031
EL2001CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2001CN	0°C to +75°C	P-DIP	MDP0031

Manufactured under U.S. Patent No. 4,833,424

General Description

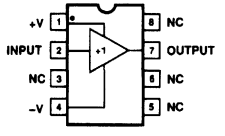
The EL2001 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a -3 dB bandwidth of 70 MHz, and delivers 100 mA, yet draws only 1.3 mA of supply current. It typically operates from $\pm$15V power supplies but will work with as little as $\pm$5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. A typical example is a general purpose op amp output current booster where the buffer must have sufficiently high bandwidth and low phase shift at the maximum frequency of the op amp.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

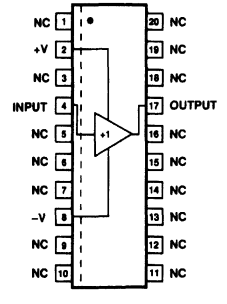
Connection Diagrams

EL2001 DIP Pinout



Top View

EL2001 SOL Pinout



Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

EL2001C
Low Power, 70 MHz Buffer Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_J	Operating Junction Temperature	150°C
V_{IN}	Input Voltage (Note 1)	±15V or V_S	T_{ST}	Storage Temperature	−65°C to +150°C
I_{IN}	Input Current (Note 1)	±50 mA		Lead Temperature	
P_D	Power Dissipation (Note 2)	See Curves		DIP Package (Soldering, < 10 seconds)	300°C
	Output Short Circuit			SOL Package	
	Duration (Note 3)	Continuous		Vapor Phase (60 seconds)	215°C
T_A	Operating Temperature Range			Infrared (15 seconds)	220°C
	EL2001AC/EL2001C	0°C to +75°C			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX9002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX9002.
III	QA sample tested per QA test plan QCX9002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			EL2001AC EL2001C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage EL2001A/EL2001AC	0	∞	25°C	−10	2	I	I	mV
				T_{MIN}, T_{MAX}	−15		+15	III	mV
	EL2001/EL2001C	0	∞	25°C	−30	2	+30	I	mV
				T_{MIN}, T_{MAX}	−40		+40	III	mV
I_{IN}	Input Current EL2001A/EL2001AC	0	∞	25°C	−3	1	+3	I	µA
				T_{MIN}, T_{MAX}	−6		+6	III	µA
	EL2001/EL2001C	0	∞	25°C	−5	1	+5	I	µA
				T_{MIN}, T_{MAX}	−10		+10	III	µA
R_{IN}	Input Resistance	±12V	100Ω	25°	3	8		I	MΩ
				T_{MIN}, T_{MAX}	1			III	MΩ

EL2001C
Low Power, 70 MHz Buffer Amplifier

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			EL2001AC EL2001C	Units
		V_{in}	Load	Temp	Min	Typ	Max	Test Level	
A_{V1}	Voltage Gain	±12V	∞	25°C	0.990	0.998		I	V/V
				T_{MIN}, T_{MAX}	0.985			III	V/V
A_{V2}	Voltage Gain	±10V	100Ω	25°C	0.83	0.93		I	V/V
				T_{MIN}, T_{MAX}	0.80			III	V/V
A_{V3}	Voltage Gain with $V_S = \pm 5V$	±3V	100Ω	25°C	0.82	0.89		I	V/V
				T_{MIN}, T_{MAX}	0.79			III	V/V
V_O	Output Voltage Swing	±12V	100Ω	25°C	±10	±11		I	V
				T_{MIN}, T_{MAX}	±9.5			III	V
R_{OUT}	Output Resistance	±2V	100Ω	25°C		10	15	I	Ω
				T_{MIN}, T_{MAX}			18	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	±100	±160		I	mA
				T_{MIN}, T_{MAX}	±95			III	mA
I_S	Supply Current	0	∞	25°C		1.3	2.0	I	mA
				T_{MIN}, T_{MAX}			2.5	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	75		I	dB
				T_{MIN}, T_{MAX}	50			III	dB
t_r	Rise Time	0.5V	100Ω	25°C		4.2		V	ns
t_d	Propagation Delay	0.5V	100Ω	25°C		2.0		V	ns
SR	Slew Rate, (Note 6)	±10V	100Ω	25°C	1200	2000		IV	V/μs

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

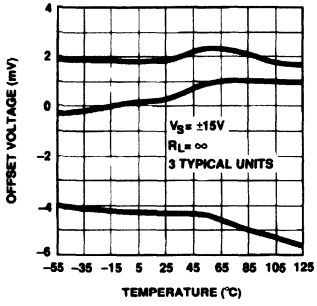
Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12 V_{IN} and −10V on the output.

Note 5: V_{OS} is measured at $V_S+ = +4.5V$, $V_S- = -4.5V$ and at $V_S+ = +18V$, $V_S- = -18V$. Both supplies are changed simultaneously.

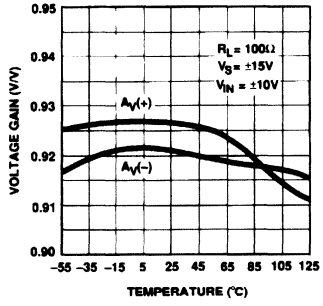
Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$.

Typical Performance Curves

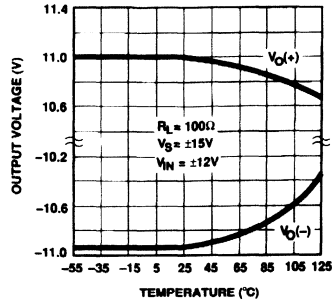
Offset Voltage vs Temperature



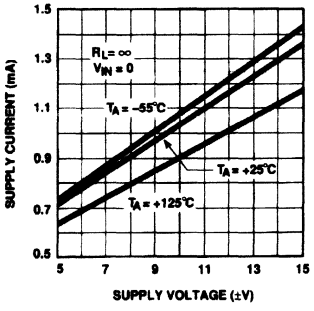
Voltage Gain vs Temperature



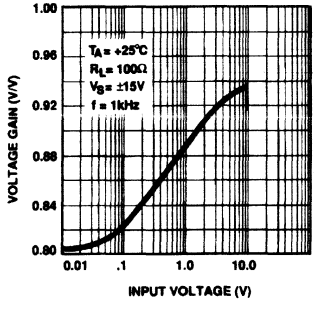
Output Voltage Swing vs Temperature



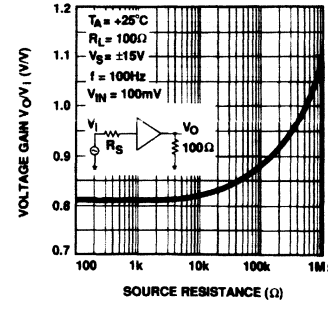
Supply Current vs Supply Voltage



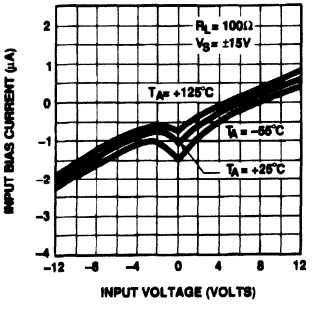
Voltage Gain vs Input Voltage



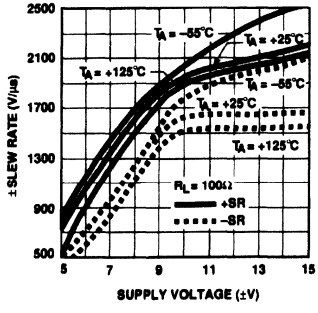
Voltage Gain vs Source Resistance



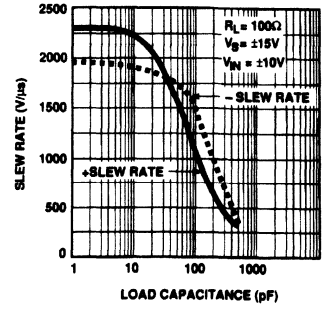
Input Bias Current vs Input Voltage



±Slew Rate vs Supply Voltage



±Slew Rate vs Capacitive Load



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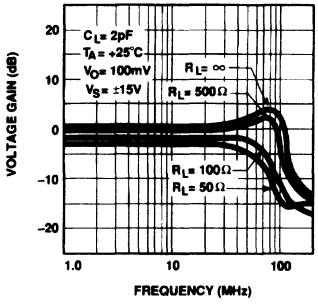
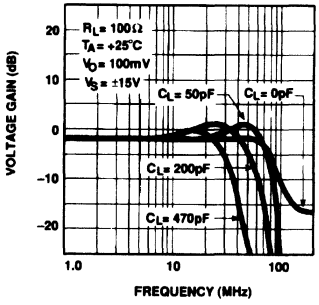
EL2001C
Low Power, 70 MHz Buffer Amplifier

Typical Performance Curves — Contd.

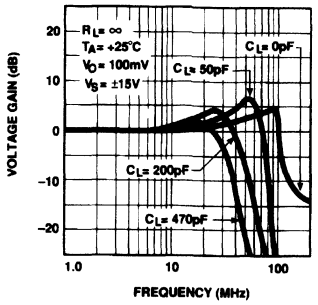
Voltage Gain vs Frequency for Various Resistive Loads



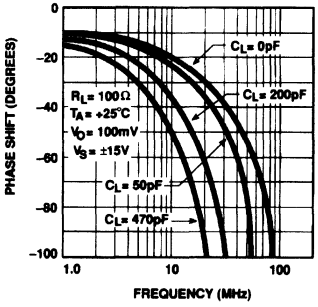
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = 100Ω



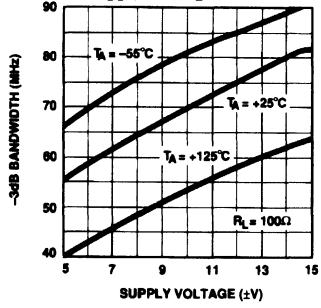
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = ∞



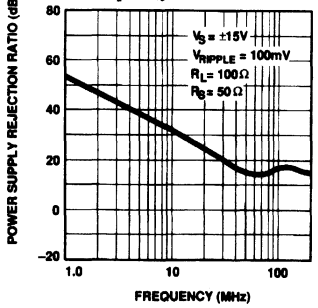
Phase Shift vs Frequency for Various Capacitive Loads



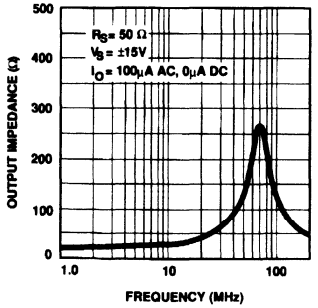
−3 dB Bandwidth vs Supply Voltage



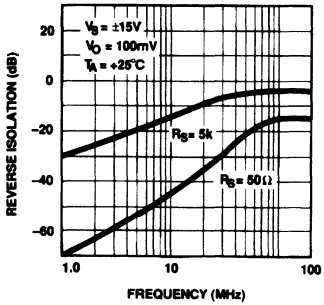
Power Supply Rejection Ratio vs Frequency



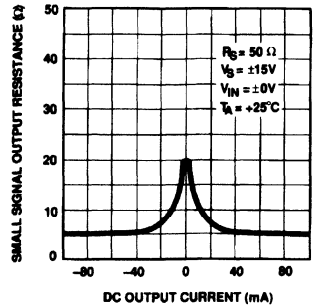
Output Impedance vs Frequency



Reverse Isolation vs Frequency



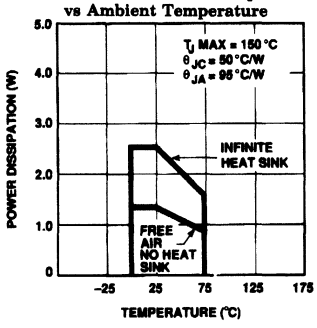
Small Signal Output Resistance vs Output Current



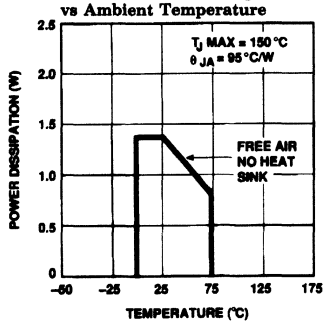
2001-5

Typical Performance Curves — Contd.

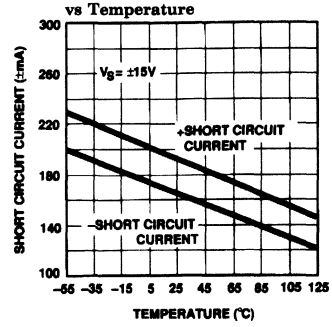
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature

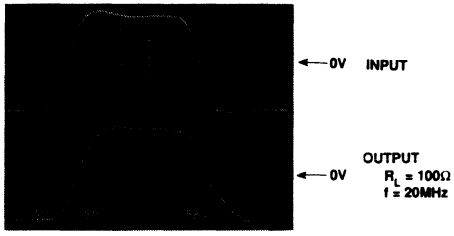


Short Circuit Current
vs Temperature



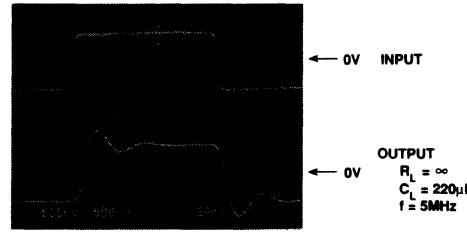
2001-6

Large Signal Response



2001-7

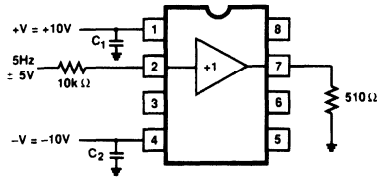
Small Signal Response



2001-8

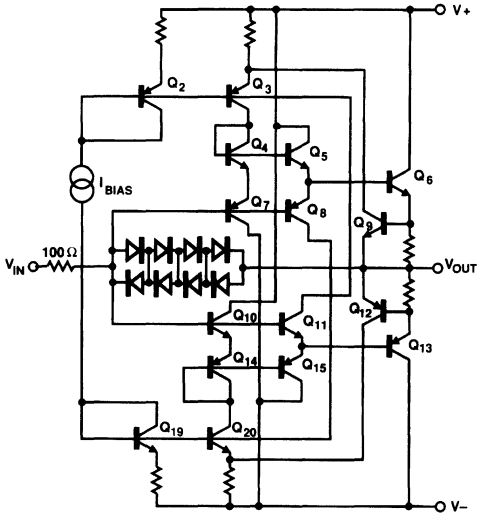
EL2001C
Low Power, 70 MHz Buffer Amplifier

Burn-In Circuit



2001-9

Simplified Schematic



2001-10

Application Information

The EL2001 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2001 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/μs slew rates with 100Ω loads possible with very low supply current.

Power Supplies

The EL2001 may be operated with single or split supplies with total voltage difference between 10V ($\pm$5V) and 36V ($\pm$18V). It is not necessary to use equal split value supplies. For example $-$5V and $+$12V would be excellent for signals from $-$2V to $+$9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2001 looks like a resistance in parallel with about 3.5 picofarads in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about $\pm$2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above $\pm$7.5V differential input to output, additional series resistance should be added.

Source Impedance

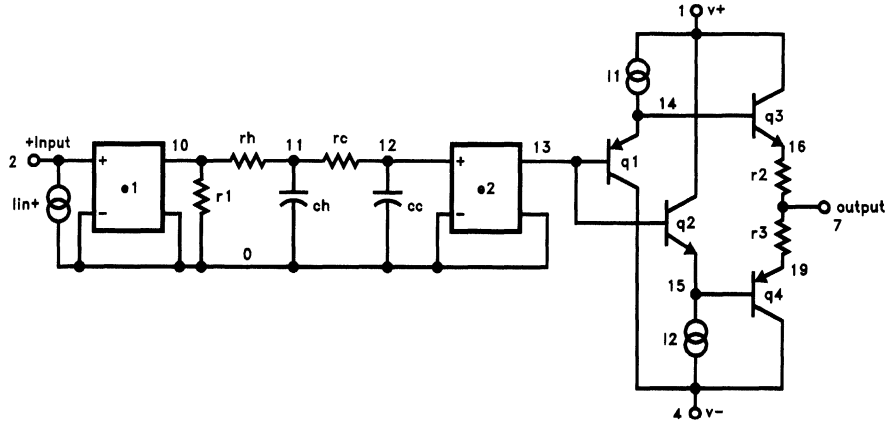
The EL2001 has good input to output isolation. When the buffer is not used in a feedback loop, capactive and resistive sources up to 1 Meg present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (R_S > 100 kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

EL2001C Macromodel

```
*Connections:   +input
*               |     +Vsupply
*               |     |     -Vsupply
*               |     |     |     output
*               |     |     |     |
.subckt M2001   2     1     4     7
* Input Stage
el 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 9pF
rc 11 12 100
cc 12 0 4pF
e2 13 0 12 0 1.0
* Output stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 1
r3 19 7 1
i1 1 14 0.9mA
i2 15 4 0.9mA
* Bias Current
iin+ 2 0 1uA
* Models
.model qn npn(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.model qp pnp(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.ends
```

EL2001C
Low Power, 70 MHz Buffer Amplifier

EL2001C Macromodel — Contd.



2001-11

EL2002C
Low Power, 180 MHz Buffer Amplifier

Features

- 180 MHz bandwidth
- 2000 V/μs slew rate
- Low bias current, 3 μA typical
- 100 mA output current
- 5 mA supply current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range $\pm$5V to $\pm$15V
- No thermal runaway

Applications

- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Isolation buffer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2002ACN	0°C to +75°C	P-DIP	MDP0031
EL2002CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2002CN	0°C to +75°C	P-DIP	MDP0031

General Description

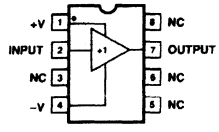
The EL2002 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a -3 dB bandwidth of 180 MHz, and delivers 100 mA, yet draws only 5 mA of supply current. It typically operates from $\pm$15V power supplies but will work with as little as $\pm$5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. Typical examples include fast op-amp output current boosters, coaxial cable drivers and A/D converter input buffers.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagrams

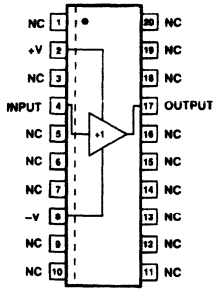
EL2002 DIP Pinout



2002-1

Top View

EL2002 SOL Pinout



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Top View

Manufactured Under U.S. Patent No. 4,833,424

EL2002C
Low Power, 180 MHz Buffer Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage ($V^+ - V^-$)	±18V or 36V
V_{IN}	Input Voltage (Note 1)	±15V or V_S
I_{IN}	Input Current (Note 1)	±50 mA
P_D	Power Dissipation (Note 2)	See Curves
	Output Short Circuit Duration (Note 3)	Continuous
T_A	Operating Temperature Range: EL2002AC/EL2002C	0°C to +75°C
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature	−65°C to +150°C
	Lead Temperature	
	DIP Package (soldering, <10 seconds)	300°C
	SOL Package	
	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

(START)

Parameter	Description	Test Conditions			Limits			EL2002AC EL2002C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage EL2002A/EL2002AC	0	∞	25°C	−15	5	+15	I	mV
				T_{MIN}, T_{MAX}	−20		+20	III	mV
	EL2002/EL2002C	0	∞	25°C	−40	10	+40	I	mV
				T_{MIN}, T_{MAX}	−50		+50	III	mV
I_{IN}	Input Current EL2002A/EL2002AC	0	∞	25°C	−10	3	+10	I	µA
				T_{MIN}, T_{MAX}	−15		+15	III	µA
	EL2002/EL2002C	0	∞	25°C	−15	5	+15	I	µA
				T_{MIN}, T_{MAX}	−20		+20	III	µA
R_{IN}	Input Resistance	+12V	100Ω	25°C	1	3		I	MΩ
				T_{MIN}, T_{MAX}	0.1			III	MΩ
A_{V1}	Voltage Gain	±12V	∞	25°C	0.990	0.998		I	V/V
				T_{MIN}, T_{MAX}	0.985			III	V/V
A_{V2}	Voltage Gain	±10V	100Ω	25°C	0.85	0.93		I	V/V
				T_{MIN}, T_{MAX}	0.83			III	V/V

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			EL2002AC EL2002C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	
A_{V3}	Voltage Gain with $V_S = \pm 5V$	±3V	100Ω	25°C	0.83	0.91		I	V/V
				T_{MIN}, T_{MAX}	0.80			III	V/V
V_O	Output Voltage Swing	±12V	100Ω	25°C	±10	±11		I	V
				T_{MIN}, T_{MAX}	±9.5			III	V
R_{OUT}	Output Resistance	±2V	100Ω	25°C		8	13	I	Ω
				T_{MIN}, T_{MAX}			15	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	+100	+160		I	mA
				T_{MIN}, T_{MAX}	±95			III	mA
I_S	Supply Current	0	∞	25°C		5	7.5	II	mA
				T_{MIN}, T_{MAX}			10	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	75		I	dB
				T_{MIN}, T_{MAX}	50			III	dB
t_r	Rise Time	0.5V	100Ω	25°C		2.8		V	ns
t_d	Propagation Delay	0.5V	100Ω	25°C		1.5		V	ns
SR	Slew Rate, (Note 6)	±10V	100Ω	25°C	1200	2000		IV	V/μs

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12 V_{IN} and −10V on the output.

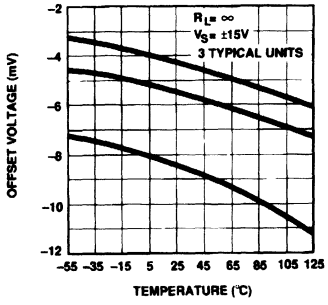
Note 5: V_{OS} is measured at $V_S+ = +4.5V$, $V_S- = -4.5V$ and $V_S+ = +18V$, $V_S- = 18V$. Both supplies are changed simultaneously.

Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$.

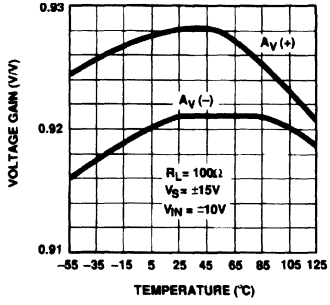
EL2002C
Low Power, 180 MHz Buffer Amplifier

Typical Performance Curves

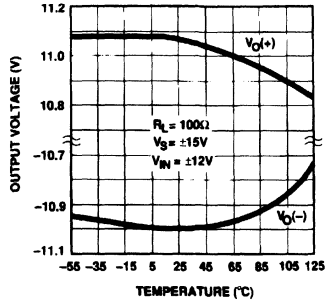
Offset Voltage vs Temperature



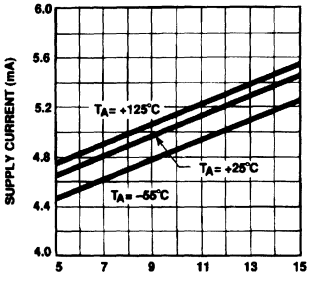
Voltage Gain vs Temperature



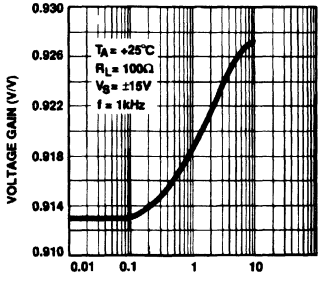
Output Voltage Swing vs Temperature



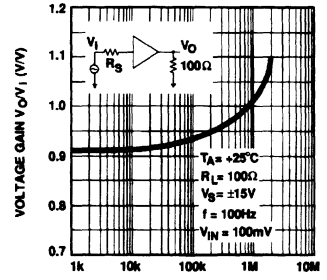
Supply Current vs Supply Voltage



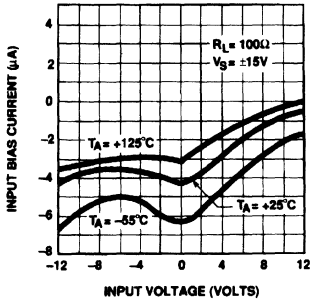
Voltage Gain vs Input Voltage



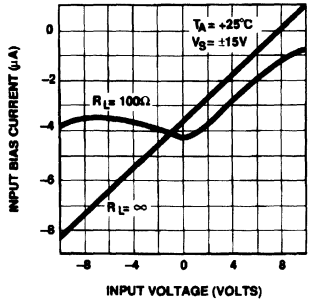
Voltage Gain vs Source Resistance



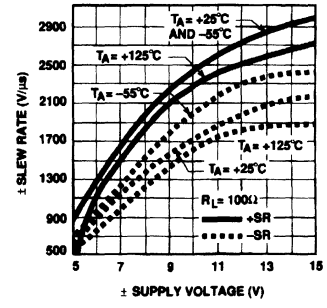
Input Bias Current vs Input Voltage at Various Temperatures



Input Bias Current vs Input Voltage



±Slew Rate vs Supply Voltage



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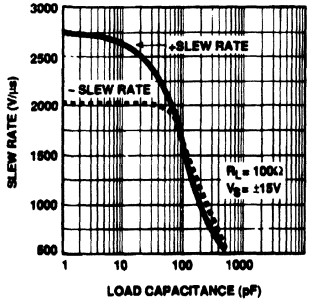
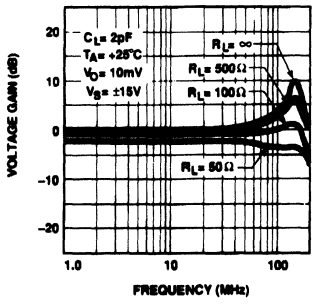
Typical Performance Curves — Contd.

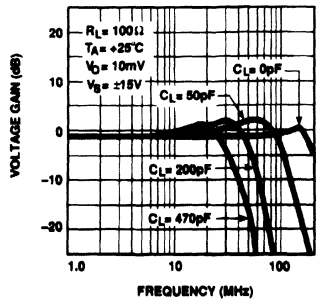
Slew Rate vs Load Capacitance



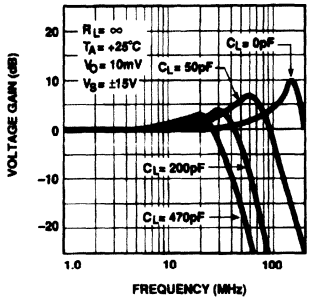
Voltage Gain vs Frequency for Various Resistive Loads



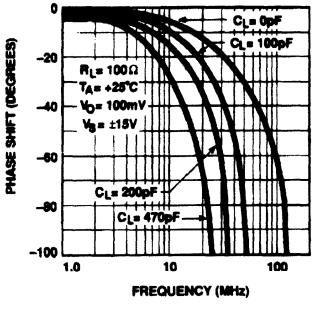
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = 100Ω



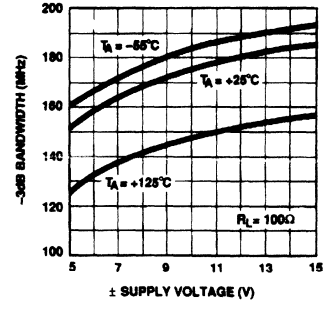
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = ∞



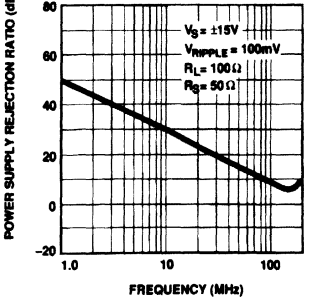
Phase Shift vs Frequency for Various Capacitive Loads



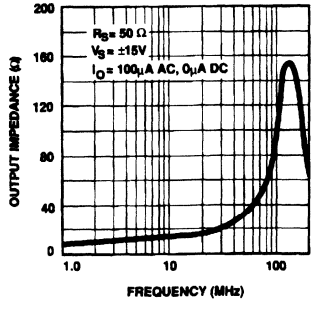
−3 dB Bandwidth vs Supply Voltage



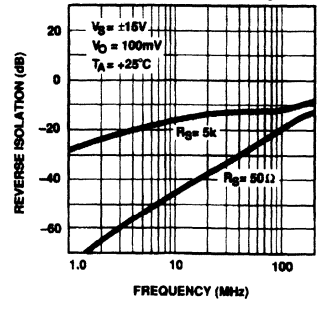
Power Supply Rejection Ratio vs Frequency



Output Impedance vs Frequency



Reverse Isolation vs Frequency



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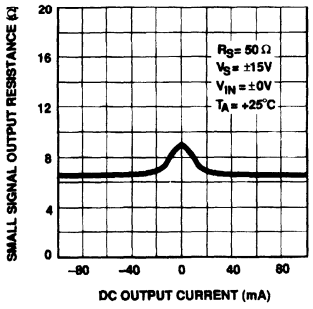
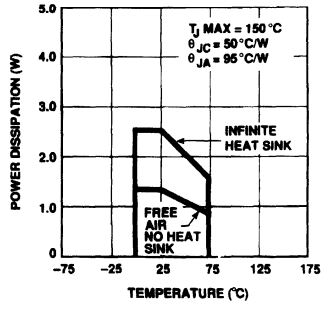
EL2002C
Low Power, 180 MHz Buffer Amplifier

Typical Performance Curves — Contd.

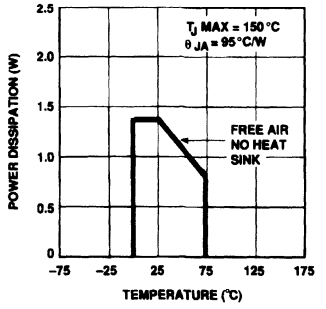
Small Signal Output Resistance vs Output Current



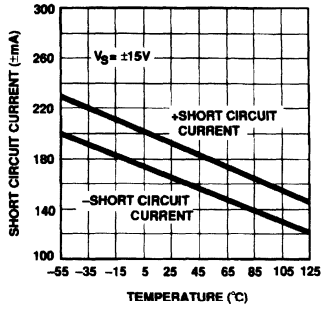
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature

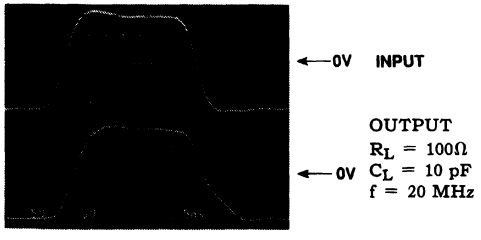


Short Circuit Current vs Temperature



2002-6

Large Signal Response



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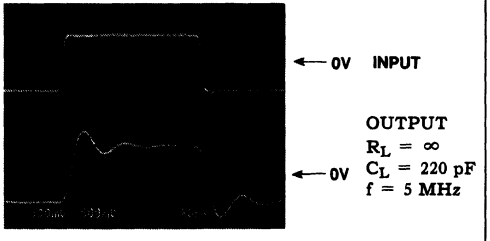
Small Signal Response



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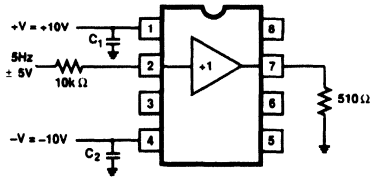
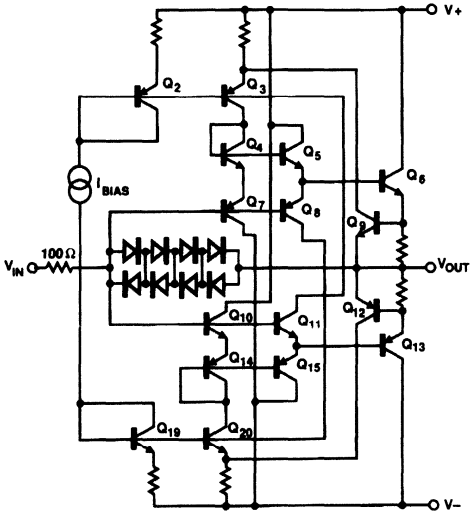
Burn-In Circuit



2002-10

Simplified Schematic



2002-11

Application Information

The EL2002 is a monolithic buffer amplifier built on Elantec's proprietary Complementary Bipolar process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2002 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2002's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/μs slew rates with 100Ω loads possible with very low supply current.

Power Supplies

The EL2002 may be operated with single or split supplies with total voltage difference between 10V ($\pm$5V) and 36V ($\pm$18V). It is not necessary to use equal split value supplies. For example $-$5V and $+$12V would be excellent for signals from $-$2V to $+$9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2002 looks like a resistance in parallel with about 3.5 pF in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about $\pm$2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above $\pm$7.5V differential input to output, additional series resistance should be added.

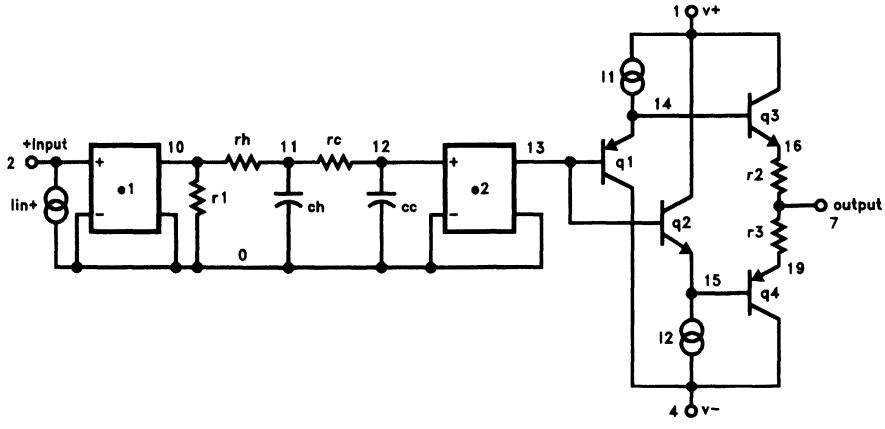
Source Impedance

The EL2002 has good input to output isolation. When the buffer is not used in a feedback loop, capacitive and resisitive sources up to 1 MHz present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (R_S > 100 kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

EL2002 Macromodel

```
* Connections:      +input
*                   |     +Vsupply
*                   |     |     -Vsupply
*                   |     |     |     output
*                   |     |     |     |
.subckt M2002       2     1     4     7
* Input Stage
e1 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 2pF
rc 11 12 100
cc 12 0 3pF
e2 13 0 12 0 1.0
* Output Stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 1
r3 19 7 1
i1 1 14 2mA
i2 15 4 2mA
* Bias Current
iin+ 2 0 3uA
* Models
.model qn npn(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.model qp pnp(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.ends
```

EL2002 Macromodel — Contd.



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EL2003C/EL2033C
100 MHz Video Line Driver

Features

- Differential gain 0.1%
- Differential phase 0.1°
- 100 mA continuous output current guaranteed
- Short circuit protected
- Wide bandwidth—100 MHz
- High slew rate—1200 V/μs
- High input impedance—2 MΩ
- Low quiescent current drain
- EL2003—Pin compatible with LH0002CN, LH0002H, HA2-5002
- EL2033—Pin compatible with HA3-5002, HA7-5002, HA3-5033, HA7-5033

Applications

- Co-ax cable driver
- Flash converter driver
- Video DAC buffer
- Op amp booster

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2003CN	0°C to +75°C	P-DIP	MDP0031
EL2003CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2033CN	0°C to +75°C	P-DIP	MDP0031

General Description

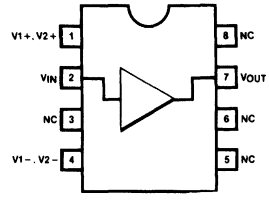
The EL2003/EL2033 are general purpose monolithic unity gain buffers featuring 100 MHz, −3 dB bandwidth and 4 ns small signal rise time. These buffers are capable of delivering a ±100 mA current to a resistive load and are oscillation free into capacitive loads. In addition, the EL2003/EL2033 have internal output short circuit current limiting which will protect the devices under both a DC fault condition and AC operation with reactive loads. The extremely fast slew rate of 1200 V/μs, wide bandwidth, and high output drive make the EL2003/EL2033 ideal choices for closed loop buffer applications with wide band op amps. These same characteristics and excellent DC performance make the EL2003/EL2033 excellent choices for open loop applications such as driving coaxial and twisted pair cables.

The EL2003/EL2033 are constructed using Elantec's proprietary dielectric isolation process that produces PNP and NPN transistors with essentially identical AC and DC characteristics.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, request our brochure: QRA-1: *Elantec's Processing—Monolithic Products.*

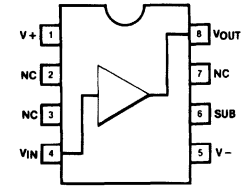
Connection Diagrams

EL2003CN



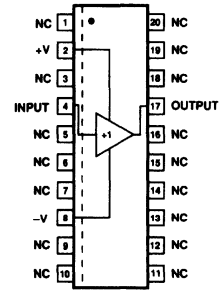
2003-1

EL2033CN



2003-2

EL2003CM



2003-5

Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_J	Operating Junction Temperature	
V_{IN}	Input Voltage (Note 1)	±15V or V_S		Metal Can	175°C
I_{IN}	Input Current (Note 1)	±50 mA		Plastic	150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{ST}	Storage Temperature	−65°C to +150°C
	Output Short Circuit			Lead Temperature	
	Duration (Note 3)	Continuous		(Soldering, <10 seconds)	300°C
T_A	Operating Temperature Range				
	EL2003C/2033C	0°C to +75°C			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max	2003C 2033C	
V_{OS}	Output Offset Voltage	0	∞	25°C	−40	5	40	I	mV
				T_{MIN}, T_{MAX}	−50		50	III	mV
I_{IN}	Input Current	0	∞	25°C, T_{MAX}	−25	−5	25	II	μA
				T_{MIN}	−50		50	III	μA
R_{IN}	Input Resistance	±12V	100Ω	25°C, T_{MAX}	1	2		II	MΩ
				T_{MIN}	0.1			III	MΩ
A_{V1}	Voltage Gain	±12V	1 kΩ	25°C	0.98	0.99		I	V/V
				T_{MIN}, T_{MAX}	0.97			III	V/V
A_{V2}	Voltage Gain	±6V	50Ω	25°C	0.83	0.90		I	V/V
				T_{MIN}, T_{MAX}	0.80			III	V/V
A_{V3}	Voltage Gain with V_S = ±5V	±3V	50Ω	25°C	0.82	0.89		I	V/V
				T_{MIN}, T_{MAX}	0.79			III	V/V
V_{O1}	Output Voltage Swing	±14V	1 kΩ	25°C	±13	±13.5		I	V
				T_{MIN}, T_{MAX}	±12.5			III	V
V_{O2}	Output Voltage Swing	±12V	100Ω	25°C	±10.5	±11.3		I	V
				T_{MIN}, T_{MAX}	±10			III	V

EL2003C/EL2033C
100 MHz Video Line Driver

Electrical Characteristics $V_S = \pm 15V, R_S = 50\Omega$ — Contd.

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max	2003C 2033C	
R_{OUT}	Output Resistance	±2V	50Ω	25°C		7	10	I	Ω
				T_{MIN}, T_{MAX}			12	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	±105	±230		I	mA
				T_{MIN}, T_{MAX}	±100			III	mA
I_S	Supply Current	0	∞	25°C, T_{MAX}		10	15	II	mA
				T_{MIN}			20	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	80		I	dB
				T_{MIN}, T_{MAX}	50			III	dB
SR1	Slew Rate, (Note 6)	±10V	1 kΩ	25°C	600	1200		I	V/μs
SR2	Slew Rate, (Note 7)	±5V	50Ω	25°C	200	400		I	V/μs
THD	Distortion @ 1 kHz	4 V_{rms}	50Ω	25°C		0.2	1	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V in and −10V on the output.

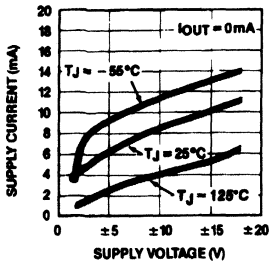
Note 5: $V_S = \pm 4.5V$ to ±18V.

Note 6: Slew rate is measured between $V_{OUT} = +5V$ and −5V.

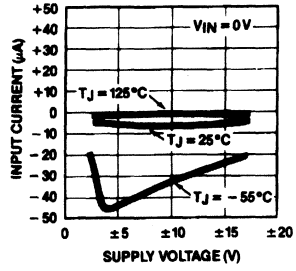
Note 7: Slew rate is measured between $V_{OUT} = +2.5V$ and −2.5V.

Typical Performance Curves

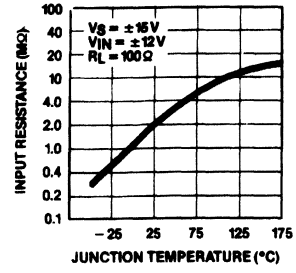
Quiescent Supply Current vs Supply Voltage



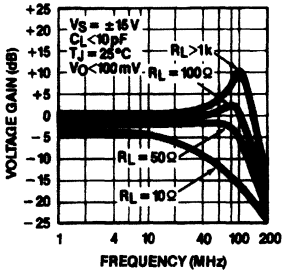
Input Current vs Supply Voltage



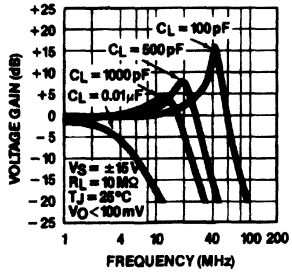
Input Resistance vs Temperature



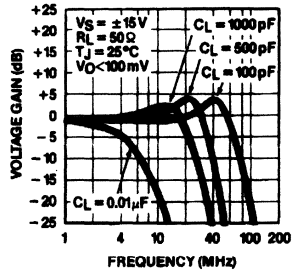
Voltage Gain vs Frequency Various Resistive Loads



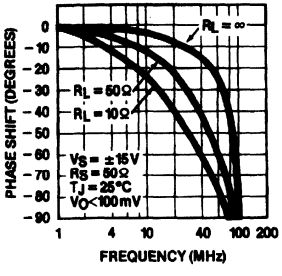
Voltage Gain vs Frequency No Resistive Load Various Capacitive Loads



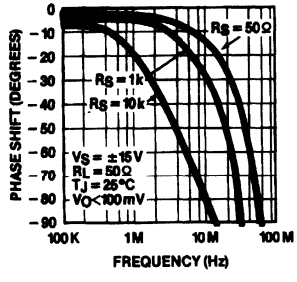
Voltage Gain vs Frequency 50Ω Resistive Load Various Capacitive Loads



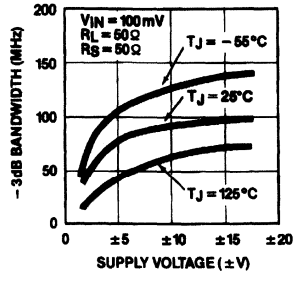
Phase Shift vs Frequency Various Resistive Loads



Phase Shift vs Frequency Various Source Resistors



−3 dB Bandwidth vs Supply Voltage



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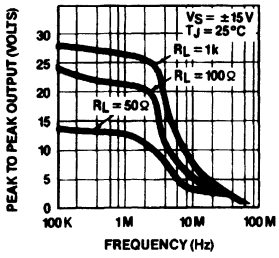
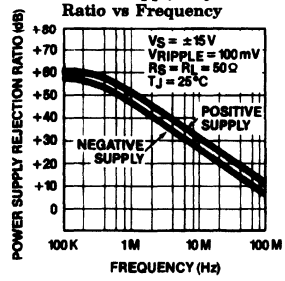
EL2003C/EL2033C
100 MHz Video Line Driver

Typical Performance Curves — Contd.

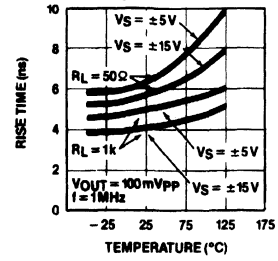
Maximum Undistorted Output Voltage vs Frequency



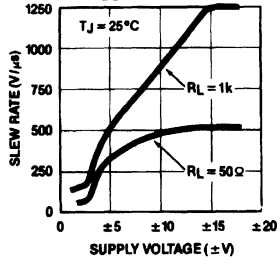
Power Supply Rejection Ratio vs Frequency



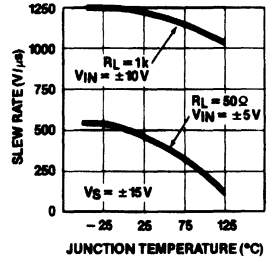
Rise Time vs Temperature



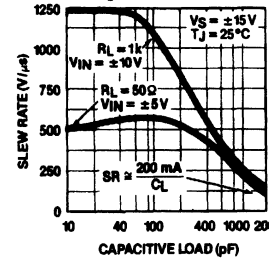
Slew Rate vs Supply Voltage



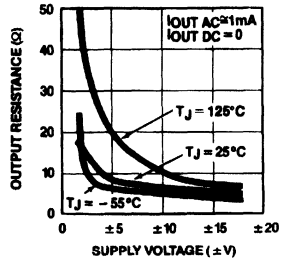
Slew Rate vs Temperature



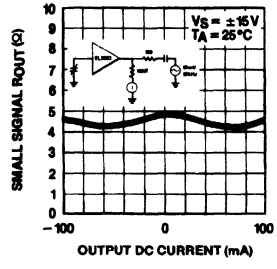
Slew Rate vs Capacitive Load



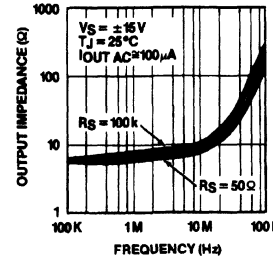
Output Resistance vs Supply Voltage



Small Signal Output Resistance vs DC Output Current



Output Impedance vs Frequency



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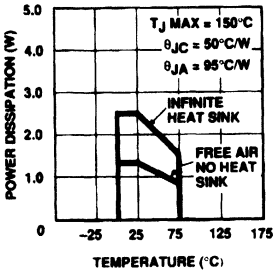
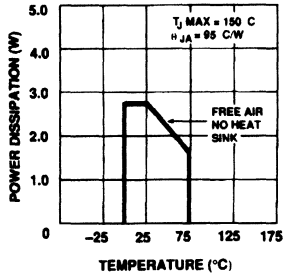
Typical Performance Curves — Contd.

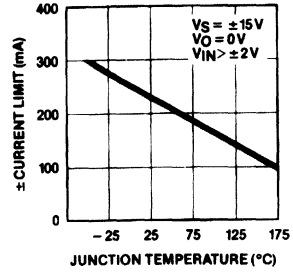
8-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



Current Limit
vs Temperature



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2

EL2003C/EL2033C
100 MHz Video Line Driver

Applications Hints

The EL2003/EL2033 are monolithic buffer amplifiers built with Elantec's proprietary dielectric isolation process that produces NPN and PNP complimentary transistors. The circuits are connection of symmetrical common collector transistors that provide both sink and source current capability independent of output voltage while maintaining constant output and input impedances. The high slew rate and wide bandwidth of the EL2003 and EL2033 make them useful beyond video frequencies.

Power Supplies

The EL2003/EL2033 may be operated with single or split supplies as low as ±2.5V (5V total) to as high as ±18V (36V total). However, the bandwidth, slew rate and output impedance degrade significantly for supply voltages less than ±5V (10V total) as shown in the characteristic curves. It is not necessary to use equal value split supplies, for example −5V and +12V would be excellent for 0V to 1V video signals.

Bypass capacitors from each supply pin to a ground plane are recommended. The EL2003/EL2033 will not oscillate even with minimal bypassing, however, the supply will ring excessively with inadequate capacitance. To eliminate a supply ringing and the interference it can cause, a 10 μF tantalum capacitor with short leads is recommended for both supplies. Inadequate supply bypassing can also result in lower slew rates and longer settling times.

The EL2003 metal can package has the collectors of the output transistors brought out separately from the input supplies for pin compatibility with the ELH0002H. If the collectors operate on lower supplies than the input stage, the internal power dissipation can be reduced. However, the output transistors can be driven into hard saturation when the input voltage exceeds the collector supply voltage. The recovery time to come out of saturation will be 2 μs or 3 μs and the output may oscillate during this recovery period.

Input Range

The input to the EL2003/EL2033 looks like a high resistance in parallel with a few picofarads in addition to a DC bias current. The input characteristics change very little with output loading, even when the amplifier is in current limit. However, there are clamp diodes from the input to the output that protect the transistor base emitter junctions. These diodes start to conduct at about ±9.5V input to output differential voltage. Of course the input resistance drops dramatically when the diodes start conducting; the diodes are rated at ±50 mA.

The input characteristics also change when the input voltage exceeds either supply by 0.5V. This happens because the input transistor's base-collector junctions forward bias. If the input exceeds the supply by LESS than 0.5V and then returns to the normal input range, the output will recover in less than 10 ns. However, if the input exceeds the supply by MORE than 0.5V, the recovery time can be 100's of nanoseconds. For this reason it is recommended that schottky diode clamps from input to supply be used if a fast recovery from large input overloads is required.

Source Impedance

The EL2003/EL2033 have excellent input-output isolation and are very tolerant of variations in source impedances. Capacitive sources cause no problems at all, resistive sources up to 100 kΩ present no problems as long as care is used in board layout to minimize output to input coupling. Inductive sources can cause oscillations; a 1 kΩ resistor in series with the buffer input lead will usually eliminate problems without sacrificing too much speed. An unterminated cable or other resonant source can also cause oscillations. Again, an isolating resistor will eliminate the problem.

Current Limit

The EL2003/EL2033 have internal current limits that protect the output transistors. The current limit goes down with junction temperature rise as shown in the characteristic curves. At a junction temperature of +175°C the current limits are at about 100 mA. If the EL2003 or EL2033 output is shorted to ground when operating on ±15V supplies, the power dissipation will be greater than 1.5W. A heat sink is required in order for the EL2003 or EL2033 to survive an indefinite short. Recovery time to come out of current limit is about 250 ns.

Applications Hints — Contd.

Heat Sinking

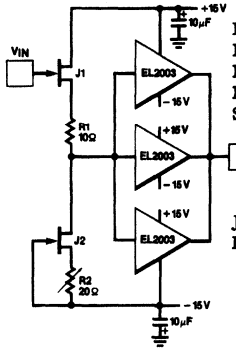
When operating the EL2003/EL2033 in elevated ambient temperatures and/or high supply voltages and low impedance loads, the internal power dissipation can force the junction temperature above the maximum rating (175°C for the metal can package and 150°C for the plastic DIP). Also, an indefinite short of the output to ground will cause excessive power dissipation.

The thermal resistance junction to case is 55°C per Watt for the metal can package and 50°C/W for the plastic DIP. A suitable heat sink will increase the power dissipation capability significantly beyond that of the package alone. Several companies make standard heat sinks for both packages. Aavid and Thermalloy heat sinks have been used successfully.

Parallel Operation

If more than 100 mA output is required or if heat management is a problem, several EL2003s or EL2033s may be paralleled together. The result is as though each device was driving only part of the load. For example, if two units are paralleled then a 50Ω load looks like 100Ω to each EL2003. Parallel operation results in lower input and output impedances, increased bias current but no increase in offset voltage. An example showing three EL2003s in parallel and also the addition of a FET input buffer stage is shown below. By using a dual FET the circuit complexity is minimal and the performance is excellent. Take care to minimize the stray capacitance at the input of the EL2003s for maximum slew rate and bandwidth.

FET Input Buffer with High Output Currents



Parallel Operation
$I_{OUT} \geq \pm 300$ mA
$R_{OUT} \cong 2\Omega$
BW ≅ 100 MHz
SR = 1000 V/µs

J1, J2 2N5911 Dual FET
R1, R2 Offset Adjust

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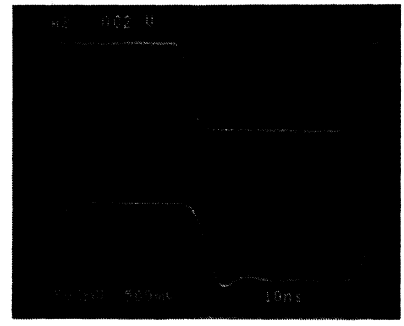
Resistive Loads

The DC gain of the EL2003/EL2033 is the product of the unloaded gain (0.995) and the voltage divider formed by the device output resistance and the load resistance.

$$A_V = 0.995 * R_L/(R_L + R_{OUT})$$

The high frequency response of the EL2003/EL2033 varies with the value of the load resistance as shown in the characteristic curves. If the 100 MHz peaking is undesirable when driving load resistors greater than 50Ω, an RC snubber circuit can be used from the output to ground. The snubber circuit works by presenting a high frequency load resistance of less than 50Ω while having no loading effect at low frequencies.

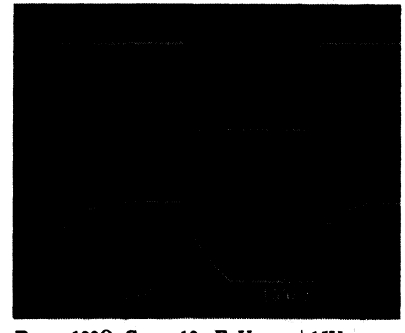
Small Signal Response



$R_L = 50\Omega$, $C_L = 10$ pF, $V_S = \pm 15$V
Top is V_{IN}, Bottom is V_{OUT}

2003-10

Large Signal Response



$R_L = 100\Omega$, $C_L = 10$ pF, $V_S = \pm 15$V
Top is V_{IN}, Bottom is V_{OUT}

2003-11

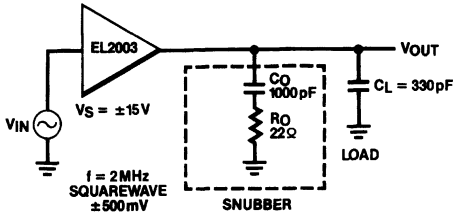
EL2003C/EL2033C
100 MHz Video Line Driver

Applications Hints — Contd.

Capacitive Loads

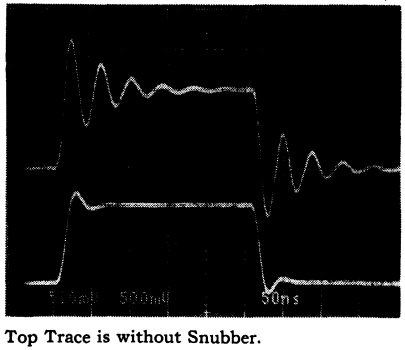
The EL2003/EL2033 are stable driving any type of capacitive load. However, when driving a pure capacitance of less than a thousand picofarads the frequency response has excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and will ring for several hundred ns.

If the peaking and ringing cause system problems they can be eliminated with an RC snubber circuit from the output to ground. The values can be found empirically by observing a squarewave or the frequency response. First just put the resistor alone from output to ground until the desired response is obtained. Of course the gain will be reduced due to R_{OUT}. Then put capacitance in series with the resistor to restore the gain at low frequencies. Start with a small capacitor and increase until the response is optimum. Too large a capacitor will roll the gain off prematurely and result in a longer settling time. The figure below shows an example of an EL2003 driving a 330 pF load, which is similar to the input of a flash converter.



2003-12

Driving a Pure Capacitance



Top Trace is without Snubber.
Bottom Trace is with Snubber Circuit.

2003-13

Inductive Loads

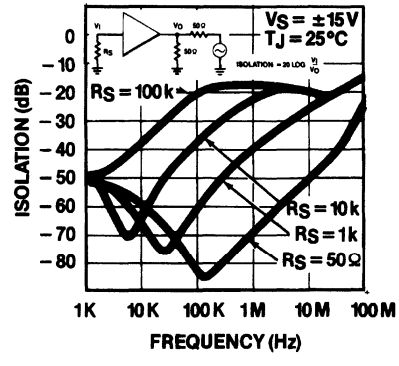
The EL2003/EL2033 can drive small motors, solenoids, LDT's and other inductive loads. Foldback current limiting is NOT used in the EL2003 or EL2033 and current limiting into an inductive load does NOT in and of itself cause spikes or kickbacks. However, if the EL2003 or EL2033 is in current limit and the input voltage is changing quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltage. Motors are also able to generate kickbacks when the EL2003 or EL2033 is in current limit.

To prevent damage to the EL2003/EL2033 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Reverse Isolation

The EL2003/EL2033 have excellent output to input isolation over a wide frequency range. This characteristic is very important when the buffer is used to drive signals between different equipment over cables. Often the cable is not perfect or the termination is improper and reflections occur that act like a signal source at the output of the buffer. Worst case the cable is connected to a source instead of where it is supposed to go. In both situations the buffer must keep these signals from its input. The following curve shows the reverse isolation of the EL2003/EL2033 verses frequency for various source resistors.

Reverse Isolation vs. Frequency



2003-14

Applications Hints — Contd.

Driving Cables

There are at least three ways to use the EL2003 and EL2033 to drive cables, as shown in the adjacent figure. The most obvious is to directly connect the cable to the output of the buffer. This results in a gain determined by the output resistance of the EL2003 or EL2033 and the characteristic impedance of the cable, assuming it is properly terminated. For RG-58 into 50Ω the gain is about −1 dB, exclusive of cable losses. For optimum response and minimum reflections it is important for the cable to be properly terminated.

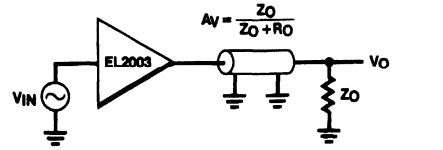
Double termination of a cable is the cleanest way to drive it since reflections are absorbed on both ends of the cable. The cable source resistor is equal to the characteristic impedance of the cable less the output resistance of the EL2003/EL2033. The gain is −6 dB exclusive of the cable attenuation.

Back matching is the last and most interesting way to drive a cable. The cable source resistor is again the characteristic impedance less the output resistance of the EL2003/EL2033; the termination resistance is now much greater than the cable impedance. The gain is 0 dB and DC levels waste no power.

An additional EL2033 or EL2033 make a good receiver at the terminating end. Because an unterminated cable looks like a resonant circuit, the receiving EL2003 or EL2033 should have an isolating resistor in series with its input to prevent oscillations when the cable is not connected to the driver. Of course if the cable is always connected to the back match, no resistor is necessary.

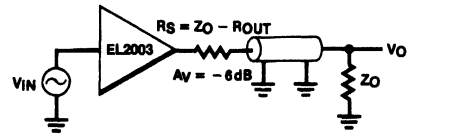
WARNING: ONE END OF A CABLE MUST BE PROPERLY TERMINATED. If neither end is terminated in the cable characteristic impedance, the cable will have standing waves that appear as resonances in the frequency response. The resonant frequencies are a function of the cable length and even relatively short cables can cause problems at frequencies as low as 1 MHz. Longer cables should be terminated on both ends.

Direct Drive



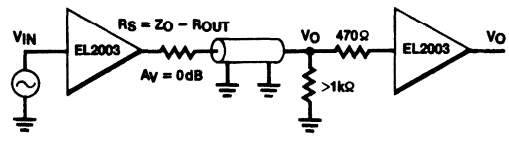
2003-15

Double Matched



2003-16

Back Matched

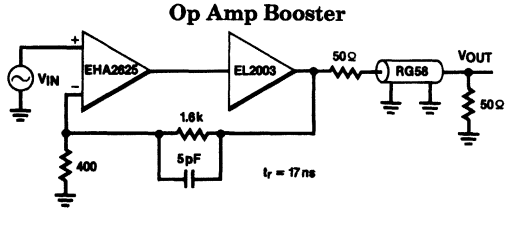


2003-17

Op Amp Booster

The EL2003 or EL2033 can boost the output drive of almost any monolithic op amp. Because the phase shift in the EL2003/EL2033 is low at the op amp's unity gain frequency, no additional compensation is required. By following an op amp with an EL2003 or EL2033, the buffered op amp can drive cables and other low impedance loads directly. Even decompensated high speed op amps can take advantage of the EL2003's or EL2033's 100 mA drive.

Op Amp Booster



2003-18

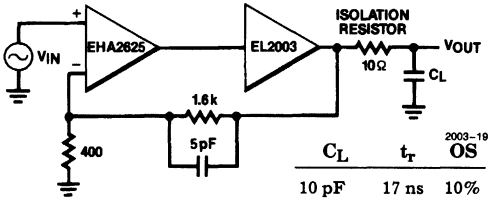
EL2003C/EL2033C
100 MHz Video Line Driver

Applications Hints — Contd.

Driving capacitive loads with any closed loop amplifier creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The output impedance of the EL2003 or EL2033 is less than 10Ω from DC to about 10 MHz, but a capacitive load of 1000 pF will generate about 45 degrees phase shift at 10 MHz and make high speed op amps unstable. Obviously more capacitance will cause the same problem but at lower frequencies, and slower op amps as well would become unstable.

The easiest way to drive capacitive loads is to isolate them from the feedback with a series resistor. Ten to twenty ohms is usually enough but the final value depends on the op amp used and the range of load capacitance.

Op Amp Booster with Capacitive Load



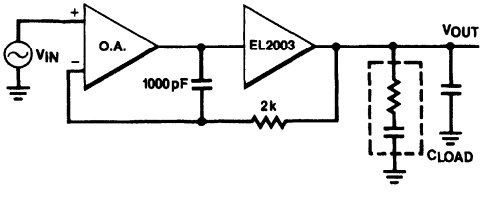
2003-19

C_L	t_r	OS
10 pF	17 ns	10%
470 pF	20 ns	50%
0.001 μF	30 ns	35%
0.005 μF	80 ns	0
0.01 μF	220 ns	0
0.05 μF	1.1 μs	0
0.1 μF	2.2 μs	0

10Ω is enough isolation and speed is determined by the isolation resistor and capacitive load time constant.

If the system requirements will not tolerate the isolation resistor, then additional high frequency feedback from the op amp output (the buffer input) and an isolating resistor from the buffer output is required. This requires that the op amp be unity gain stable.

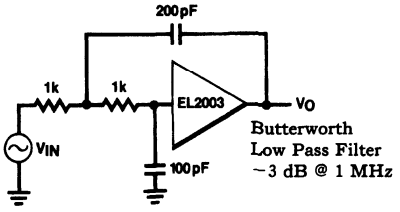
Complex Feedback with the Buffer to Drive Capacitive Loads



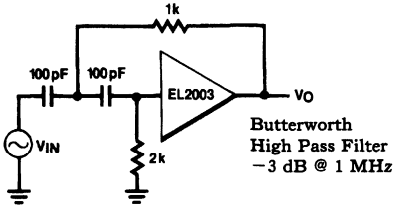
2003-20

This works with any unity gain stable OA. Snubber Circuit (51Ω 470 pF) is optional.

Typical Applications

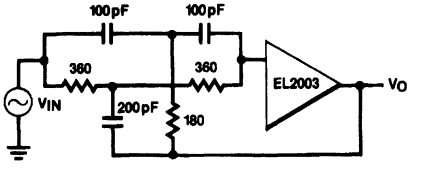


2003-21



2003-22

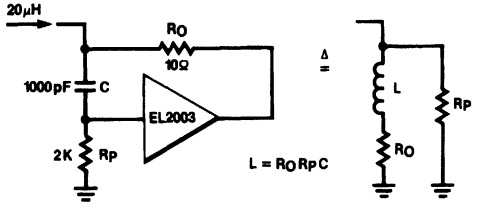
High Q Notch Filter



2003-23

$$f_O = \frac{1}{2\pi\,(100\text{ pF})\,(360)} \approx 4.4\text{ MHz}$$

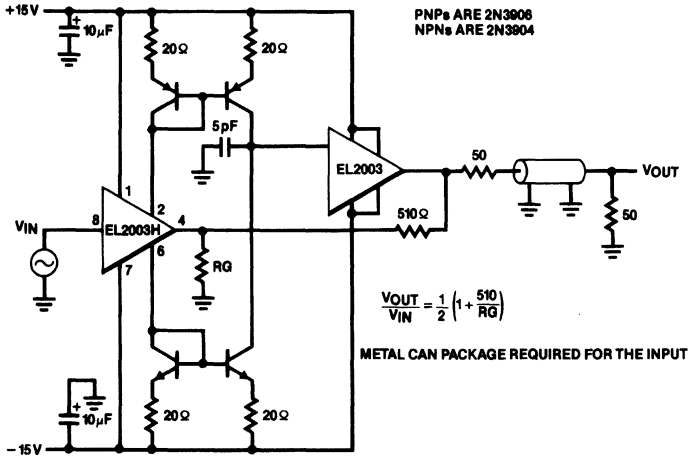
Simulated Inductor



2003-24

Typical Applications — Contd.

Turbo Amplifier, BW = 30 MHz for Gains from 1 to 5

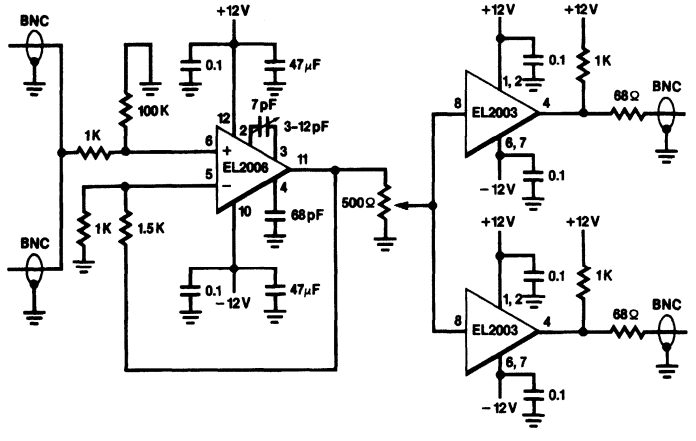


2003-25

Video Distribution Amplifier

In this broadcast quality circuit, the EL2006 FET input amplifier provides a very high input impedance so that it may be used with a wide variety of signal sources including video DACs, CCD cameras, video switches or 75Ω cables. The EL2006 provides a voltage gain of 2.5 while the potentiometer allows the overall gain to be adjusted to drive the standard signal levels into the back matched 75Ω cables. Back matching prevents multiple reflections in the event that the remote end of the cable is not properly terminated. The 1k pull up resistors reduce the differential gain error from 0.15% to less than 0.1%.

Video Distribution Amplifier

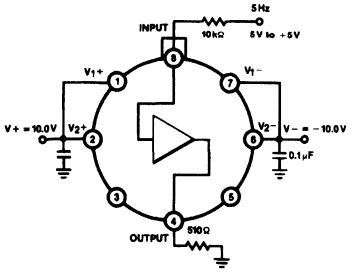


2003-26

EL2003C/EL2033C
100 MHz Video Line Driver

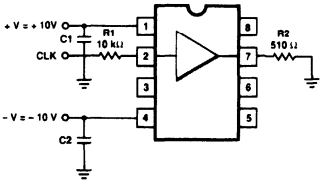
Burn-In Circuits

EL2003 Metal Can



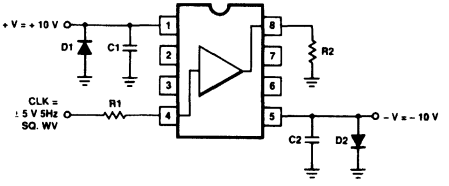
2003-27

EL2003 DIP



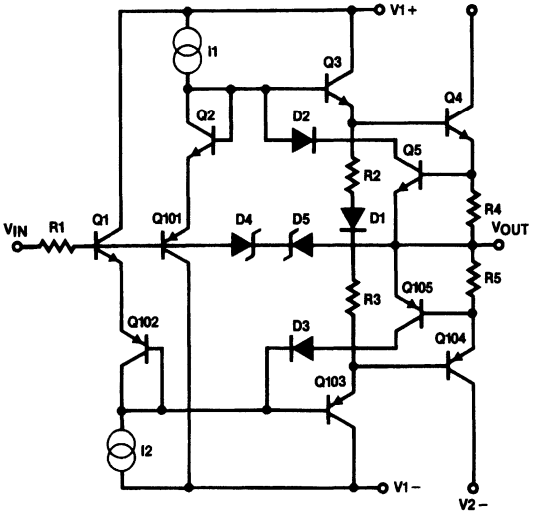
2003-28

EL2033 DIP



2003-29

Simplified Schematic

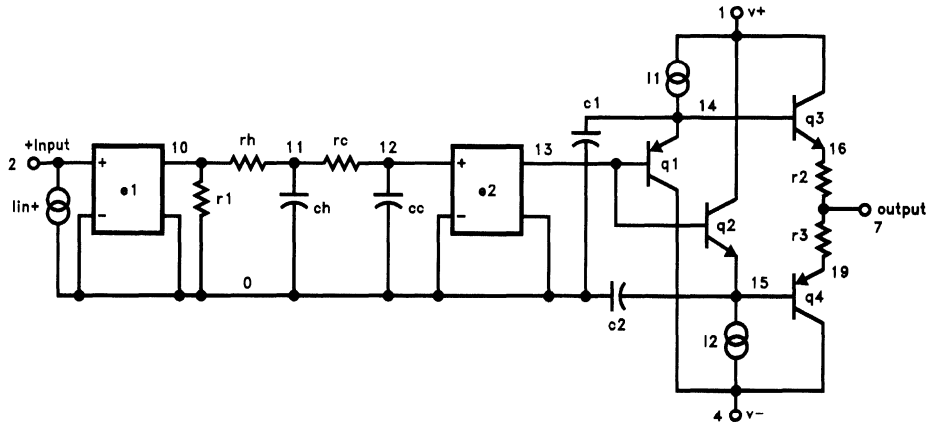


2003-30

EL2003 Macromodel

```
* Connections:      +input
*                   |     +Vsupply
*                   |     |     -Vsupply
*                   |     |     |     output
*                   |     |     |     |
.subckt M2003       2     1     4     7
* Input Stage
e1 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 10pF
rc 11 12 100
cc 12 0 3pF
e2 13 0 12 0 1.0
* Output Stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 5
r3 19 7 5
c1 14 0 3pF
c2 15 0 3pF
i1 1 14 3mA
i2 15 4 3mA
* Bias Current
iin+ 2 0 5uA
* Models
.model qn npn(is=5e-15 bf=150 rb=350 ptf=45 cjc=2pF tf=0.3nS)
.model qp pnp(is=5e-15 bf=150 rb=350 ptf=45 cjc=2pF tf=0.3nS)
.ends
```

EL2003 Macromodel — Contd.



2003-31

EL2008C
55 MHz 1 Amp Buffer Amplifier

Features

- High slew rate—2500 V/μs
- Wide bandwidth—
  100 MHz @ R_L = 50Ω
  55 MHz @ R_L = 10Ω
- Output current—1A continuous
- Output impedance—1Ω
- Quiescent current—13 mA
- Short circuit protected
- Power package with isolated metal tab

Applications

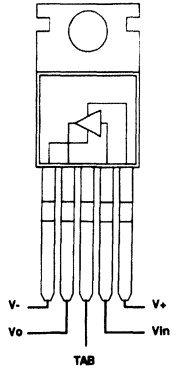
- Video distribution amplifier
- Fast op amp booster
- Flash converter driver
- Motor driver
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2008CT	0°C to +75°C	TO-220	MDP0028

Connection Diagram

5-Pin TO-220



2008-1

Top View

General Description

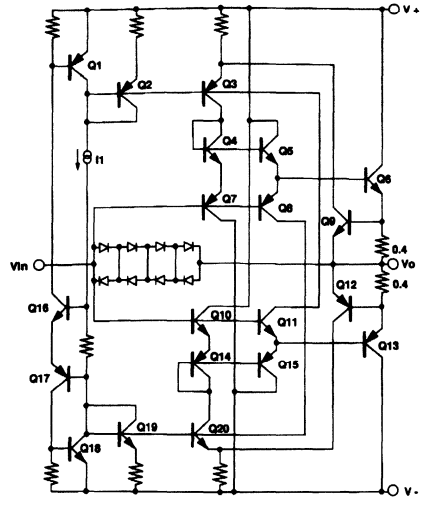
The EL2008 is a patented high speed bipolar monolithic buffer amplifier designed to provide currents over 1 amp at high frequencies, while drawing only 13 mA of quiescent supply current. The EL2008's 1500 V/μs slew rate and 55 MHz bandwidth driving a 10Ω load is second only to the EL2009 and insures stability in fast op amp feedback loops. Elantec has applied for patents on unique circuitry within the EL2008.

Used as an open loop buffer, the EL2008's low output impedance (1Ω) gives a gain of 0.99 when driving a 100Ω load and 0.9 driving a 10Ω load. The EL2008 has output short circuit current limiting which will protect the device under both a DC fault condition and AC operation with reactive loads.

The EL2008 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2008, the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages. Therefore the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2008CT is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Simplified Schematic



2008-2

Manufactured under U.S. Patent No. 4,833,424 and 4,827,223.

EL2008C
55 MHz 1 Amp Buffer Amplifier

Absolute Maximum Ratings (25°C)

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	0°C to +75°C
V_{IN}	Input Voltage (Note 1)	±15 or V_S	T_J	Operating Junction Temp	175°C
I_{IN}	Input Current (Note 1)	±50 mA	T_{ST}	Storage Temp Range	−65°C to +150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{LD}	Lead Solder Temp <10 seconds	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	25°C	−40	10	+40	I	mV
				T_{MIN}, T_{MAX}	−50		+50	IV	mV
I_{IN}	Input Current	0	∞	25°C	−35	−5	+35	I	μA
				T_{MIN}, T_{MAX}	−50		+50	IV	μA
R_{IN}	Input Impedance	±12V	100Ω	25°C	0.5	2		I	MΩ
A_{V1}	Voltage Gain	±10V	∞	25°C	0.985	0.9995		I	V/V
A_{V2}	Voltage Gain	±10V	10Ω	25°C	0.88	0.91		I	V/V
A_{V3}	Voltage Gain, V_S = ±15V	±3V	10Ω	25°C	0.87	0.89		I	V/V
V_{O1}	Output Voltage Swing	±14V	100Ω	25°C	±13			I	V
V_{O2}	Output Voltage Swing	±12V	10Ω	25°C	±10.5	±11		I	V
R_{O1}	Output Impedance	±10V	±10 mA	25°C		1.8	2.5	I	Ω
R_{O2}	Output Impedance	±10V	±1A	25°C		0.8	1.0	I	Ω
I_O	Output Current	±12V	(Note 3)	25°C	1.4	1.8		I	A
				T_{MIN}, T_{MAX}	1			IV	A
I_S	Supply Current	0	∞	25°C	9	13	22	I	mA
PSRR	Supply Rejection (Note 4)	0	∞	25°C	60			I	dB
V_S+, V_S-	Supply Sensitivity (Note 5)		∞	25°C			2	I	mV/V

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
SR_1	Slew Rate	$\pm 10V$	50Ω	25°C		2500		V	V/μs
	(Note 6)	$\pm 10V$	10Ω	25°C		1500		V	V/μs
SR_2	Slew Rate (Note 7)	$\pm 5V$	10Ω	25°C		800		V	V/μs
t_r, t_f	Rise/Fall Time	100 mV	10Ω	25°C		7		V	ns
BW	−3 dB Bandwidth	100 mV	10Ω	25°C		55		V	MHz
C_{IN}	Input Capacitance			25°C		25		V	pF
THD				25°C			1	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the application hints for information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V and −10V on the output.

Note 4: $V_S = \pm 4.5V$ then V_S is changed to ±18V.

Note 5: $V_S+ = +15V$, $V_S- = -4.5V$ then V_S- is changed to −18V and $V_S- = -15V$, $V_S+ = +4.5V$ then V_S+ is changed to +18V.

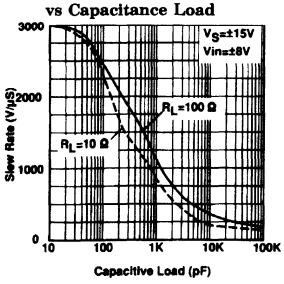
Note 6: Slew Rate is measured between $V_{OUT} = +5V$ and −5V.

Note 7: Slew Rate is measured between $V_{OUT} = +2.5V$ and −2.5V.

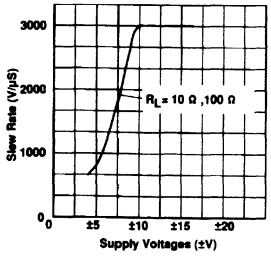
EL2008C
55 MHz 1 Amp Buffer Amplifier

Typical Performance Curves

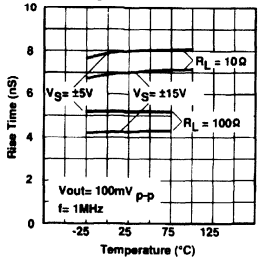
Slew Rate vs Capacitance Load



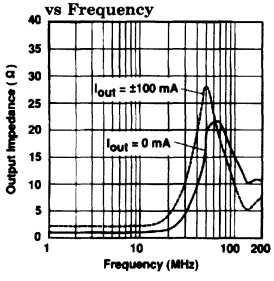
Slew Rate vs Supply Voltage



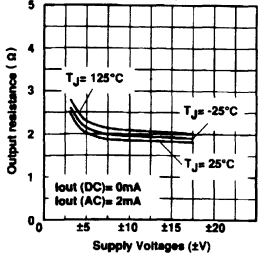
Rise Time vs Temperature



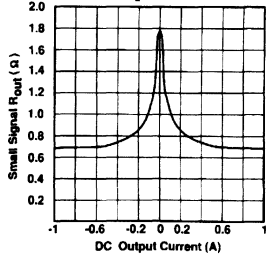
Output Impedance vs Frequency



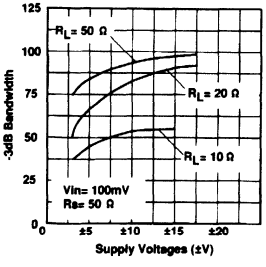
Output Resistance vs Supply Voltage



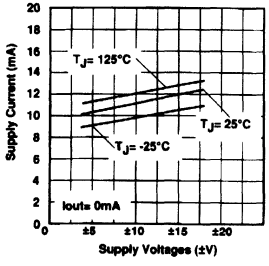
Small Signal Output Resistance vs DC Output Current



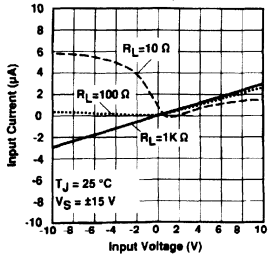
−3 dB Bandwidth vs Supply Voltage



Quiescent Supply Current vs Supply Voltage



Input Current vs Input Voltage



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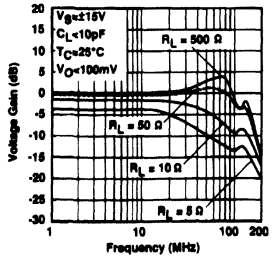
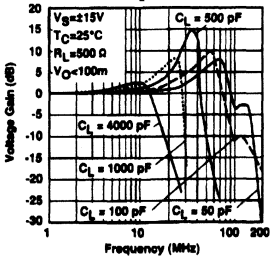
Typical Performance Curves — Contd.

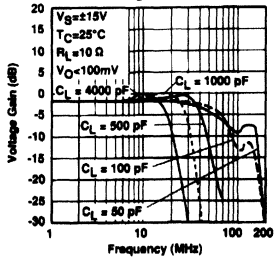
Voltage Gain vs Frequency at Various Resistive Loads



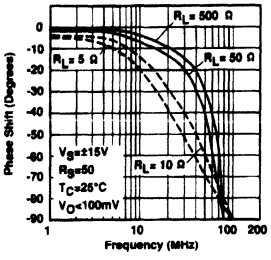
Voltage Gain vs Frequency at Various Capacitive Loads



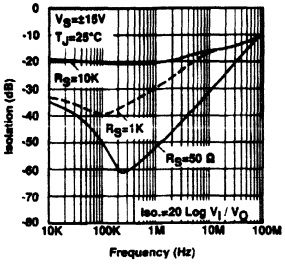
Voltage Gain vs Frequency at Various Capacitive Loads



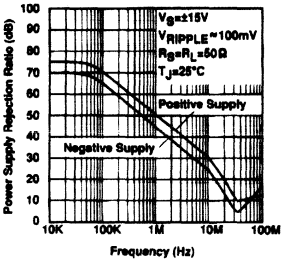
Phase Shift vs Frequency at Various Resistive Loads



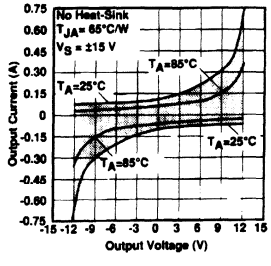
Reverse Isolation vs Frequency



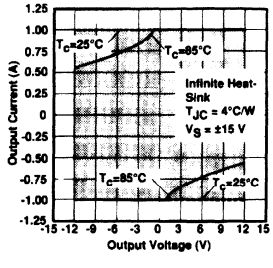
Power Supply Rejection Ratio vs Frequency



Active operating area.



Active operating area.



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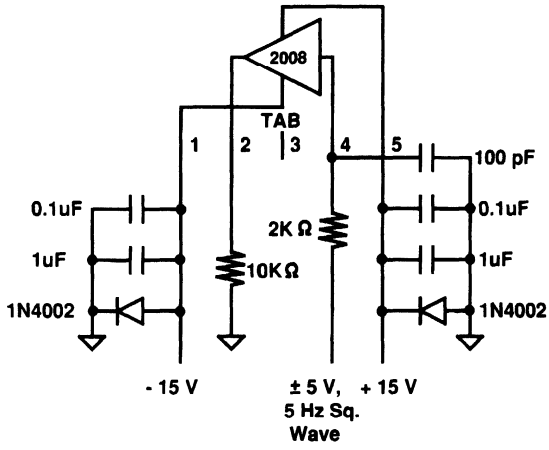
EL2008C
55 MHz 1 Amp Buffer Amplifier

Burn-In Circuit



Applications Information

The EL2008 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2008 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2008's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 3000 V/μs slew rates with 10Ω load possible with modest supply current.

Power Supplies

The EL2008 may be operated with single or split supplies with total voltage difference between 10V ($\pm$5V) and 36V ($\pm$18V). However, bandwidth, slew rate and output impedance are affected by total supply voltages below 20V ($\pm$10V) as shown by the characteristic curves. It is not necessary to use equal split value supplies. For example $-$5V and $+$12V would be excellent for signals from $-$2V to $+$9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum a 10 μF tantalum capacitor in parallel with a 0.1 μF capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2008 looks like a resistance in parallel with about 25 pF in addition to a DC bias current. The DC bias current is due to the mismatch in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range in some units. A few typical input current (I_{IN}) curves are shown in the characteristic curves.

Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about $\pm$2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. If the output of the EL2008 is accidentally shorted it is possible that some devices driving the EL2008's input could be damaged or destroyed driving the EL2008's load through the diodes while the EL2008 is unaffected. In such cases a resistor in series with the input of the EL2008 can limit the current.

Applications Information — Contd.

Source Impedance

The EL2008 has good input to output isolation. Open loop, capacitive and resistive sources up to 100 kΩ present no oscillation problem driving resistive loads as long as care is used in board layout to minimize output to input coupling and the supplies are properly bypassed. When driving capacitive loads in the 100 pF to 1000 pF region source resistances above 25Ω can cause peaking and oscillation. Such problems can be eliminated by placing a capacitor from the EL2008's input to ground. The value should be about ¼ the load capacitance. In a feedback loop there is a speed penalty and a possibility of oscillation when the EL2008 is driven with a source impedance of 200Ω or more. Significant phase shift can occur due to the EL2008's 25 pF input capacitance. Inductive sources can cause oscillations. A series resistor of a few hundred ohms to 1 kΩ will usually solve the problem.

Current Limit

The EL2008 has internal current limiting to protect the output transistors. The current limit is about 1.5A at room temperature and decreases with junction temperature. At 150°C junction temperature it is above 1A.

Heat Sinking

A suitable heat sink will be required for most applications. The thermal resistance junction to case for the TO-220 package is 4°C per watt. No voltage appears at the heat sink tab so no precautions need to be taken to avoid shorting the tab to a supply voltage or ground. As there is a small parasitic capacitance between the tab and the buffer circuitry, it is recommended that the tab be connected to AC ground (either supply voltage or DC ground). The center lead is internally connected to the tab so the connection can be made at the tab or the center lead.

Parallel Operation

If more than 1A is required or if heat management is a problem, several EL2008s may be paralleled together. The result is as through each device was driving only part of the load. For example, if two units are paralleled then a 5Ω load looks like 10Ω to each EL2008. Of course, parallel operation reduces both the input and output impedance and increases bias current. But there is no increase in offset voltage. Three units in parallel can drive a 3Ω load ±10V at 2500 V/μs. The output impedance will be about 0.33Ω.

Resistive Loads

The DC gain of the EL2008 is the product of the unloaded gain (0.999) and the voltage divider formed by the device output resistance and the load resistance.

$$A_V = 0.999^* (R_L/R_L + R_{OUT})$$

The high frequency response varies with the load resistance as shown by the characteristic curves. Both gain and phase are shown. If the 80 MHz peaking is undesireable when driving load resistors greater than 50Ω, an RC snubber circuit can be used from output to ground. The capacitive load section discusses snubber usage in more detail.

Capacitive Loads

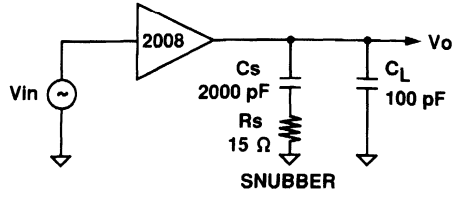
The EL2008 is not stable driving purely capacitive loads between 100 pF and 500 pF. Purely capacitive loads from 500 pF to 1000 pF will also have excessive peaking as shown in the characteristic curves. The squarewave response will have large overshoots and ring for hundreds of nanoseconds.

When driving capacitive loads, stability can be achieved and peaking and ringing can be mini-

EL2008C
55 MHz 1 Amp Buffer Amplifier

Applications Information — Contd.

mized either by adding a 50Ω (or less) load in parallel with the capacitive load or by an RC snubber circuit from output to ground. The snubber values can be found empirically by observing a squarewave or the frequency response. First just put a resistor alone from the output to ground until the desired response is achieved. The gain will be reduced due to the output resistance of the EL2008 and power consumption will be high. Then put a capacitor in series with the resistor to restore gain at low frequencies and eliminate the DC current. Start with a small capacitor and increase until the response is optimum. The figure below shows an example of an EL2008 driving a 100 pF load.



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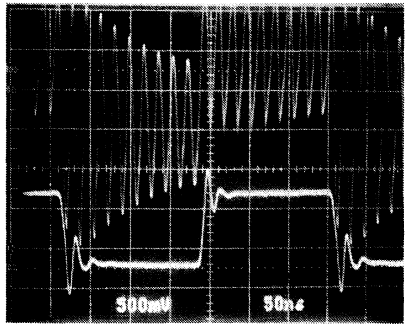

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Driving a pure capacitive load. Top trace is without a snubber. Bottom trace is with a snubber circuit.

Inductive Loads

The EL2008 with its 1A output current can drive small motors and other inductive loads. The EL2008's current limiting into inductive loads does NOT in and of itself cause spikes and kickbacks. However, if the EL2008 is in current limit and the input voltage is changing very quickly (i.e., a squarewave) the inductive load can kick the output beyond the supply voltages. Motors are also able to generate kickback voltages when the EL2008 is in current limit.

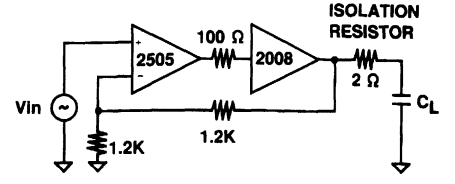
To prevent damage to the EL2008 when the output kicks beyond the supplies it is recommended that catch diodes be placed from each supply to the output.

Op Amp Booster

The EL2008 can boost the output drive of almost any monolithic op amp. If the phase shift in the EL2008 is low at the op amp's unity gain frequency, no additional frequency compensation is required. An op amp followed with the EL2008 can drive loads as low as 10Ω to ±10V.

Driving capacitive loads with any closed loop system creates special problems. The open loop output impedance works into the load capacitance to generate phase lag which can make the loop unstable. The EL2008 output impedance is less than 10Ω from DC to 30 MHz. But a capacitive load of 1000 pF will generate about 45 degrees of phase shift at 30 MHz. More capacitance will cause the problem at lower frequency.

With enough capacitance even slow op amps will become unstable. The simplest way to drive capacitive loads is to isolate them from the feedback with a series resistor. 1Ω to 5Ω is usually enough but the final value will depend on the op amp used and the range of load capacitance.



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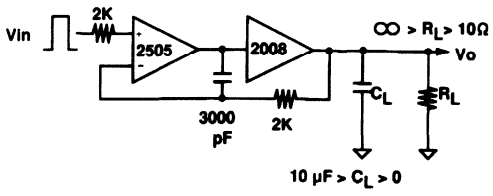
C_L		t_r		O.S.
13	pF	45	ns	20%
470	pF	50	ns	20%
1000	pF	55	ns	30%
3300	pF	60	ns	30%
0.1	µF	350	ns	0%
1	µF	4	µs	0%
5	µF	20	µs	0%

Applications Information — Contd.

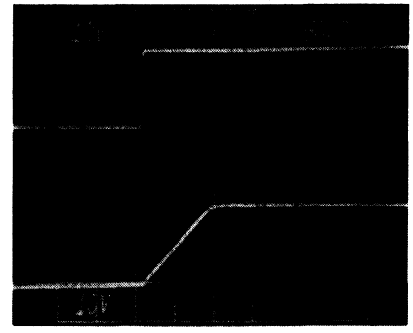
Unfortunately the isolation resistor is not inside the op amp feedback loop and cannot be neglected when computing the DC voltage gain into a resistive load. If load dependent DC gain is not tolerable then additional high frequency feedback from the op amp output (the EL2008 input) and an isolation resistor from the buffer output can be used to stabilize the loop. This configuration requires the op amp to be unity gain stable. This feedback method will allow the EL2008 to boost the output of the EHA2505 amplifier below and serve as a variable, bipolar 1A voltage supply with short circuit protection.



Slew Rate = $1A/C_L$

Video Distribution Amplifier

The EL2008 can drive 15 double matched 75Ω cables. If the EL2008 is used within an op amp feedback loop the output levels are independent of loading. The circuit below accepts 1 of 2 inputs and drives 15 cables. Pin 8 of the EL2020 (Disable) is used to multiplex between the inputs and can be easily expanded to accept more inputs. The circuit as shown when fully loaded has differential phase $<0.1°$ and differential gain $<0.1\%$. The 100Ω resistor at the EL2008 input (R1) is necessary to stabilize the loop. The 100Ω resistor at the EL2008 output (R2) to the −12V supply, insures that the EL2008 sources current even when the output voltage is at 0V. This is necessary to achieve the excellent differential gain and phase values. More information about driving cables can be found in the EL2003 data sheet. See the EL2020 data sheet to learn more about using it as a multiplexer.

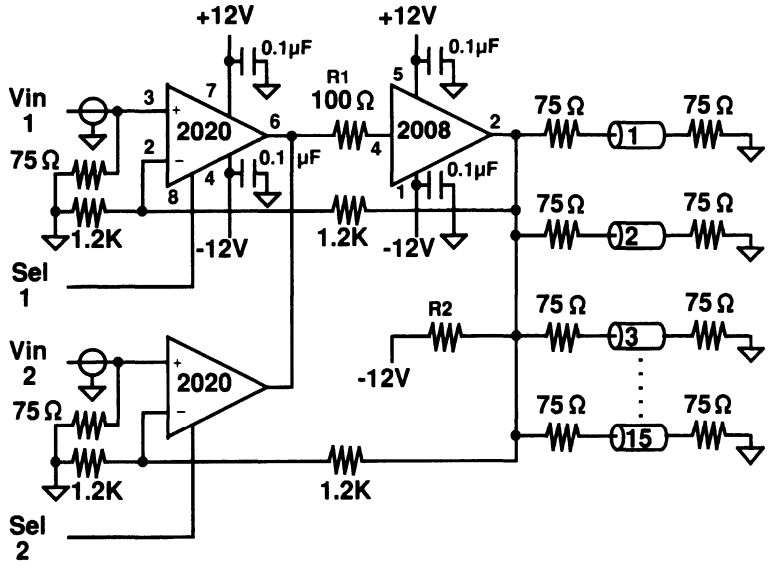


Input (top trace) and output (bottom trace) of EHA2505 op amp boosted by EL2008.

2

EL2008C
55 MHz 1 Amp Buffer Amplifier

Video Mux and Distribution Amplifier



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EL2008 Macromodel

```
* Connections:      +input
*                   |     +Vsupply
*                   |     |     -Vsupply
*                   |     |     |     output
*                   |     |     |     |
.subckt M2008       4     5     1     2
*
* Input Stage
*
e1 10 0 4 0 1.0
r1 10 0 1K
rh 10 11 1K
ch 11 0 2.65pF
rc 11 12 10K
cc 12 0 0.159pF
e2 13 0 12 0 1.0
*
* Output Stage
*
q1 1 13 14 qp
q2 5 13 15 qn
q3 5 14 16 qn 15
q4 1 15 19 qp 15
r2 16 2 0.4
r3 19 2 0.4
c1 14 0 0.6pF
c2 15 0 0.6pF
i1 5 14 1.2mA
i2 15 1 1.2mA
*
* Bias Current
*
iin+ 4 0 5µA
*
* Models
*
.model qn npn (is=5e-15 bf=1500)
.model qp pnp (is=5e-15 bf=1500)
.ends
```

EL2009C
90 MHz 1 Amp Buffer Amplifier

elantec HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Features

- High slew rate—3000 V/μs
- Wide bandwidth—
  125 MHz @ R_L = 50Ω
  90 MHz @ R_L = 10Ω
- Output current—1A continuous
- Output impedance—1Ω
- Short circuit protected
- Power package with isolated metal tab

Applications

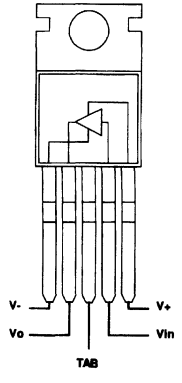
- Video distribution amplifier
- Fast op amp booster
- Flash converter driver
- Motor driver
- Pulse transformer driver
- A.T.E. pin driver

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2009CT	0°C to +75°C	TO-220	MDP0028

Connection Diagram

5-Pin TO-220



Top View

General Description

The EL2009 is a patented high speed bipolar monolithic buffer amplifier designed to provide currents over 1 amp at high frequencies, while drawing 40 mA of quiescent supply current. The EL2009's 3000 V/μs slew rate and 90 MHz bandwidth driving a 10Ω load insures stability in fast op amp feedback loops. Elantec has applied for patents on unique circuitry within the EL2009.

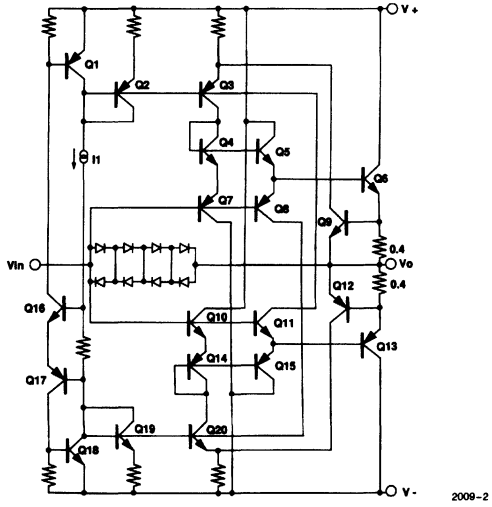
Used as an open loop buffer, the EL2009's low output impedance (1Ω) gives a gain of 0.99 when driving a 100Ω load and 0.9 driving a 10Ω load.

The EL2009 has an output short circuit current limit which will protect the device under both a DC fault condition and AC operation with reactive loads.

The EL2009 is constructed using Elantec's proprietary Complementary Bipolar process that produces PNP and NPN transistors with essentially identical AC and DC characteristics. In the EL2009, the Complementary Bipolar process also insulates the package's metal heat sink tab from all supply voltages. Therefore, the tab may be mounted to an external heat sink or the chassis without an insulator.

The EL2009CT is specified for operation over the 0°C to +75°C temperature range and is provided in a 5-lead TO-220 plastic power package.

Simplified Schematic



Manufactured under U.S. Patent No. 4,833,424 and 4,827,223.

EL2009C
90 MHz 1 Amp Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	0°C to +75°C
V_{IN}	Input Voltage (Note 1)	±15V or V_S	T_J	Operating Junction Temp.	175°C
I_{IN}	Input Current (Note 1)	±50 mA	T_{ST}	Storage Temp. Range	−65°C to +150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{LD}	Lead Solder Temp. <10 seconds	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_{OS}	Output Offset Voltage	0	∞	25°C	−60		60	I	mV
				T_{MIN}, T_{MAX}	−80		80	IV	mV
I_{IN}	Input Current	0	∞	25°C	−125	−5	125	I	µA
				T_{MIN}, T_{MAX}	−200		200	IV	µA
R_{IN}	Input Impedance	±12V	100Ω	25°C	250	900		I	kΩ
A_{V1}	Voltage Gain	±10V	∞	25°C	0.985	0.999		I	V/V
A_{V2}	Voltage Gain	±10V	10Ω	25°C	0.88	0.90		I	V/V
A_{V3}	Voltage Gain, V_S = ±5V	±3V	10Ω	25°C	0.87	0.89		I	V/V
V_{O1}	Output Voltage Swing	±14V	100Ω	25°C	±13			I	V
V_{O2}	Output Voltage Swing	±12V	10Ω	25°C	±10.5	±11		I	V
R_{O1}	Output Impedance	±10V	±10 mA	25°C			1.5	I	Ω
R_{O2}	Output Impedance	±10V	±1A	25°C		0.9	1.0	I	Ω
I_O	Output Current	±12V	(Note 3)	25°C	1.4	1.8		I	A
				T_{MIN}, T_{MAX}	1			IV	A
I_S	Supply Current	0	∞	25°C	30	45	65	I	mA
PSRR	Supply Rejection (Note 4)	0	∞	25°C	60			I	dB

EL2009C
90 MHz 1 Amp Buffer Amplifier

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			Test Level	Units
		V_{IN}	Load	Temp	Min	Typ	Max		
V_S+, V_S-	Supply Sensitivity (Note 5)		∞	25°C			2	I	mV/V
SR_1	Slew Rate (Note 6)	±10V	50Ω 10Ω	25°C		3000 2500		V	V/μs
SR_2	Slew Rate (Note 7)	±5V	10Ω	25°C		1250		V	V/μs
t_r, t_f	Rise/Fall Time	100 mV	10Ω	25°C		7		V	ns
BW	−3 dB Bandwidth	100 mV	10Ω	25°C		90		V	MHz
C_{IN}	Input Capacitance			25°C		25		V	pF
THD	Total Harmonic Distortion			25°C			1	I	%

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input voltage exceeds ±7.5V then the input current must be limited to ±50 mA.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12V input and −10V on the output.

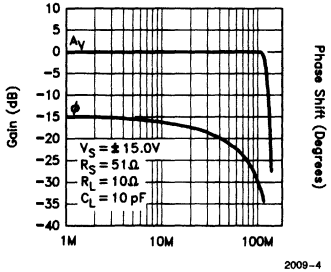
Note 4: $V_S = \pm 4.5V$ then V_S is changed to ±18V.

Note 5: $V_S+ = +15V$, $V_S- = 4.5V$ then V_S- is changed to −18V and $V_S- = -15V$, $V_S+ = +4.5V$ then V_S+ is changed to +18V.

Note 6: Slew Rate is measured between $V_{OUT} = +5V$ and −5V.

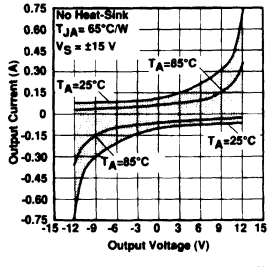
Note 7: Slew Rate is measured between $V_{OUT} = +2.5V$ and −2.5V.

Voltage Gain and Phase vs Frequency



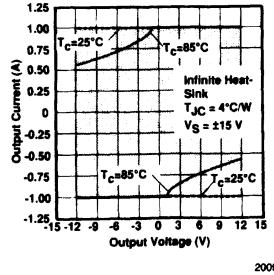
2009-4

Active operating area



2009-5

Active operating area



2009-6

Applications Information

The EL2009 is a higher bandwidth of the EL2008. It is recommended that you read the EL2008 application section.

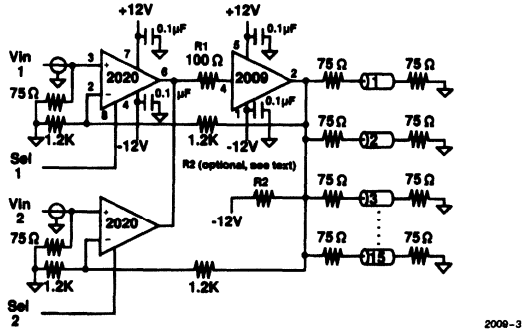
Video Distribution Amplifier

The EL2009 can drive 15 double matched 75Ω cables. If the EL2009 is used within an op amp feedback loop the output levels are independent of loading. The circuit below accepts 1 of 2 inputs and drives 15 cables. Pin 8 of the EL2020 (Disable) is used to multiplex between the inputs and can be easily expanded to accept more inputs. The circuit as shown when fully loaded has differential phase <0.1° and differential gain <0.1%. The 100Ω resistor at the EL2009 input (R1) is necessary to stabilize the loop. The EL2009 operates with a CLASS AB output which exhibits a slight rise in output impedance when-

Applications Information — Contd.

ever the current it sources into the load approaches zero. In those cases, where differential gain and phase are measurably affected, resistor R2 may be added to ensure that the EL2009 output current never reaches zero. This will result in a CLASS A output stage with active pulldown but with the penalty of power dissipation in R2. More information about driving cables can be found in the EL2003 data sheet.

Video Mux and Distribution Amp.



EL2009 Macromodel

```
* Connections:      +input
*                   |     +Vsupply
*                   |     |     -Vsupply
*                   |     |     |     output
*                   |     |     |     |
.subckt M2009       4     5     1     2
*
* Input Stage
*
e1 10 0 4 0 1.0
r1 10 0 1K
rh 10 11 1K
ch 11 0 1pF
rc 11 12 6.3K
cc 12 0 0.159pF
e2 13 0 12 0 1.0
*
* Output Stage
*
q1 1 13 14 qp
q2 5 13 15 qn
q3 5 14 16 qn 10
q4 1 15 19 qp 10
r2 16 2 0.2
r3 19 2 0.2
c1 14 0 1.7pF
c1 15 0 1.7pF
i1 5 14 5mA
i2 15 1 5mA
*
* Bias Current
*
iin+ 4 0 5μA
*
* Models
*
.model qn npn (is=5e-15 bf=500)
.model qp pnp (is=5e-15 bf=500)
*
.ends
```

EL2031C
550 MHz Buffer Amplifier

Features

- Wide bandwidth—550 MHz
- High slew rate—7000 V/μs
- Low quiescent power
- FET input
- 100 mA peak output current

Applications

- Current booster
- Cable/line driver for high resolution graphics
- Flash A/D input buffer
- Isolation buffer
- A.T.E. pin driver

Ordering Information

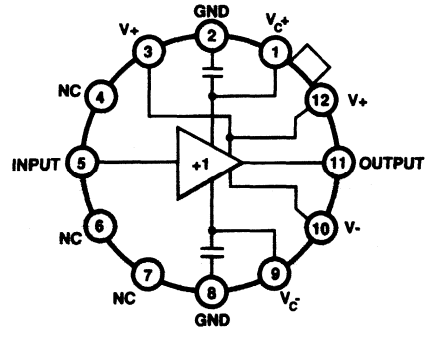
Part No.	Temp. Range	Pkg.	Outline #
EL2031CG	0°C to +70°C	TO-8	MDP0026

General Description

The EL2031C is an extremely high speed hybrid buffer amplifier which can drive 100Ω loads at frequencies from DC to 550 MHz and with large signal slew rates greater than ±8000 V/μs. The FET input insures minimal loading of the input signal and optimum transient performance. It can output peak currents of ±100 mA. To minimize power supply coupling effects, 0.015 μF supply bypass capacitors are included inside the EL2031C.

These extremely high speed buffers may be used in a broad range of analog or digital applications requiring extremely fast, high current outputs. Examples include high resolution graphics terminal R-G-B line drivers, ATE pin drivers or pin receiver buffers, flash A/D converter input buffers, and oscilloscope input stages. The pinout is similar to earlier generation EL2004 and ELH0033 buffers.

Connection Diagram



Top View

EL2031C
550 MHz Buffer Amplifier

Absolute Maximum Ratings (T_A = 25°C)

(V+) - (V−)	Supply Voltage	−0.3V to +25V	I_{OUT}	Output current (Continuous)	±70 mA
(V_C+) - (V_C−)	Output Device Collector Supplies	−0.3V to +25V		(Peak)	±100 mA
(V+) - (V_C+) or (V_C−) - (V−)			(V_C+) - Gnd or (V_C−) - Gnd		
	Supply Differential	−0.3V to +25V		Output device supply to gnd	±50V
(V+) - (V_{IN}) or (V_{IN}) - (V−)			T_J	Operating Junction Temperature	175°C
	Input Range	17.5V	T_A	Operating Temperature Range	0°C to +70°C
I_{IN}	Input (fault) Current	±20 mA	T_{ST}	Storage Temperature Range	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V+ = V_C+ = 10V, V− = V_C− = −10V, R_S = 50Ω

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_{OS}	Offset Voltage	V_{IN} = 0, T_A = 25°C		3	10	I	mV
		T_{MIN}, T_{MAX}			20	III	mV
I_B	Input Bias Current	V_{IN} = 0, 5V, T_A = 25°C, T_{MIN}, T_{MAX}			10	II	nA
		V_{IN} = 5V, T_A = 25°C, T_{MIN}, T_{MAX}			1	II	µA
R_{IN}	Input Impedance	V_{IN} = ±1V, T_A = 25°C, T_{MIN}, T_{MAX}		4000		V	MΩ
V_O	Output Voltage Swing	V_{IN} = ±7.5V, T_A = 25°C, T_{MIN}, T_{MAX}					
		No Load,	±6.6	±7.2		II	V
		R_L = 100Ω	±6.0	±6.8		II	V
A_V	Voltage Gain	V_{IN} = ±5V, T_A = 25°C, T_{MIN}, T_{MAX}					
		No Load,	0.96	0.985	1.0	II	V/V
		R_L = 100Ω	0.86	0.93	0.96	II	V/V
R_O	Output Impedance	V_{IN} = ±5V, I_L = 0 mA to 50 mA	3	6	11	II	Ω
		T_A = 25°C, T_{MIN}, T_{MAX}					
I_S	Total Supply Current	V_{IN} = 0, T_A = 25°C, T_{MIN}, T_{MAX}		22	26	II	mA

DC Electrical Characteristics $V+ = V_C+ = 10V, V- = V_C- = -10V, R_S = 50\Omega$ — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
PSRR	Power Supply Rejection	$V_{IN} = 0, T_A = 25°C$ (Note 1)		61		V	dB
V_S+	Sensitivity	$V_{IN} = 0, T_A = 25°C, V- = V_C- = -10V$ and $V+ = V_C+$ from +5V to +12V		7	25	I	mV/V
V_S-	Sensitivity	$V_{IN} = 0, T_A = 25°C, V+ = V_C+ = 10V$ and $V- = V_C-$ from −5V to −12V		9	25	I	mV/V

AC Electrical Characteristics (Note 2) $V+ = V_C+ = 10V, V- = V_C- = -10V, R_S = 50\Omega, T_A = 25°C$

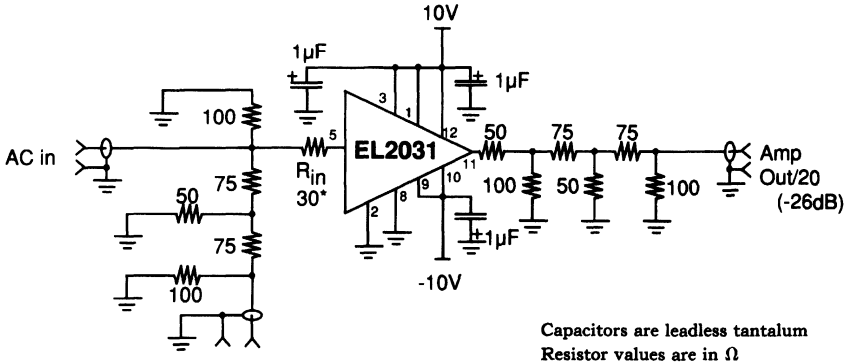
Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
t_r	Rise Time	$V_{IN} = -0.5V$ to 0.5V, $R_L = 100\Omega$ 10% to 90%		650	1000	I	ps
t_f	Fall Time	$V_{IN} = 0.5V$ to −0.5V, $R_L = 100\Omega$, 10% to 90%		650	1000	I	ps
t_{pd}	Propagation Delay	$V_{IN} = -0.5$ to 0.5V or 0.5V to −0.5V, $R_L = 100\Omega$, 10% of V_{IN} to 10% of V_{OUT}		500		V	ps
t_{rl}	Large Signal Rise Time	$V_{IN} = -5V$ to 5V, $R_L = 100\Omega$, 10% to 90%		650		V	ps
t_{fl}	Large Signal Fall Time	$V_{IN} = -5V$ to 5V, $R_L = 100\Omega$, 10% to 90%		1200		V	ps
SR+	Positive Slew-rate	$V_{IN} = -5V$ to 5V, $R_L = 100\Omega$, 25% to 75%	5000	10000		I	V/μs
SR−	Negative Slew-rate	$V_{IN} = 5V$ to −5V, $R_L = 100\Omega$, 25% to 75%	−5000	−7000		I	V/μs
BW	−3 dB Bandwidth	$V_{IN} = 1 V_{p-p}, R_L = 100\Omega$		550		V	MHz
	Gain Peaking	$V_{IN} = 1 V_{p-p}, R_L = 100\Omega$, 0.5 MHz to 500 MHz		0.5		V	dB
	Group Delay	$V_{IN} = 1 V_{p-p}, R_L = 100\Omega$ 5 MHz to 125 MHz		0.5		V	ns
	Phase Linearity	$V_{IN} = 1 V_{p-p}, R_L = 100\Omega$ 5 MHz to 125 MHz		1.0		V	°
A_V	Voltage Gain	$V_{IN} = 1 V_{p-p}, R_L = 100\Omega$, 10 MHz		0.94		V	V/V
Z_{OUT}	Output Impedance	$V_{IN} = 1 V_{p-p}$, 10 MHz		6		V	Ω
C_{IN}	Input Capacitance	10 MHz		3		V	pF

Note 1: PSRR tests are performed with $V+ = V_C+$ and $V- = V_C-$. The supplies are simultaneously changed from ±5V to ±12V.

Note 2: AC tests are done using an Avtech AVMP−3-C pulse generator and a Tektronics 11402 digitizing oscilloscope with an 11A71, 1 GHz plug-in. The device under test has 50Ω input termination, 100Ω output load, and a Tektronics P66501, 750 MHz probe buffers the output for cabling to the oscilloscope. The system rise time is removed from all device reading.

EL2031C
550 MHz Buffer Amplifier

AC Test Fixture



Capacitors are leadless tantalum
Resistor values are in Ω

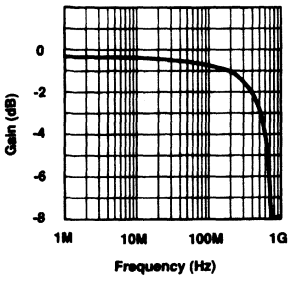
*R_{IN} = 30Ω for small signal AC
R_{IN} = 0 for transient signal tests

2031-2

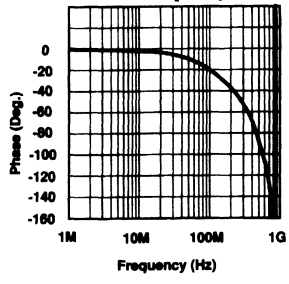
Reference out
= (V_{inDUT})/10
(−20 dB)

Typical Performance Curves

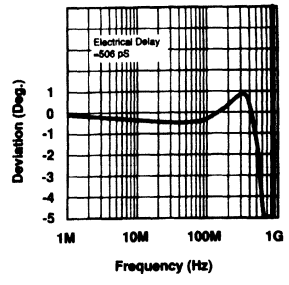
Gain vs Frequency



Phase vs Frequency

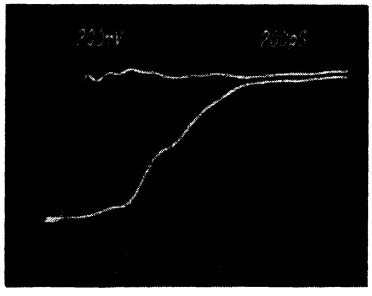


Deviation from Linear Phase



2031-3

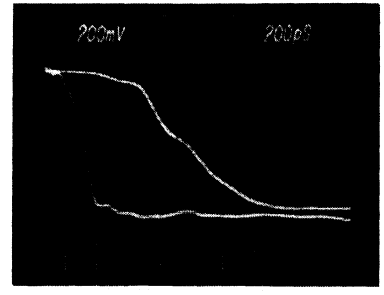
Small Signal Response



200 mV/cm vertical, 200 ps/cm horizontal
R_L = 100Ω, R_S = 50Ω, V_S = ±10V

2031-4

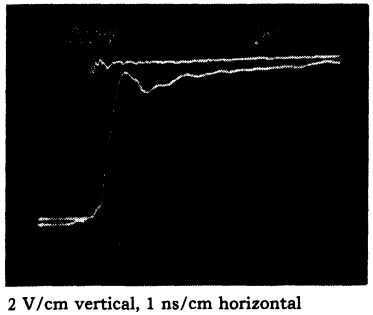
Small Signal Response



200 mV/cm vertical, 200 ps/cm horizontal
R_L = 100Ω, R_S = 50Ω, V_S = ±10V

2031-5

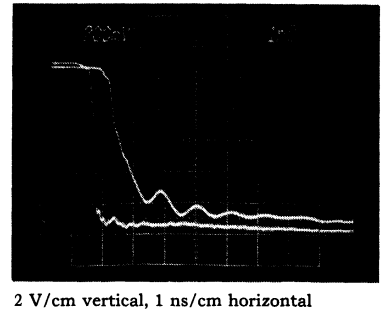
Large Signal Response



2 V/cm vertical, 1 ns/cm horizontal
R_L = 100Ω, R_S = 50Ω, V_S = ±10V

2031-6

Large Signal Response

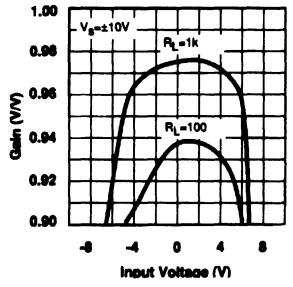


2 V/cm vertical, 1 ns/cm horizontal
R_L = 100Ω, R_S = 50Ω, V_S = ±10V

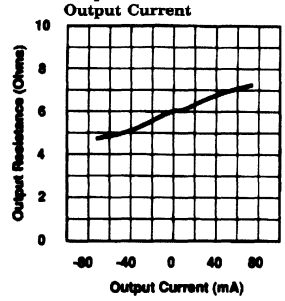
2031-7

Typical Performance Curves — Contd.

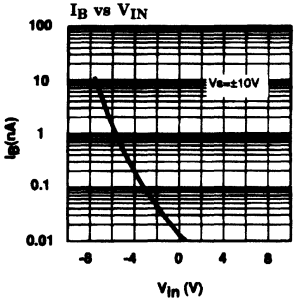
Gain vs Input Voltage



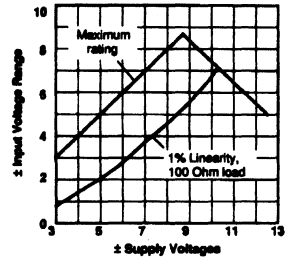
Output Resistance vs Output Current



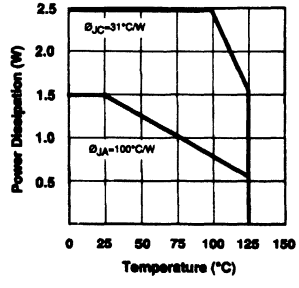
I_B vs V_{IN}



Input Range vs Supply Voltage



Maximum Power Dissipation



2031-8

Application Information

The EL2031 is a very pure buffer amplifier—a wire with good reverse isolation, so to speak, and as such is very easy to use. Obtaining its ultimate performance, though, requires attention to operating limits and construction details.

Operating Voltages

The transistors used within the EL2031 have f_t's of several GHz, and are consequently limited in voltage range. As seen in the absolute rating table, the input voltage is restricted to within 17.5V of any supply rail. Thus, if the supplies are ±10V the input must not exceed ±7.5V. With the highest supplies allowed (±12.5V), the input is restricted to ±5V.

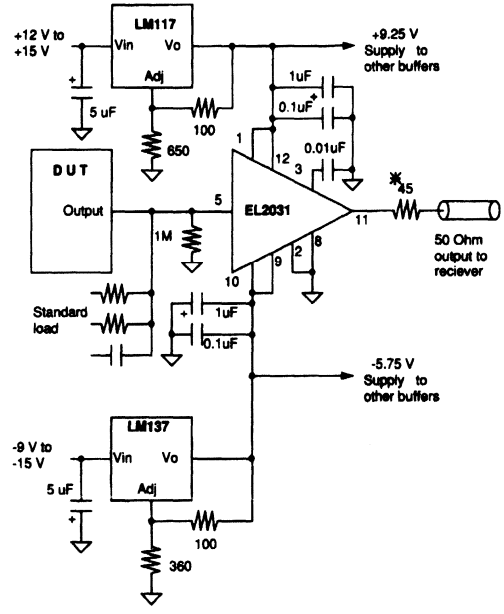
A practical approach might be to supply the power to the EL2031 via two inexpensive 3-terminal adjustable voltage regulators. The Input Voltage Range versus Supply Voltage curve shows the maximum supply and input voltage range along with the input range that does not exceed 1% linearity error wih a 100Ω load.

Design Example: Buffering Logic Outputs in an Automatic IC Test System

The output of logic circuits can range from a −2V low ECL level to a +5V high CMOS level. It would be desirable to buffer the output pin from the 50Ω transmission system so that the test-head electronics need not be packed with pin receivers and switches to route signal locally.

The 1% linear input range of the EL2031 should be set to at least −2.5V to +6V, or an 8.5V span. If this span was based symmetrically around ground, it would require supplies that support ±4.25V swings with 1% linearity. Referring to the Input Voltage Range versus Supply Voltage curve, we would need at least ±7.5V supplies. Offsetting the supplies to match the input range offset, we arrive at +9.25V and −5.75V supplies.

Figure 1 shows a practical ATE interface. Note the 1 MΩ resistor at the input of the EL2031, providing a known input level to the buffer in the absence of a device or standard load being connected. A second benefit from the buffer driving a 50Ω environment is that the full logic swing is halved before being monitored by the comparators in the measuring system, and their input range is not exceeded.



*45Ω + 5Ω output impedance of EL2031 matches 50Ω load.

Figure 1. EL2031 is Pin Buffer for an IC Test System

Circuit and Construction Techniques

In any circuit that operates above 100 MHz, parasitic capacitance and inductance will limit AC performance. Although the EL2031 is quite stable with source resistance as high as 500Ω, only 64 MHz of −3 dB bandwidth would be possible with a practical 5 pF circuit and parasitic input capacitance. Generally, all signals should be kept in a 50Ω environment to preserve bandwidth. Given such a 50Ω system (presenting a 25Ω source if doubly terminated), even 12 pF of stray capacitance can be tolerated while preserving the 550 MHz bandwidth of the EL2031.

EL2031C
550 MHz Buffer Amplifier

Application Information — Contd.

Parasitic inductance is perhaps more of a problem than capacitance at these frequencies. An inch of straight #34 wire has an inductance of 50 nH. This apparently small inductance has a reactance of 173Ω at 550 MHz! Clearly, signals should be connected with traces shorter than ¼ inch (6 mm) wherever possible. Use low inductance leadless resistors and capacitors in the signal path.

To ease the power supply decoupling, two 0.015 μF capacitors are mounted inside the EL2031. External high frequency capacitors (0.1 μF in parallel with 1 μF), should be connected from the power supply pins of the buffer to the ground plain (See Figure 1), as close to the buffer as possible. A solid ground plane and stripline layout techniques will help realize the potential performance of the buffer. The ground plane below the strip intercepts and diminishes magnetic fields from the wire, greatly reducing its inductance. In general, a ground plane should always be used with the EL2031. It is better to have only one plane, the one on the opposite side of the signal interconnect, as the return of bypass and signal components. A second ground plane will not be at the same "ground" potential as the first ground plane, and the pulse quality and frequency flatness of the circuit will be compromised. Finally, gold plating reduces skin effect resistances of all circuit traces and improves AC performance.

A socket will add parasitic inductance and magnetic coupling, degrading AC characteristics. The EL2031 comes with short ¼" leads, but it is still better to mount the device as close to the circuit board as possible. Pin sockets are a good compromise.

The case is unconnected, but less ringing from pulses will result from grounding the case. Just where on the circuit board ground should be connected is found experimentally. A small degradation in speed results from grounding the case. For extended temperature operation, a Thermalloy 2240A (33°C/W), Wakefield 215CB (30°C/W) or IERC 848CB (15°C/W) heat sink can be used to reduce the nominal 100°C/W case to ambient thermal resistance.

Pinout Consideration

The pinout of the EL2031 is similar to that of the EL2004 and ELH0033 buffers, except that the Offset Adjust pins 6 and 7 are not brought out, to maintain the frequency response of the device. Pin 2 and 8 are being used in the EL2031 package as a ground return for the internal bypass capacitors and should be tied to the ground plane as close to the package as possible. V+ appears on both pin 3 and pin 12.

Short Circuit Protection

As stated before, the transistors within the EL2031 are fairly delicate and can only output 100 mA peak. Short-circuit protection circuitry inevitably would have slowed the performance of the device, and was not included.

The traditional use of resistors in series with the power supply lines limits the short-circuit (see the application section of the EL2004 buffer) but does not allow a full loaded output swing. Restricting the input voltage range allows the resistors to be a higher value while allowing adequate loaded swing. Back-termination (a 50Ω source working into an unterminated load) maximizes the swing with higher valued resistors.

Finally, a series 50Ω output resistor will help reduce the short-circuit current. Note that if the output of the buffer is shorted and a positive input applied to the input, input current will rise if the output transistor saturates against the supply line resistor. Maximum input as well as output currents must be observed.

Example: A worst case short-circuit and some remedies

Figure 2 shows a simplified schematic of the EL2031. For the worst short circuit situation, let V+ and V− be ±10V, R_{SC} = 0, R_S = 0, R_O = 0 and V_{IN} = +7.5V.

When the output is shorted, large and uncontrolled currents flow through Q2's collector and emitter. Uncontrolled currents also flow through Q1's gate and source and Q2's base, since Q1's gate is now forward biased. The input current maximum rating is also violated. Actually, even normal operation can violate the maximum

Application Information — Contd.

current ratings of the part. If the input is a realistic 5V level, the output current will be almost 100 mA, not sustainable continuously.

Setting R_O to 50Ω will halve the output current to safe levels and provide better impedance match to the 50Ω cable and load, although the voltage gain is reduced to ½.

We can set R_{SC} to 140Ω in an attempt to limit Q2's collector current. With R_O = 0 and an output short to ground, Q2 will saturate with a collector current of about 70 mA. This will again cause large input currents to flow from V_{IN} if R_S is small. With the output shorted, the input voltage (at the maximum 20 mA of input current) will be about 1.8V. To tolerate an input of +5V, set R_S to 160Ω. To preserve frequency response, R_S should be paralleled with a 100 pF to 1000 pF capacitor. This approach will save the buffer from shorts, but it can only output 2.5V before Q2 or Q3 saturates.

At this point the values need to be refined. The Idss of Q1 is added to the 20 mA of input current and sent to the output. Thus, there is a total output current of 110 mA into a short. We can revise the value of R_S to 300Ω and R_{SC} to 250Ω to reduce currents. The maximum output swing is now diminished to 1.5V.

Another approach is to set R_O to 50Ω. Now an output short leaves 50Ω at the EL2031 output to ground rather than 0Ω. The 70 mA maximum output current sets 3.5V at the buffer output and V_{IN} may rise to about 5.3V before an input R_S is needed to limit input current. At V_{IN} = 5V, no input current flows, so only Idss adds to the output. R_{SC} is set to 130Ω (10V supply minus the 3.5V output, since Q2 is saturated, all divided by 70 mA minus the 20 mA Idss). Thus a 3.5V maximum output can be generated, or 1.7V at the load.

Clearly, not shorting the device output will obviate the need for R_S and R_{SC} and allow maximum output swing. When buffers are mounted on a board and are physically protected from shorts, no electrical protection should be needed.

Obtaining Optimum Frequency Responses

The EL2031, like all other amplifiers, has an input impedance that changes with frequency. At 750 MHz, the input impedance falls to about 15Ω, and has a negative real component. This means that a very fast input edge will cause a transient response at the input of the device, although this is not observed at the EL2031 output. A one to two dB peak can be seen in the frequency response curve at about 480 MHz as well, and it is affected by input wire inductance and source resistance and capacitance. A 30Ω resistor in series with the input will "de-Q" the EL2031 and provide the extremely well-behaved responses shown in the Bode and phase linearity plots.

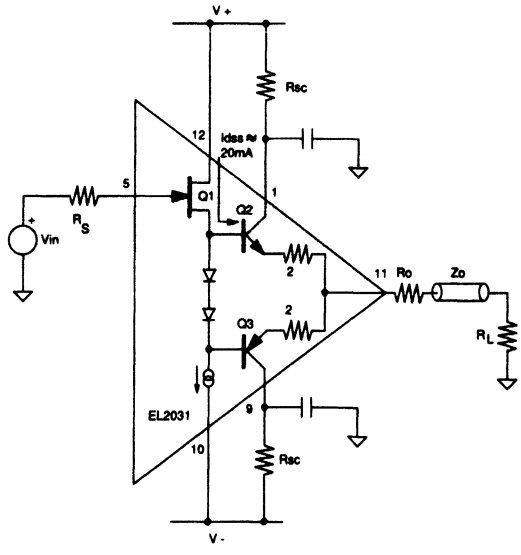
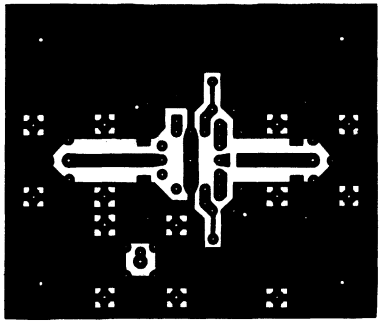


Figure 2. Simplified EL2031 Buffer Schematic

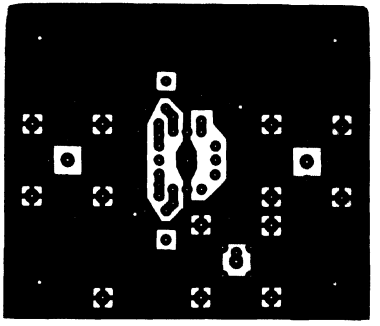
EL2031C
550 MHz Buffer Amplifier

Component Side



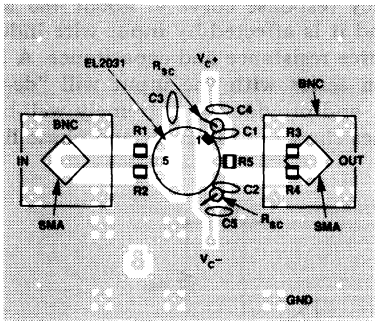
2031-11

Connector Side



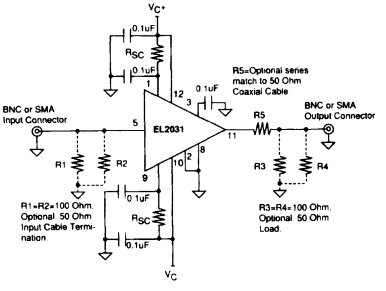
2031-13

Assembly Drawing



2031-12

PCB Schematic



2031-14

Suggested PC Board Layout

The EL2031 is a very fast buffer amplifier. Obtaining its ultimate performance requires attention to construction details. The PC board shown above was used to test and characterize the EL2031. It contains an extensive ground plane, parasitic capacitance and inductance are kept to a minimum by keeping the traces short and SMD low inductance leadless resistors were being used in the signal path and placed close to the EL2031.

Two 0.015 μF decoupling capacitors are mounted inside the EL2031. The PC board has provisions for five external high frequency 0.1 μF capacitors connected from the power supply pins of the buffer to the ground plane as close to the buffer as possible. Note that the capacitors can be mounted on the connector side.

The PC board has room for optional resistors:

R1 & R2: 100Ω resistors forming 50Ω termination of the input coaxial cable.

R3 & R4: 100Ω resistors forming a 50Ω load for the buffer.

R5: Series match for the output 50Ω coaxial cable.

R_{SC}: Short-circuit current limiting resistors.

Remember to insert a jumper if the R_{SC} resistors or R5 are not being used. Note that one of the ground pins in the SMA Coaxial connectors needs to be clipped to fit in the PCB. Mount the SMA or BNC connectors on the connector side so as not to interfere with R3 and R4.

Features

- 730 MHz −3 dB bandwidth (0.5 V_{PP})
- 5 ns settling to 0.2%
- V_S = ±5V @ 15 mA
- Low distortion: HD2, HD3 of −65 dBc at 20 MHz
- Overload/short-circuit protected
- Closed-loop, unity gain
- Low cost
- Direct replacement for CLC110

Applications

- Video buffer
- Video distribution
- HDTV buffer
- High-speed A/D buffer
- Photodiode, CCD preamps
- IF processors
- High-speed communications

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2072CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL2072CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL2072 is a wide bandwidth, fast settling monolithic buffer built using an advanced complementary bipolar process. This buffer is closed loop to achieve lower output impedance and higher gain accuracy. Designed for closed-loop unity gain, the EL2072 has a 730 MHz −3 dB bandwidth and 5 ns settling to 0.2% while consuming only 15 mA of supply current.

The EL2072 is an obvious high-performance solution for video distribution and line-driving applications. With low 15 mA supply current and a 70 mA output drive, performance in these areas is assured.

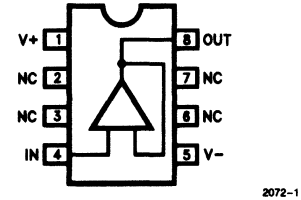
The EL2072's settling to 0.2% in 5 ns, low distortion, and ability to drive capacitive loads make it an ideal flash A/D driver. The wide 730 MHz bandwidth and extremely linear phase allow unmatched signal fidelity.

The EL2072 can be used inside an amplifier loop or PLL as its wide bandwidth and fast rise time have minimal effect on loop dynamics.

Elantec products and facilities comply with MIL-I-45028A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document *QRA-1: Elantec's Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



Top View

EL2072C
730 MHz Closed Loop Buffer

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Input Voltage	$\pm V_S$
Operating Temperature	−40°C to +85°C

Lead Temperature	
DIP Package	300°C
(Soldering: <5 Seconds −CN; <10 Seconds −J)	
SO Package	
Vapor Phase (60 Seconds)	215°C
Infrared (15 Seconds)	220°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C
Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 175°C/W SO

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Output Offset Voltage		25°C		2.0	8.0	I	mV
			T_{MIN}			16.0	III	mV
			T_{MAX}			13.0	III	mV
TCV_{OS}	Average Offset Voltage Drift		25°C − T_{MAX}		20.0	50.0	IV	µV/°C
			25°C − T_{MIN}		20.0	100.0		
I_B	Input Bias Current		25°C, T_{MAX}		10.0	50.0	II	µA
			T_{MIN}			100.0	III	µA
TCI_B	Average Input Bias Current Drift		25°C − T_{MAX}		200.0	300.0	IV	nA/°C
			25°C − T_{MIN}		200.0	700.0		
A_V	Small Signal Gain	R_L = 100Ω	25°C	0.96	0.98		I	V/V
			T_{MIN}, T_{MAX}	0.95			III	V/V
ILIN	Integral End Point linearity	±2V F.S.	25°C		0.2	0.4	IV	%F.S.
			T_{MIN}			0.8	IV	%F.S.
			T_{MAX}			0.3	IV	%F.S.
PSRR	Power Supply Rejection Ratio		All	45.0	65.0		II	dB
I_S	Supply Current—Quiescent	No Load	All		15.0	20.0	II	mA

DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
R_{IN}	Input Resistance		25°C	100.0	160.0		I	kΩ
			T_{MIN}	50.0			III	kΩ
			T_{MAX}	200.0			III	kΩ
C_{IN}	Input Capacitance		25°C		1.6	2.2	IV	pF
			T_{MIN}, T_{MAX}			2.5	IV	pF
R_{OUT}	Output Impedance (DC)		25°C		2.0	3.0	IV	Ω
			T_{MIN}, T_{MAX}			3.5	IV	Ω
I_{OUT}	Output Current		25°C, T_{MAX}	50.0	70.0		II	mA
			T_{MIN}	45.0			III	mA
V_{OUT}	Output Voltage Swing	R_L = 100Ω	25°C, T_{MAX}	±3.2	±4.0		II	V
			T_{MIN}	±3.0			III	V

AC Electrical Characteristics V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
FREQUENCY RESPONSE								
SSBW	−3 dB Bandwidth (V_{OUT} < 0.5 V_{PP})		25°C	400.0	730.0		III	MHz
			T_{MIN}	400.0			IV	MHz
			T_{MAX}	300.0			IV	MHz
LSBW	−3 dB Bandwidth (V_{OUT} = 5.0 V_{PP})		25°C	55.0	90.0		IV	MHz
			T_{MIN}, T_{MAX}	50.0			IV	MHz
GAIN FLATNESS								
GFPL	Peaking V_{OUT} < 0.5 V_{PP}	<200 MHz	25°C		0.0	0.5	III	dB
			T_{MAX}			0.6	IV	dB
			T_{MIN}			0.8	IV	dB
GFR	Rolloff V_{OUT} < 0.5 V_{PP}	<200 MHz	25°C		0.0	0.8	III	dB
			T_{MIN}			1.0	IV	dB
			T_{MAX}			1.2	IV	dB
GDL	Group Delay	<200 MHz	25°C, T_{MIN}		0.75	1.0	IV	ns
			T_{MAX}			1.2	IV	ns
LPD	Linear Phase Deviation V_{OUT} < 0.5 V_{PP}	<200 MHz	25°C, T_{MIN}		0.7	1.5	IV	°
			T_{MAX}			2.0	IV	°

EL2072C
730 MHz Closed Loop Buffer

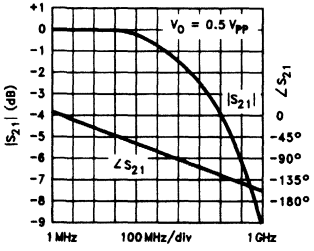
AC Electrical Characteristics — Contd.

V_S = ±5V, R_L = 100Ω, R_S = 50Ω unless otherwise specified

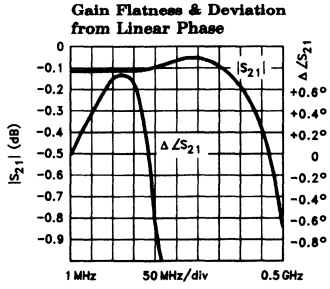
Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level	Units
TIME-DOMAIN RESPONSE								
TR1, TF1	Rise Time, Fall Time Input Signal Rise/Fall = 300 ps	0.5V Step	25°C, T_{MIN}		0.4	1.0	IV	ns
			T_{MAX}			1.4	IV	ns
TR2, TF2	Rise Time, Fall Time Input Signal Rise/Fall ≤ 1 ns	5.0V Step	25°C		4.5	7.5	IV	ns
			T_{MIN}, T_{MAX}			8.5	IV	ns
TS1	Settling Time to 0.2% Input Signal Rise/Fall ≤ 1 ns	2.0V Step	All		5.0	10.0	IV	ns
OS	Overshoot Input Signal Rise/Fall = 300 ps	0.5V Step	25°C		0.0	10.0	IV	%
			T_{MIN}, T_{MAX}			15.0	IV	%
SR	Slew Rate		25°C	500.0	800.0		IV	V/µs
			T_{MIN}, T_{MAX}	450.0			IV	V/µs
DISTORTION								
HD2	2nd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−55.0	−50.0	III	dBc
			T_{MIN}			−48.0	IV	dBc
			T_{MAX}			−55.0	IV	dBc
HD2A	2nd Harmonic Distortion at 50 MHz	2 V_{PP}	25°C , T_{MAX}		−50.0	−45.0	IV	dBc
			T_{MIN}			−40.0	IV	dBc
HD3	3rd Harmonic Distortion at 20 MHz	2 V_{PP}	25°C		−65.0	−55.0	III	dBc
			T_{MIN}, T_{MAX}			−55.0	IV	dBc
HD3A	3rd Harmonic Distortion at 50 MHz	2 V_{PP}	25°C , T_{MIN}		−60.0	−50.0	IV	dBc
			T_{MAX}			−45.0	IV	dBc
EQUIVALENT INPUT NOISE								
NF	Noise Floor >100 kHz		25°C, T_{MIN}		−158.0	−155.0	IV	dBm (1 Hz)
			T_{MAX}			−154.0	IV	dBm (1 Hz)
INV	Integrated Noise 100 kHz to 200 MHz		25°C, T_{MIN}		40.0	57.0	IV	µV
			T_{MAX}			63.0	IV	µV

Typical Performance Curves (V_S = ±5V, R_L = 100Ω, R_S = 50Ω)

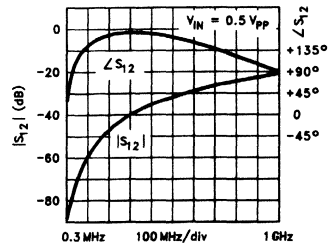
Forward Gain and Phase



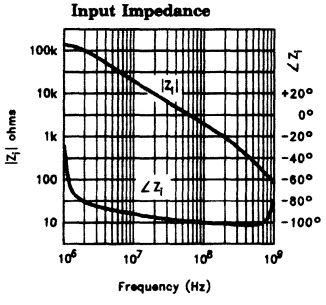
Gain Flatness & Deviation from Linear Phase



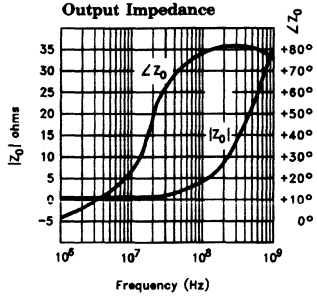
Reverse Gain and phase



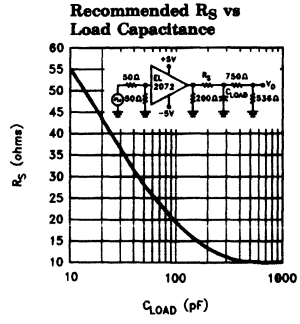
Input Impedance



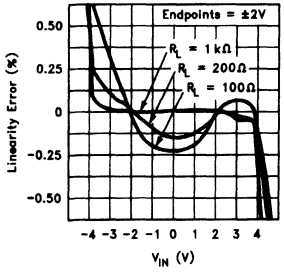
Output Impedance



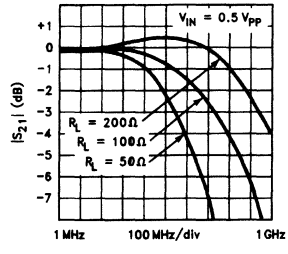
Recommended R_S vs Load Capacitance



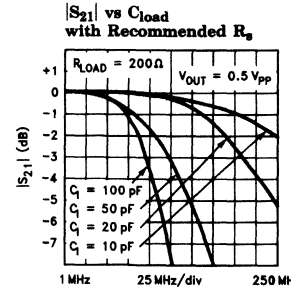
Integral Linearity Error



Frequency Response vs R_{load}



$|S_{21}|$ vs C_{load} with Recommended R_s

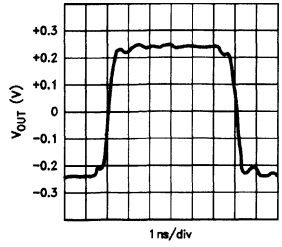


2072-2

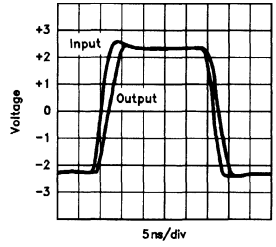
EL2072C
730 MHz Closed Loop Buffer

Typical Performance Curves (V_S = ±5V, R_L = 100Ω, R_S = 50Ω) — Contd.

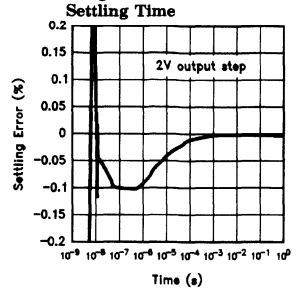
Small Signal Pulse Response



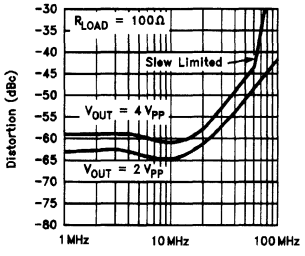
Large Signal Pulse Response



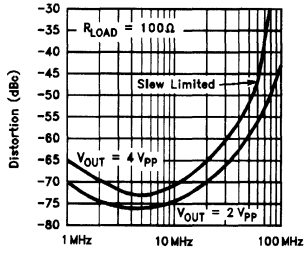
Long-Term Settling Time



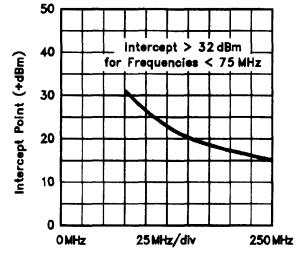
2nd Harmonic Distortion



3rd Harmonic Distortion

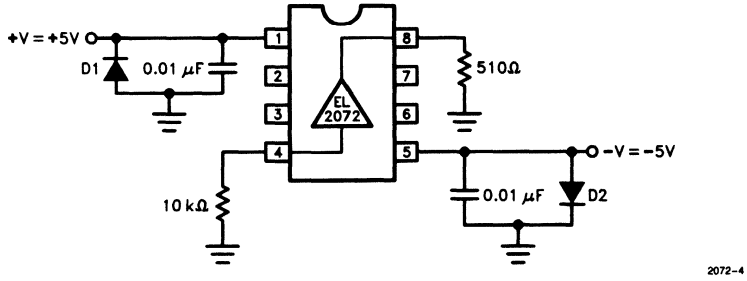


2-Tone, 3rd Order Intermodulation Intercept



2072-3

Burn-In Circuit



Printed Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. This is especially important for the EL2072, which has a typical bandwidth of 730 MHz. Ground plane construction is a requirement, as is good power-supply bypassing close to the package. A closely-placed 0.01 μF ceramic capacitor between each supply pin and the ground plane is usually sufficient decoupling.

Pins 2, 3, 6, and 7 should be connected to the ground-plane to minimize capacitive feedthrough, and all input and output traces should be laid out as transmission lines and terminated as close to the EL2072 package as possible.

Increasing capacitance on the output of the EL2072 will add phase shift, decreasing phase margin and increasing frequency-response peaking. A small series resistor before the capacitance decouples this effect, and should be used for large capacitance values. Please refer to the graphs for the appropriate resistor value to be used.

Power MOSFET Drivers

élantec

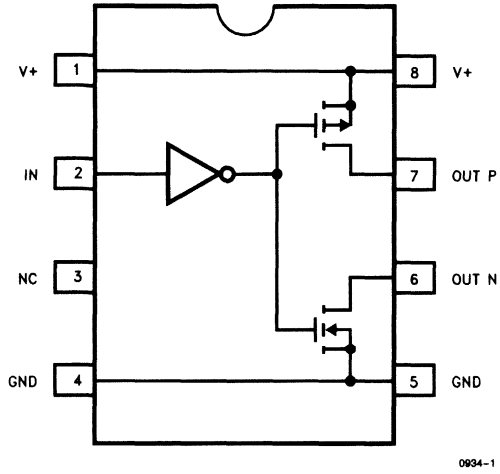
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

CMOS Power MOSFET Drivers

ELANTEC Part Number	Description	Configuration	Peak Current	Max "ON" Resistance	T_{D1}/T_{D2} (ns)	T_R/T_F (ns)	I_S mA	Package
EL7104	High Current/ Single Channel	Non-Inverting/Iso-Drains	4.0A	3Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7114	High Current/ Single Channel	Inverting/Iso-Drains	4.0A	3Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7134	High Current/ Single Channel	3-State	4.0A	3Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7144	High Current/ Single Channel	2-Input Logic AND	4.0A	3Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7182	2-Phase CCD Driver	Complementary Outputs	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7202	Dual Channel	Non-Inverting	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7212	Dual Channel	Inverting	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7222	Dual Channel	Complementary Outputs	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7232	Dual Channel	3-State	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7242	Dual Channel	2-Input Logic AND	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7252	Dual Channel	2-Input Logic NAND	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7262	Dual Channel	Inverting/Iso-Drain	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO
EL7272	Dual Channel	Non-Inverting/Iso-Drain	2.5A	6Ω	20/20	20/20	5.0	8 Pin DIP, 8 Lead SO

Single Channel, 4.0 Amps Output

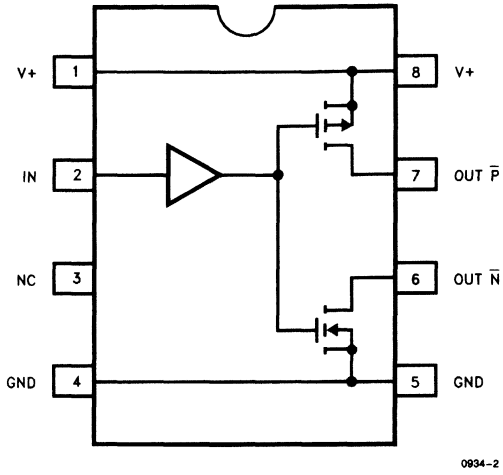
EL7104



Non-Inverting

- Isolated Drains
- 20 ns Switching Time

EL7114

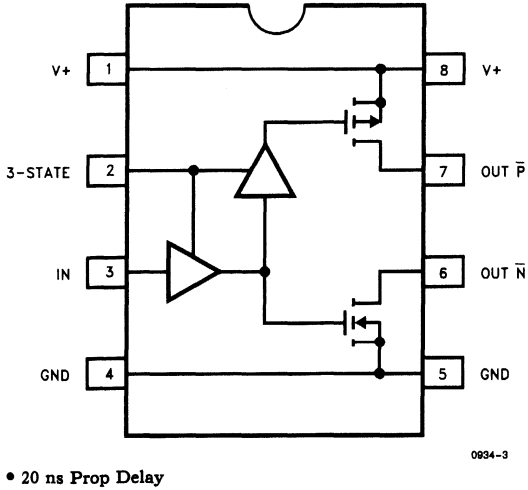


Inverting

- Isolated Drains
- 20 ns Switching Time

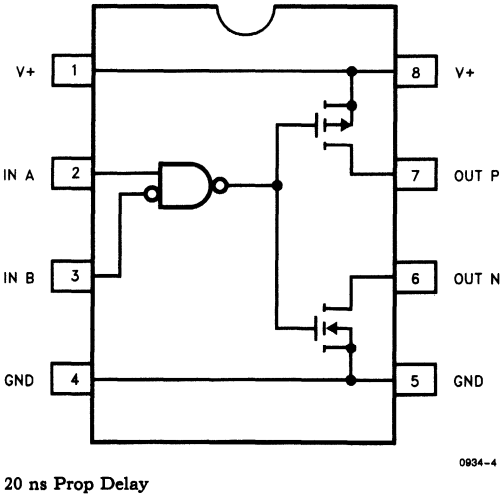
3-State Line Driver/Dual Input Line Driver, 4.0 Amps Output

EL7134



- 20 ns Prop Delay
- 20 ns Switching Time

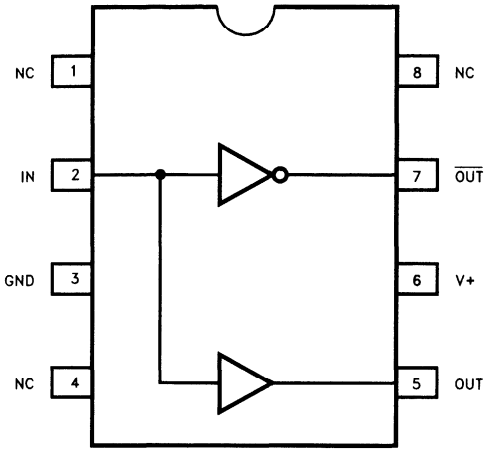
EL7144



- 20 ns Prop Delay
- 20 ns Switching Time

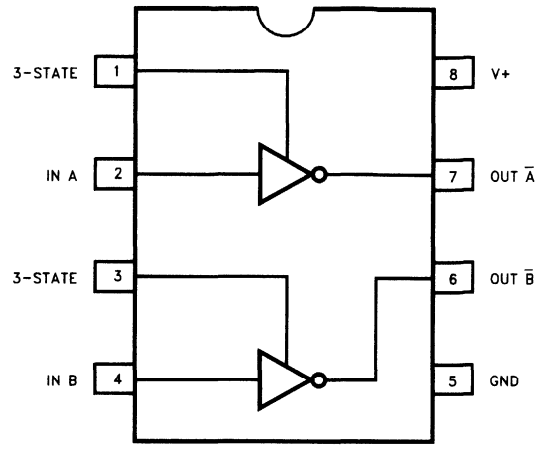
CCD Driver/Dual Channel 3-State Line Driver

EL7182



- Reduced Clock Skew
- 20 ns Switching Time

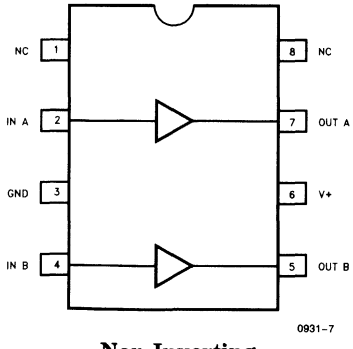
EL7232



- 20 ns Prop Delay
- 20 ns Switching Time

Dual Channel, 2.0 Amps Output

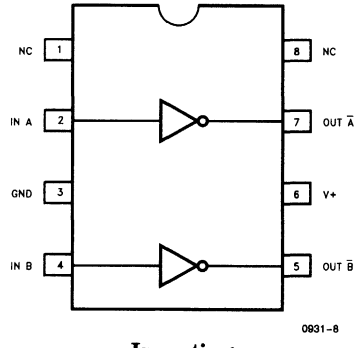
EL7202



Non-Inverting

- 20 ns Prop Delay
- 20 ns Switching Time

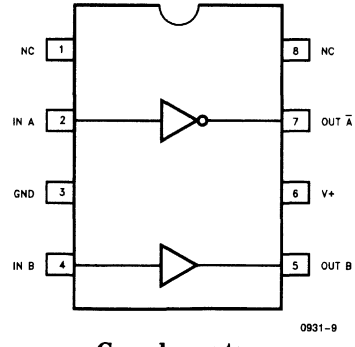
EL7212



Inverting

- 20 ns Prop Delay
- 20 ns Switching Time

EL7222

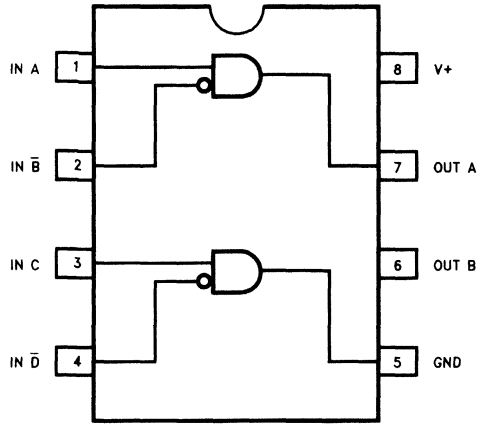


Complementary

- 20 ns Prop Delay
- 20 ns Switching Time

Dual Channel/Dual Input, 2.0 Amps

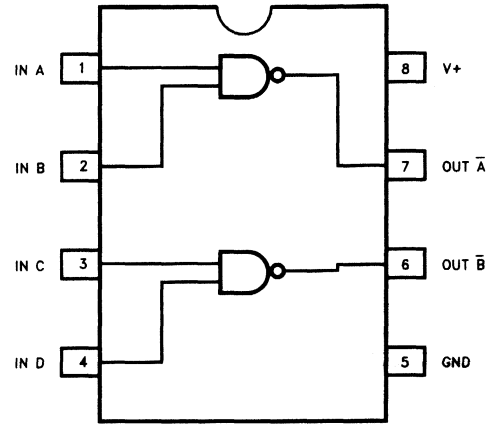
EL7242



0931-10

- 20 ns Prop Delay
- 20 ns Switching Time

EL7252

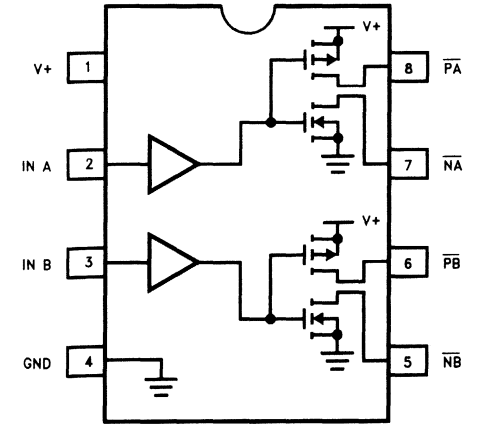


0931-11

- 20 ns Prop Delay
- 20 ns Switching Time

Dual Channel—Isolated Drains, 2.0 Amps

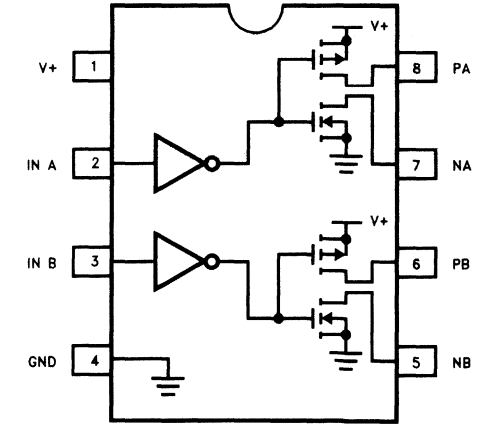
EL7262



0931-12

- 20 ns Prop Delay
- 20 ns Switching Time

EL7272



0931-13

- 20 ns Prop Delay
- 20 ns Switching Time

Applications

• Clock Drivers • Line Drivers • CCD Drivers • Ultrasound Transducer Drivers • Switching Power Supplies • Bus Driver • Motor Control • Charge Pumps • Pin Drivers • EPROM Programming • Resonant Charging Non-overlapped Switching

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7104C/EL7114C

High Speed, Single Channel, Power MOSFET Drivers

Features

- Industry standard driver replacement
- Improved response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating range
- Separate drain connections

Applications

- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Resonant charging
- Cascoded drivers

Ordering Information

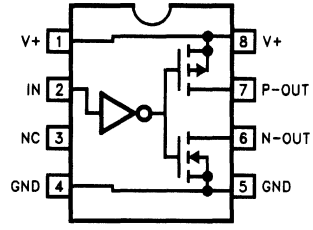
Part No.	Temp. Range	Pkg.	Outline #
EL7104CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7104CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL7114CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7114CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7104C/EL7114C ICs are matched driver ICs that improve the operation of the industry standard TC-4420/29 clock drivers. The Elantec versions are very high speed drivers capable of delivering peak currents of 4A into highly capacitive loads. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices.

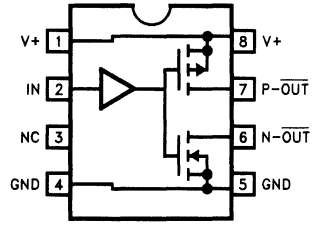
Connection Diagrams

EL7104C
Non-Inverting Driver



7104-1

EL7114C
Inverting Driver



7104-2

EL7104C/EL7114C

High Speed, Single Channel, Power MOSFET Drivers

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics T_A = 25°C, V+ = 15V unless otherwise specified

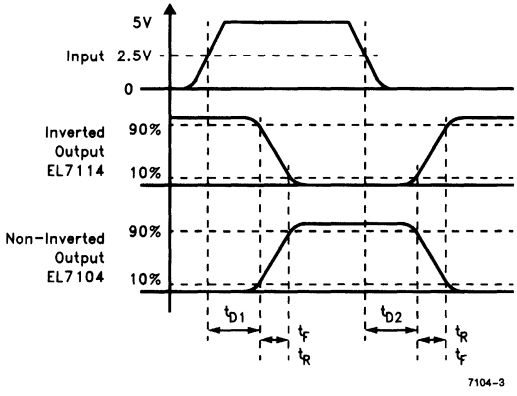
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HYS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		1.5	4	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		2	4	I	Ω
I_{OUT}	Output Current	V+/GND		0.2	10	I	µA
I_{PK}	Peak Output Current	Source Sink		4 4		IV	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Input = V+ EL7104 EL7114		4.5 1	7.5 2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

EL7104C/EL7114C
High Speed, Single Channel, Power MOSFET Drivers

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

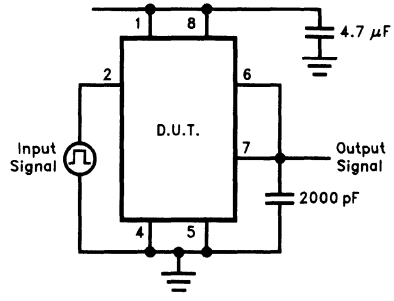
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 1000 pF C_L = 2000 pF		7.5 10	 20	IV	ns
t_F	Fall Time	C_L = 1000 pF C_L = 2000 pF		10 15	 20	IV	ns
t_{D-ON}	Turn-On Delay Time	See Timing Table		18	25	IV	ns
t_{D-OFF}	Turn-Off Delay Time	See Timing Table		18	25	IV	ns

Timing Table



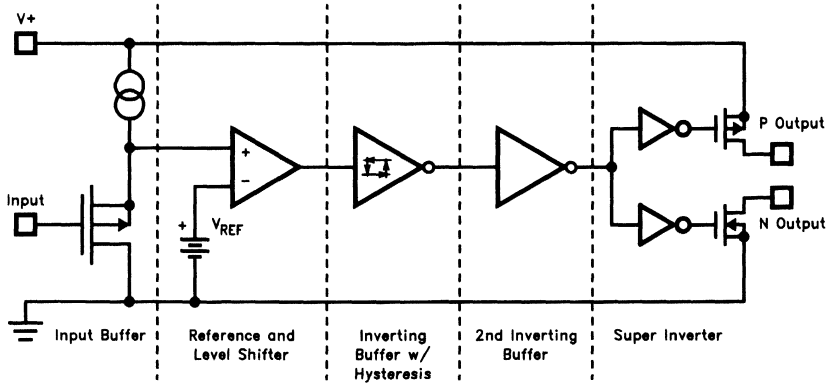
7104-3

Standard Test Configuration



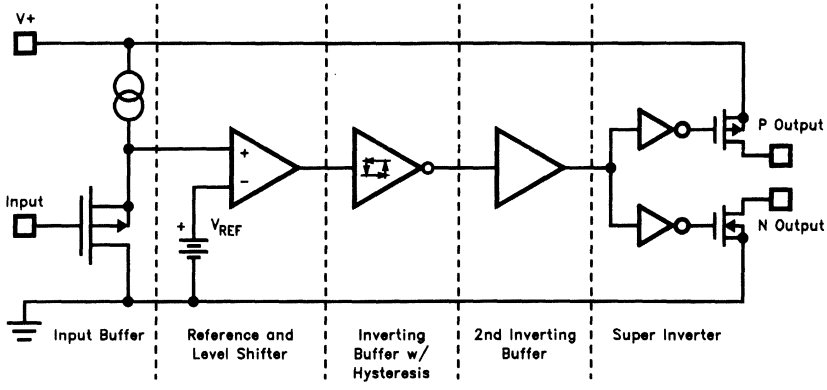
7104-4

7104C Simplified Schematic



7104-5

7114C Simplified Schematic

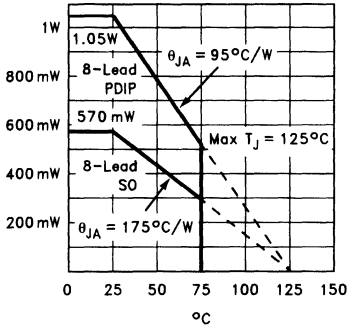


7104-6

EL7104C/EL7114C
High Speed, Single Channel, Power MOSFET Drivers

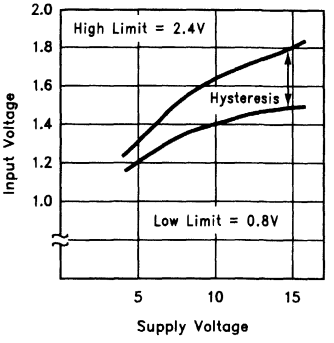
Typical Performance Curve

Max Power/Derating Curves



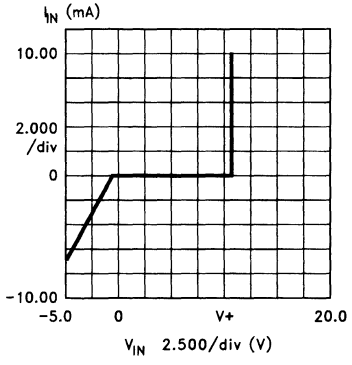
7104-7

Switch Threshold vs Supply Voltage



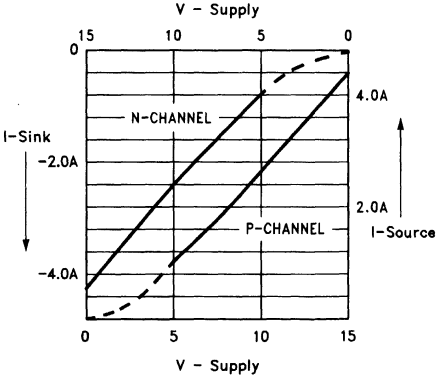
7104-8

Input Current vs Voltage



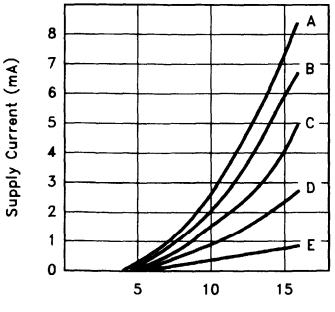
7104-9

Peak Drive vs Supply Voltage



7104-10

Quiescent Supply C

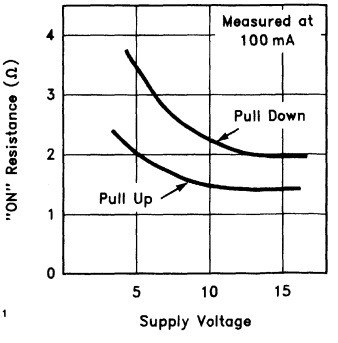


CASE:

Device	Input Level	Curve
EL7104	GND	A
EL7104	V+	C
EL7114	GND	C
EL7114	V+	E

7104-11

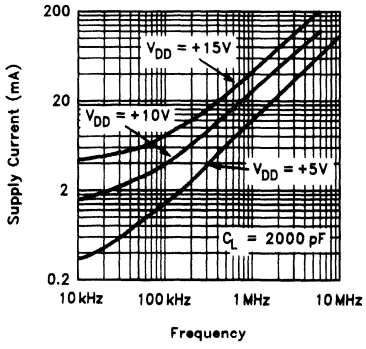
"ON" Resistance vs Supply Voltage



7104-12

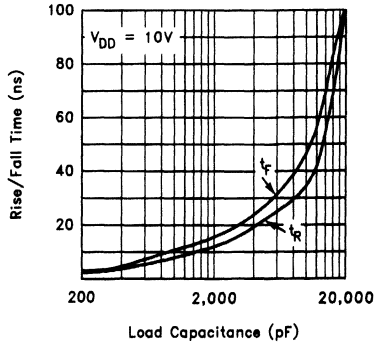
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



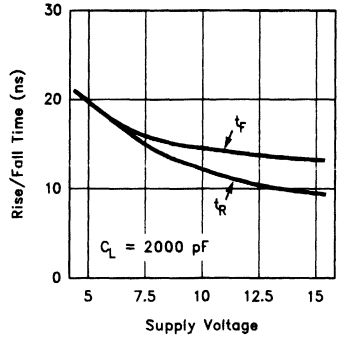
7104-13

Rise/Fall Time vs Load



7104-15

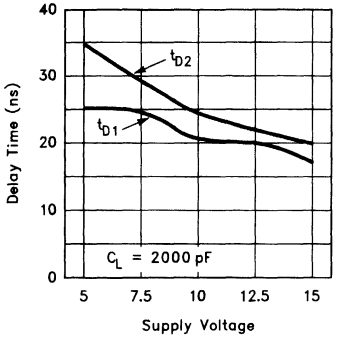
Rise/Fall Time vs Supply Voltage



7104-16

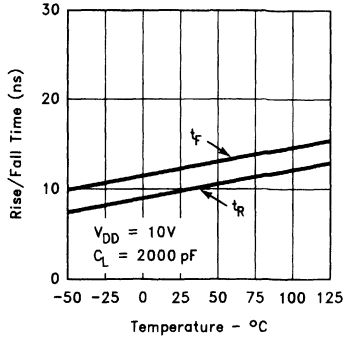
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage



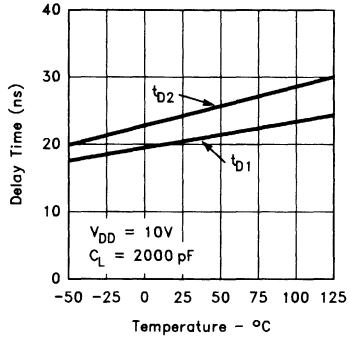
7104-17

Rise/Fall Time vs Temperature



7104-18

Delay vs Temperature



7104-19

Features

- 3-State output
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance—2.5Ω
- Low quiescent current—5 mA
- Wide operating voltage—4.5V–16V

Applications

- Parallel bus line drivers
- EPROM and PROM programming
- Motor controls
- Charge pumps
- Sampling circuits
- Pin drivers

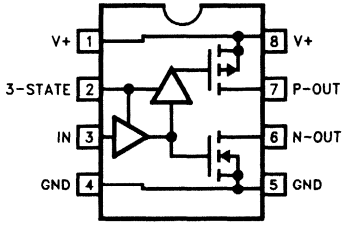
Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7134CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7134CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7134C 3-state driver is particularly well suited for ATE and microprocessor based applications. The low quiescent power dissipation makes this part attractive in battery applications. The 4A peak drive capability, makes the EL7134C an excellent choice when driving high speed capacitive lines.

Connection Diagram



Top View

Truth Table

3-State	Input	P-Out	N-Out
0	0	Open	Open
0	1	Open	Open
1	0	HIGH	Open
1	1	Open	LOW

EL7134C
High Speed, High Current, Line Driver w/3-State

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

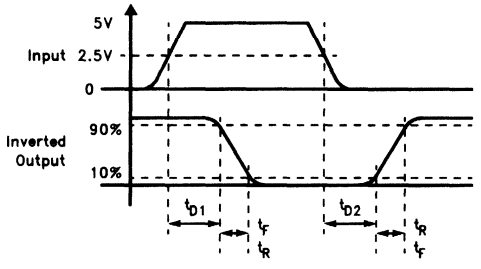
DC Electrical Characteristics T_A = 25°C, V+ = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	V_{IH} = V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	V_{IL} = 0V		0.1	10	I	µA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		1.5	4	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		2	4	I	Ω
I_{OUT}	Output Leakage Current	V+/GND		0.2	10	I	µA
I_{PK}	Peak Output Current	Source Sink		4.0 4.0		V	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Inputs = V+		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

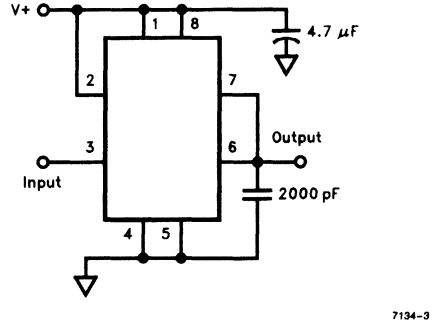
AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test [illegible]	Units
Switching Characteristics							
t_R	Rise Time	C_L = 1000 pF C_L = 2000 pF		7.5 10	 20	[illegible]	ns
t_F	Fall Time	C_L = 1000 pF C_L = 2000 pF		10 13	 20	[illegible]	ns
t_{D-ON}	Turn-On Delay Time			18	25	[illegible]	ns
t_{D-OFF}	Turn-Off Delay Time			18	25	[illegible]	ns

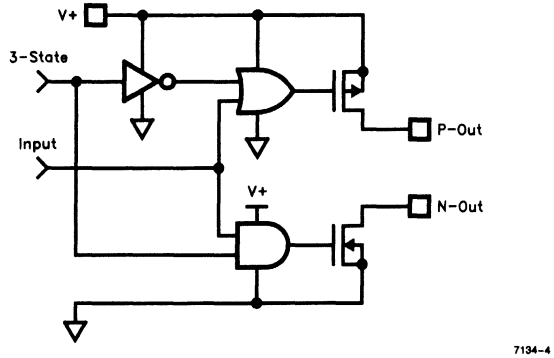
Timing Table



Standard Test Configuration



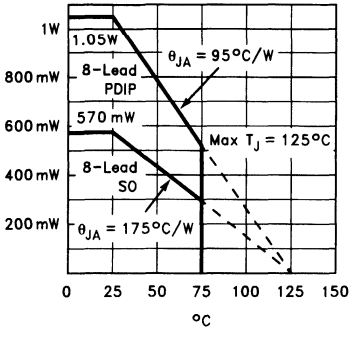
Simplified Schematic



EL7134C
High Speed, High Current, Line Driver w/3-State

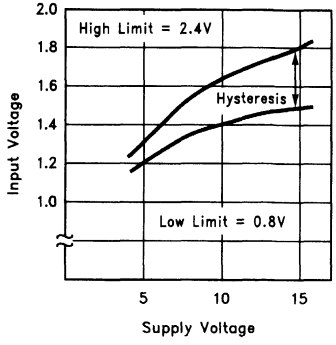
Typical Performance Curve

Max Power/Derating Curves



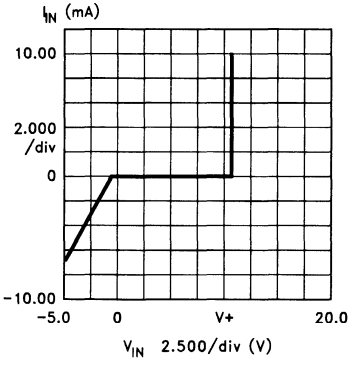
7134-5

Switch Threshold vs Supply Voltage



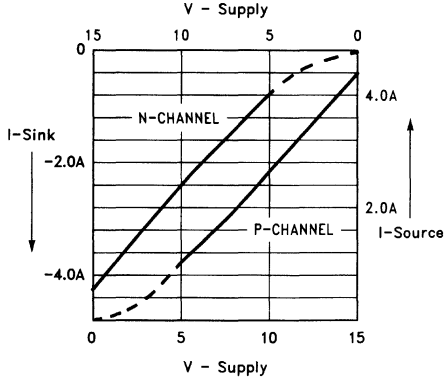
7134-6

Input Current vs Voltage



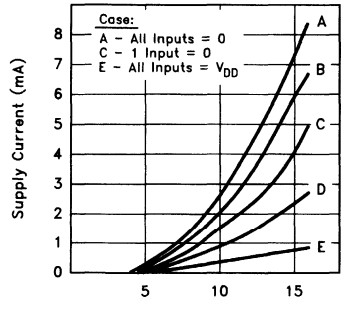
7134-7

Peak Drive vs Supply Voltage



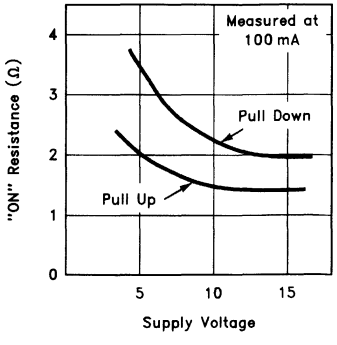
7134-8

Quiescent Supply C



7134-9

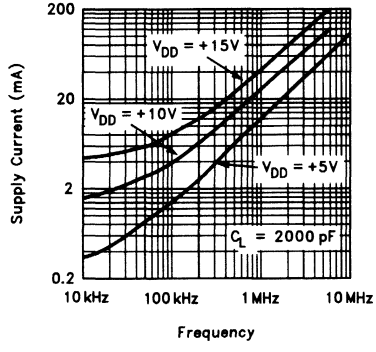
"ON" Resistance vs Supply Voltage



7134-10

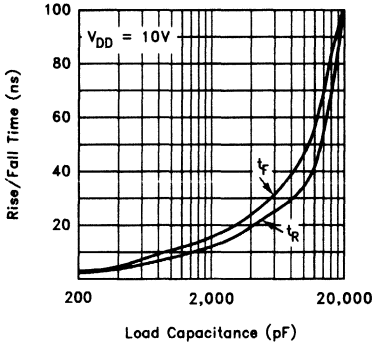
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



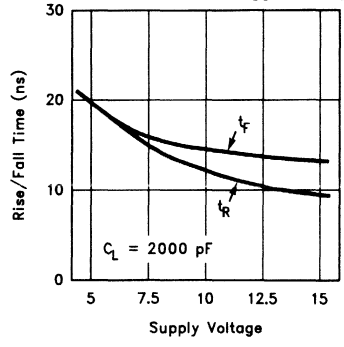
7134-11

Rise/Fall Time vs Load



7134-13

Rise/Fall Time vs Supply Voltage

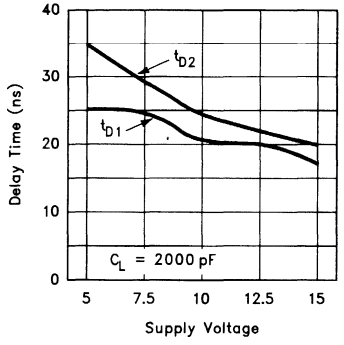


7134-14

EL7134C
High Speed, High Current, Line Driver w/3-State

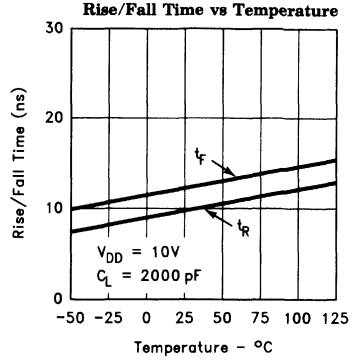
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage



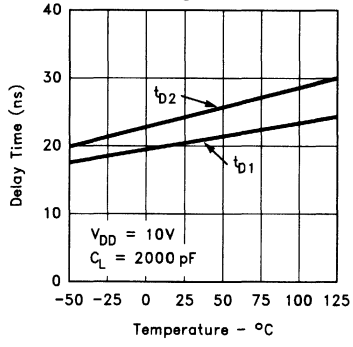
7134-15

Rise/Fall Time vs Temperature



7134-16

Delay vs Temperature



7134-17

EL7144C

Dual Input, High Speed, High Current Power MOSFET Driver

Features

- Logic and input
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 4A Peak drive
- Isolated drains
- Low output impedance—2.5Ω
- Low quiescent current—5 mA
- Wide operating voltage—4.5V–16V

Applications

- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Asymmetrical switching
- Resonant charging
- Cascoded switching

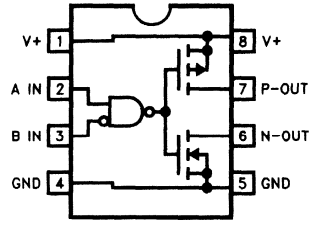
Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7144CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7144CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7144C dual input, driver achieves excellent switching while providing added flexibility. The 2-input logic and configuration coupled with the "isolated drains" makes this part well suited for various driver applications requiring an asymmetrical drive, resonant charging, and gated control. Providing twice as much drive as the EL7242 family, the EL7144C is excellent for driving large power MOSFET's and other capacitive loads.

Connection Diagram



Top View

EL7144C
Dual Input, High Speed, High Current Power MOSFET Driver

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

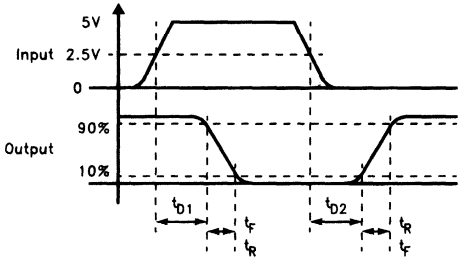
DC Electrical Characteristics T_A = 25°C, V+ = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	V_{IH} = V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	V_{IL} = GND		0.1	10	I	µA
V_{HYS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		1.5	4	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		2	4	I	Ω
I_{OUT}	Output Leakage Current	V+/GND		0.2	10	I	µA
I_{PK}	Peak Output Current	Source Sink		4 4		V	A
I_{DC}	Continuous Output Current	Source/Sink	200			I	mA
Power Supply							
I_S	Power Supply Current	Inputs V+		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

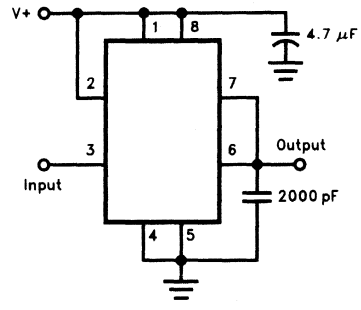
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 1000 pF C_L = 2000 pF		7.5 10	 20		ns
t_F	Fall Time	C_L = 1000 pF C_L = 2000 pF		10 13	 20		ns
t_{D-ON}	Turn-On Delay Time	See Timing Table		18	25		ns
t_{D-OFF}	Turn-Off Delay Time	See Timing Table		20	25		ns

Timing Table



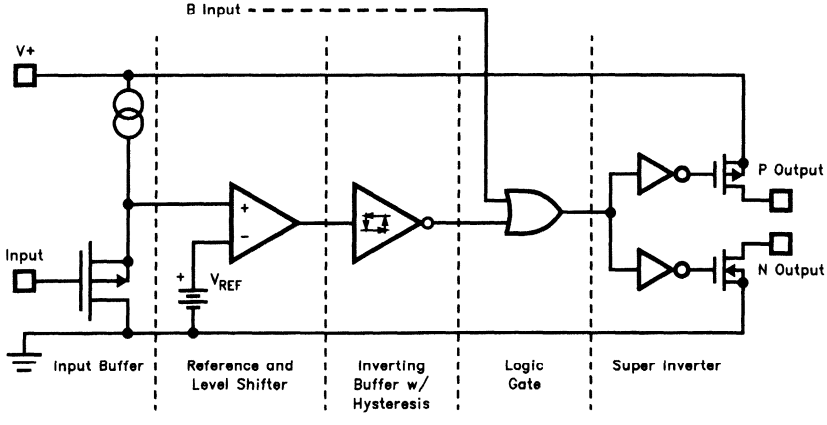
7144-2

Standard Test Configuration



7144-3

Simplified Schematic

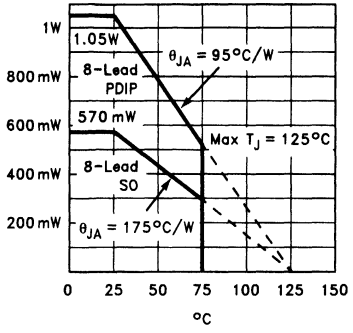


7144-4

EL7144C
Dual Input, High Speed, High Current Power MOSFET Driver

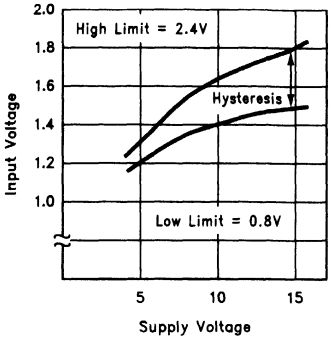
Typical Performance Curve

Max Power/Derating Curves



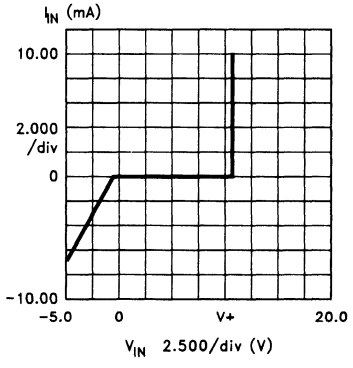
7144-5

Switch Threshold vs Supply Voltage



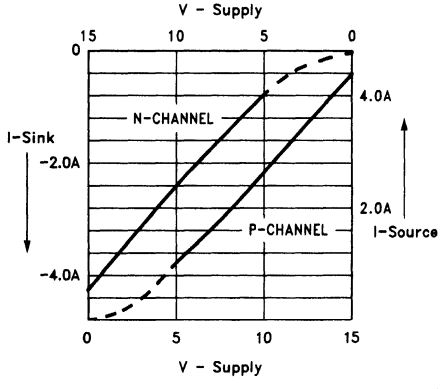
7144-6

Input Current vs Voltage



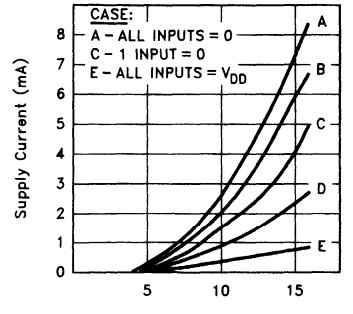
7144-7

Peak Drive vs Supply Voltage



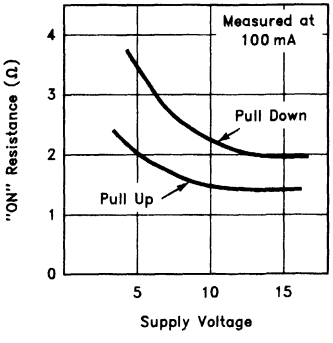
7144-8

Quiescent Supply C



7144-9

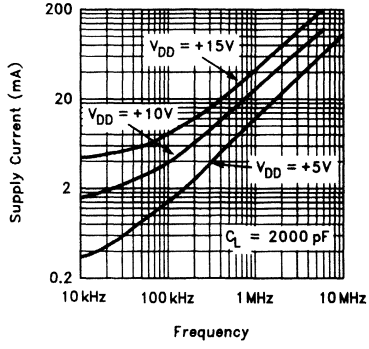
"ON" Resistance vs Supply Voltage



7144-10

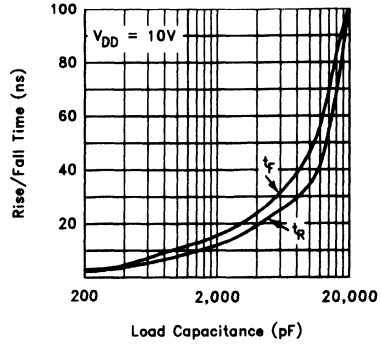
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



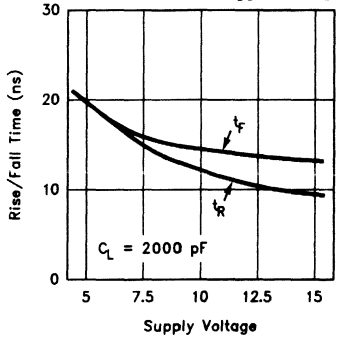
7144-11

Rise/Fall Time vs Load



7144-13

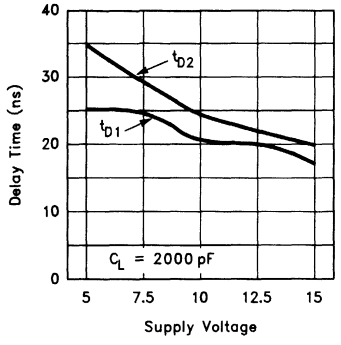
Rise/Fall Time vs Supply Voltage



7144-14

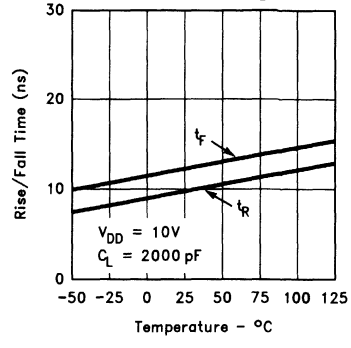
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage



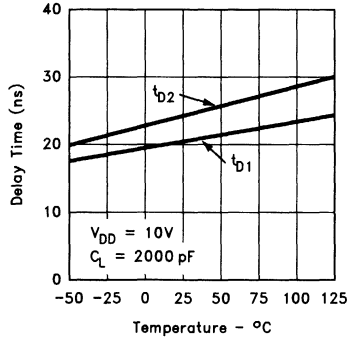
7144-15

Rise/Fall Time vs Temperature



7144-16

Delay vs Temperature



7144-17

EL7182C
2-Phase, High Speed CCD Driver

Features

- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- Reduced clock skew
- 20 ns Switching/delay time
- 2A Peak drive
- Low quiescent current
- Wide operating voltage—4.5V–16V

Applications

- CCD Drivers requiring high-contrast imaging
- Differential line drivers
- Push-pull circuits

Ordering Information

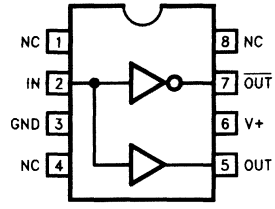
Part No.	Temp. Range	Pkg.	Outline #
EL7182CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7182CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL7182C is extremely well suited for driving CCD's, especially where high contrast imaging is desirable. The 16V supply rating is attractive for higher voltage CCD applications, as in color fax machines. The input is TTL and 3V compatible. The low quiescent current requirement is advantageous in portable/battery powered systems. The EL7182 is available in 8-pin P-DIP and 8-lead SO packages.

Connection Diagram

EL7182C



7182-1

EL7182C
2-Phase, High Speed CCD Driver

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

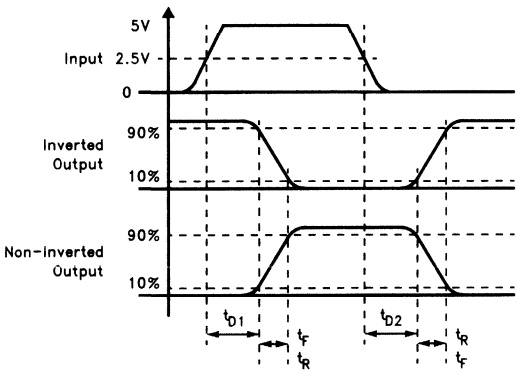
DC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Input High		2.5	5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

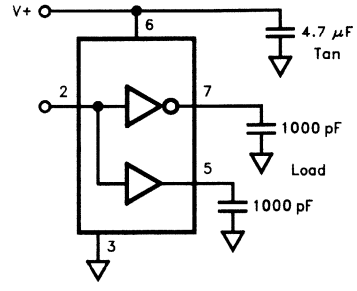
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		7.5 10	 20	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		10 13	 20	IV	ns
t_{D-ON}	Turn-On Delay Time			18	25	IV	ns
t_{D-OFF}	Turn-Off Delay Time			20	25	IV	ns

Timing Table



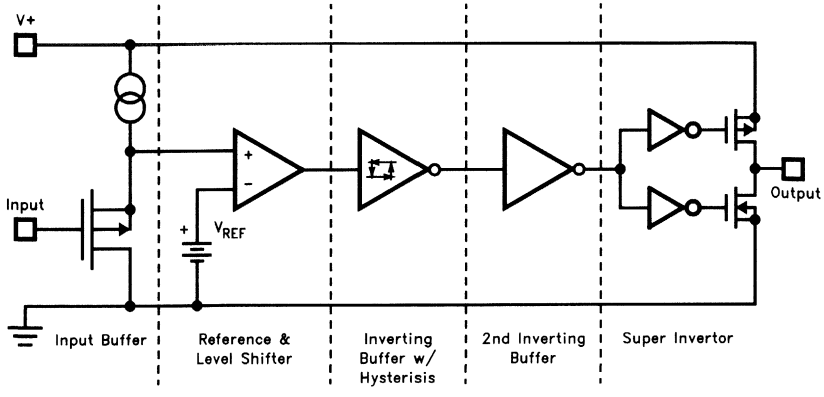
7182-2

Standard Test Configuration



7182-3

Simplified Schematic

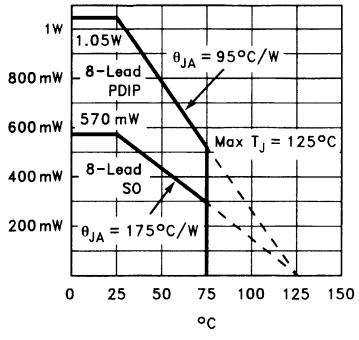


7182-17

EL7182C
2-Phase, High Speed CCD Driver

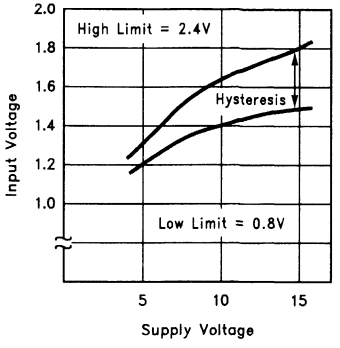
Typical Performance Curve

Max Power/Derating Curves



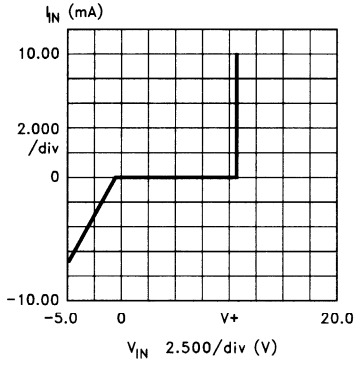
7182-15

Switch Threshold vs Supply Voltage



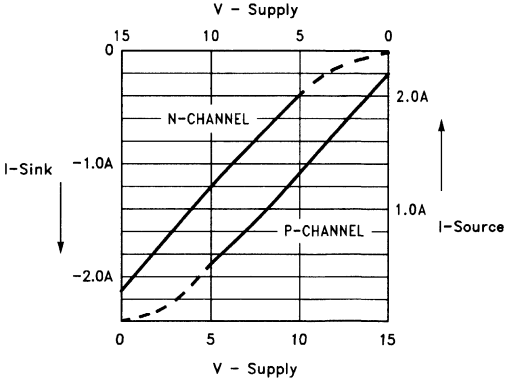
7182-4

Input Current vs Voltage



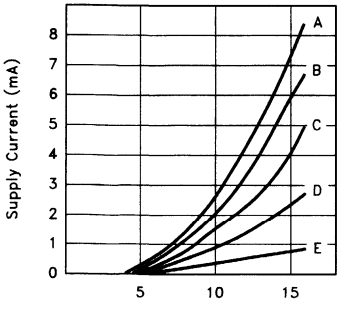
7182-5

Peak Drive vs Supply Voltage



7182-6

Quiescent Supply C

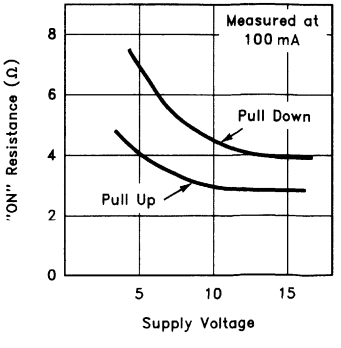


CASE:

Input Level	Curve
GND	B
V+	D

7182-7

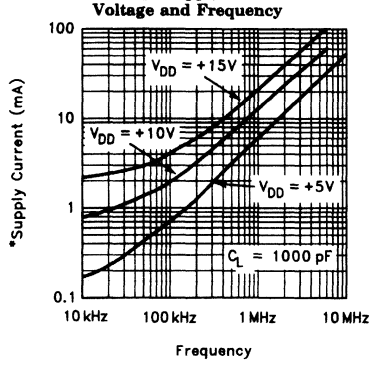
"ON" Resistance vs Supply Voltage



7182-16

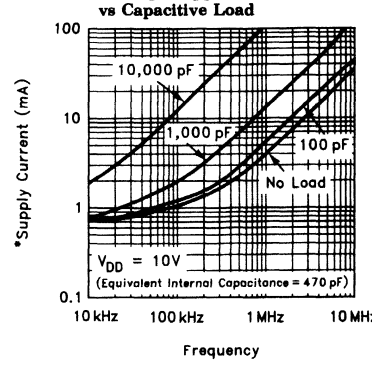
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



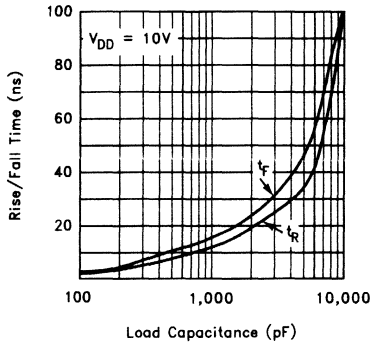
7182-8

Average Supply Current vs Capacitive Load



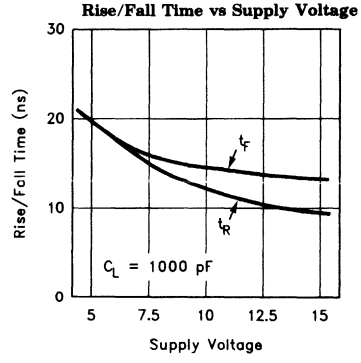
7182-9

Rise/Fall Time vs Load



7182-14

Rise/Fall Time vs Supply Voltage



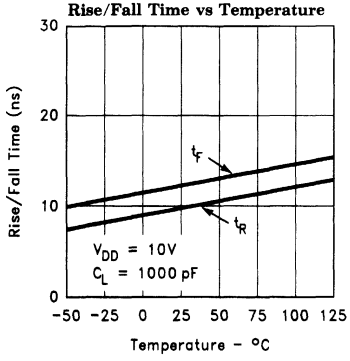
7182-10

3

EL7182C
2-Phase, High Speed CCD Driver

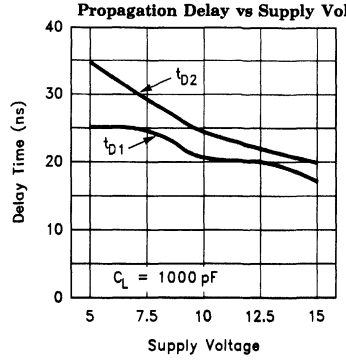
Typical Performance Curve — Contd.

Rise/Fall Time vs Temperature



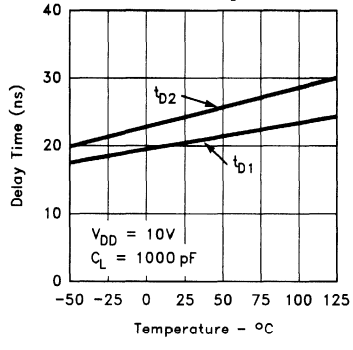
7182-12

Propagation Delay vs Supply Voltage



7182-11

Delay Time vs Temperature



7182-13

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL7202C/7212C/7222C

High Speed, Dual Channel Power MOSFET Drivers

Features

- Industry standard driver replacement
- Improved response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating voltage range

Applications

- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Class D switching amplifiers
- Ultrasonic and RF generators
- Pulsed circuits

Ordering Information

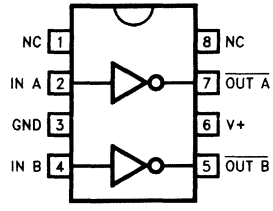
Part No.	Temp. Range	Pkg.	Outline #
EL7202CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7202CS	−40°C to +85°C	8-Pin SOL	MDP0027
EL7212CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7212CS	−40°C to +85°C	8-Pin SOL	MDP0027
EL7222CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7222CS	−40°C to +85°C	8-Pin SOL	MDP0027

General Description

The EL7202C/EL7212C/EL7222C ICs are matched dual-drivers ICs that improve the operation of the industry standard DS0026 clock drivers. The Elantec Versions are very high speed drivers capable of delivering peak currents of 2.0 amps into highly capacitive loads. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

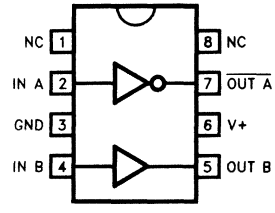
Connection Diagrams

EL7212C



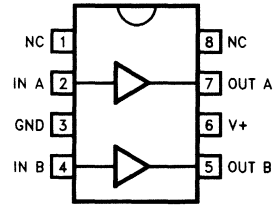
Inverting Drivers

EL7222C



Complementary Drivers

EL7202C



Non-Inverting Drivers

EL7202C/EL7212C/EL7222C
High Speed, Dual Channel Power MOSFET Drivers

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterisation Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

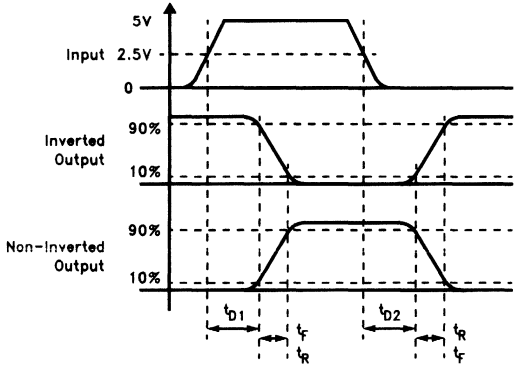
DC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HYS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High/7202 Inputs High/7212 Inputs High/7222		4.5 1 2.5	7.5 2.5 5.0	I I I	mA
V_S	Operating Voltage		4.5		15	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

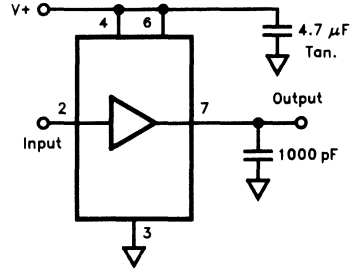
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		7.5 10	 20		ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		10 13	 20		ns
t_{D1}	Turn-On Delay Time	See Timing Table		18	25		ns
t_{D2}	Turn-Off Delay Time	See Timing Table		20	25		ns

Timing Table



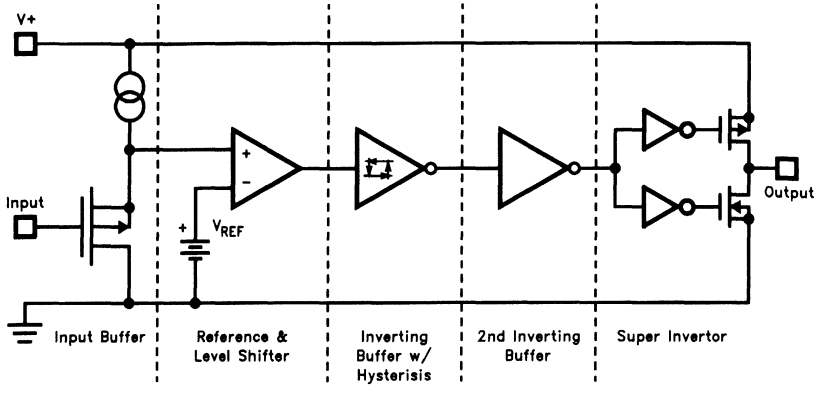
7202-4

Standard Test Configuration



7202-19

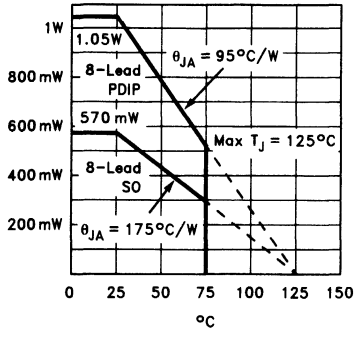
Simplified Schematic



7202-5

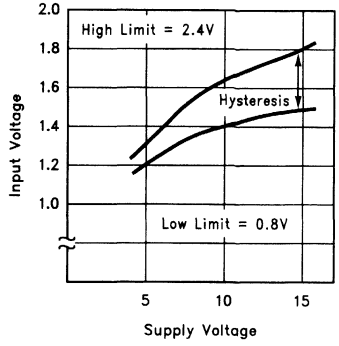
Typical Performance Curve

Max Power/Derating Curves



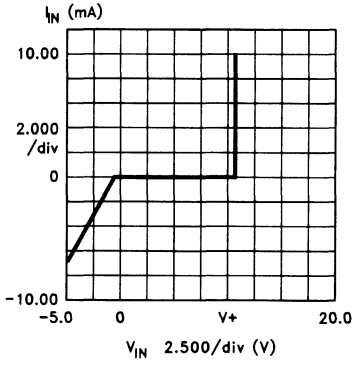
7202-6

Switch Threshold vs Supply Voltage



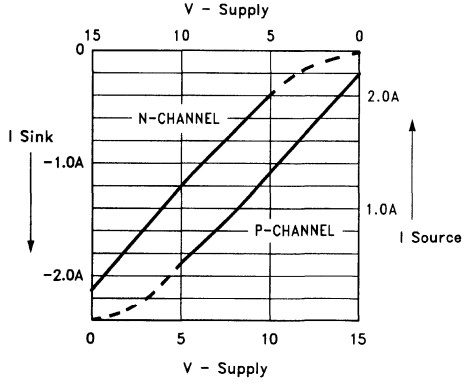
7202-7

Input Current vs Voltage



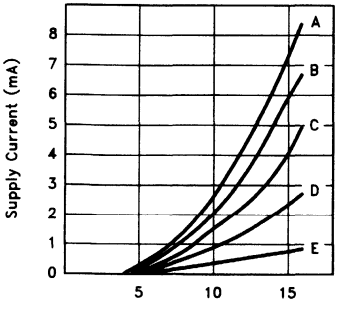
7202-8

Peak Drive vs Supply Voltage



7202-9

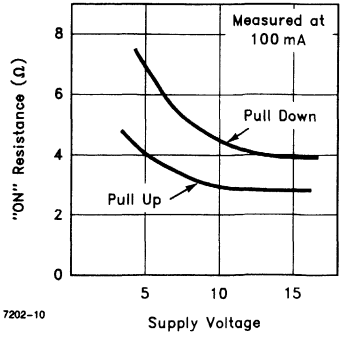
Quiescent Supply C



CASE:

Device	Input Level	Curve
EL7202	GND	A
EL7202	GND, V+	B
EL7202	V+	C
EL7212	GND	C
EL7212	GND, V+	D
EL7212	V+	E
EL7222	GND	B
EL7222	GND, V+	C
EL7222	V+	D

"ON" Resistance vs Supply Voltage

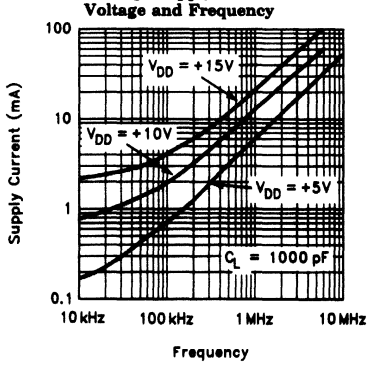


7202-10

7202-11

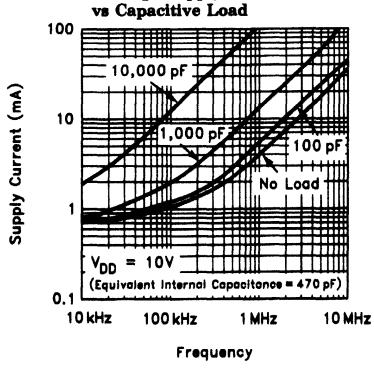
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



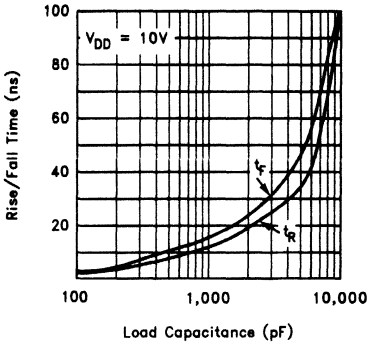
7202-12

Average Supply Current vs Capacitive Load



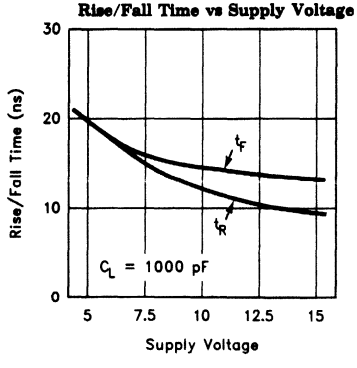
7202-13

Rise/Fall Time vs Load



7202-14

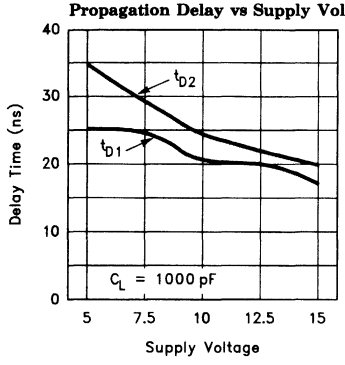
Rise/Fall Time vs Supply Voltage



7202-15

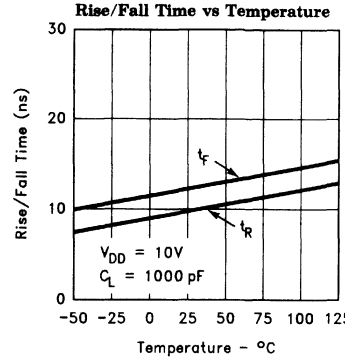
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage



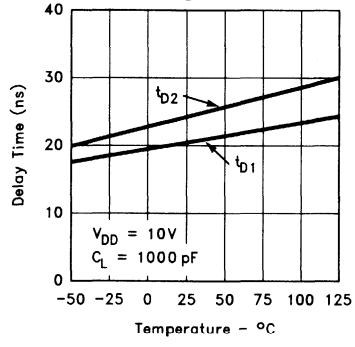
7202-16

Rise/Fall Time vs Temperature



7202-17

Delay vs Temperature



7202-18

EL7232C

Dual Channel, High Speed, High Current Line Driver w/3-State

Features

- 3-State output
- 3V and 5V input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Low, matched output impedance—5Ω
- Low quiescent current—2.5 mA
- Wide operating voltage—4.5V--16V

Applications

- Parallel bus line drivers
- EPROM and PROM programming
- Motor controls
- Charge pumps
- Sampling circuits
- Pin drivers
- Bridge circuits

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL7232CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7232CS	−40°C to +85°C	8-Pin SO	MDP0027

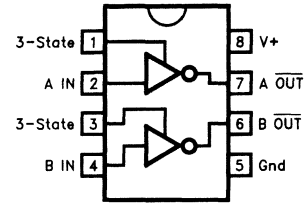
Truth Table

3-State	Input	Output
1	0	1
1	1	0
0	0	Open
0	1	Open

General Description

The EL7232C 3-state drivers are particularly well suited for ATE and microprocessor based applications. The low quiescent power dissipation makes this part attractive in battery applications. The 2A peak drive capability, makes the EL7232C an excellent choice when driving high speed capacitive lines, as well. The input circuitry provides level shifting from TTL levels to the supply rails. The EL7232C is available in 8-pin P-DIP and 8-lead SO packages.

Connection Diagram



7232-1

EL7232C

Dual Channel, High Speed, High Current Line Driver w/3-State

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All electrical specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTS2??? Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

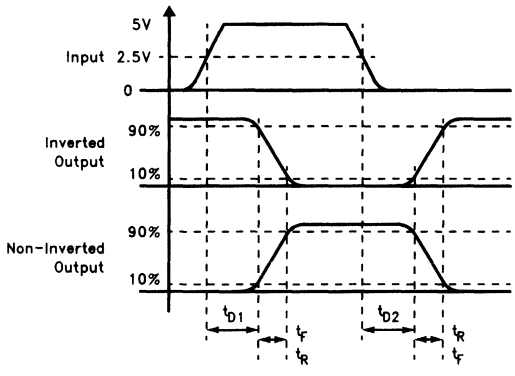
DC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max		Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HYS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		4	6	I	Ω
I_{OFF}	3-State Output Leakage	V_{OUT} = V+ V_{OUT} = 0V	0.2		10	I	µA
I_{PK}	Peak Output Current	Source Sink		2.0 2.0		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

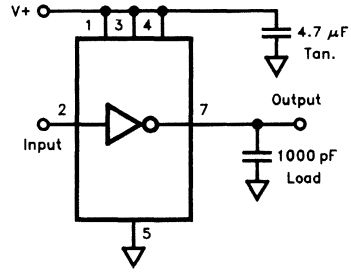
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		7.5 10		IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		10 13	20	IV	ns
t_{D-ON}	Turn-On Delay Time			18	25	IV	ns
t_{D-OFF}	Turn-Off Delay Time			20	25	IV	ns

Timing Table



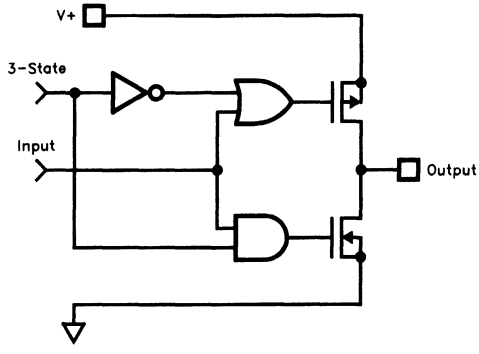
7232-2

Standard Test Configuration



7232-3

Simplified Schematic

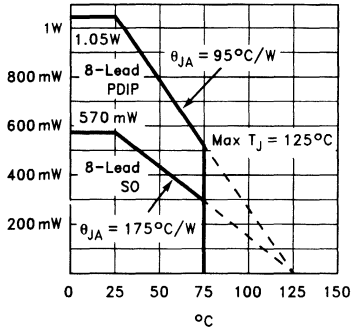


7232-4

EL7232C
Dual Channel, High Speed, High Current Line Driver w/3-State

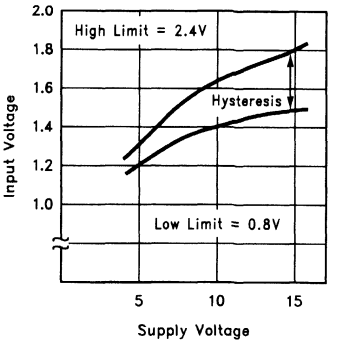
Typical Performance Curve

Max Power/Derating Curves



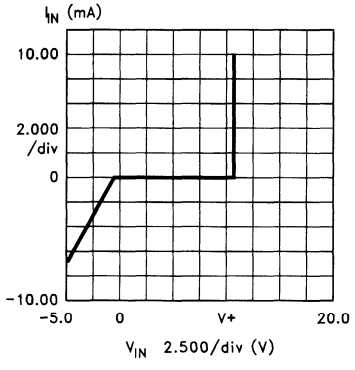
7232-6

Switch Threshold vs Supply Voltage



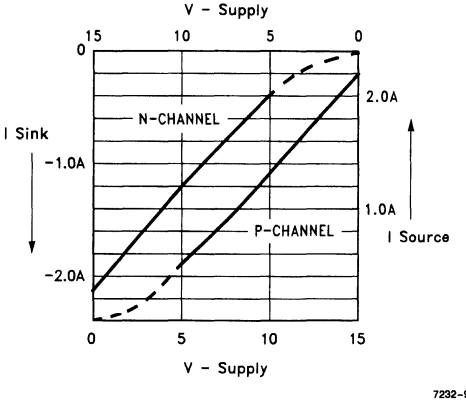
7232-7

Input Current vs Voltage



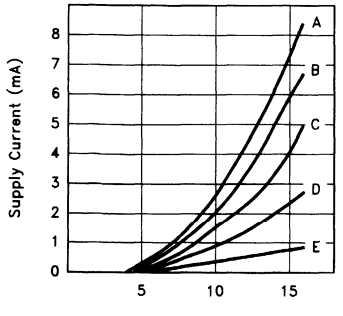
7232-8

Peak Drive vs Supply Voltage



7232-9

Quiescent Supply C

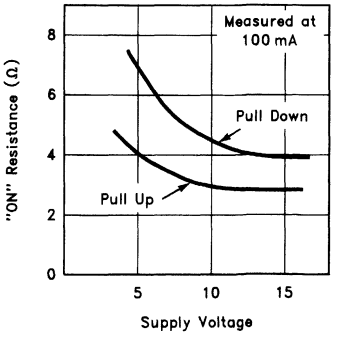


CASE:

Device	Input Level	Curve
EL7202	GND	A
EL7202	GND, V+	B
EL7202	V+	C
EL7212	GND	C
EL7212	GND, V+	D
EL7212	V+	E
EL7222	GND	B
EL7222	GND, V+	C
EL7222	V+	D

7232-10

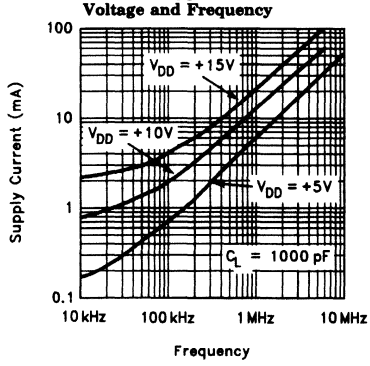
"ON" Resistance vs Supply Voltage



7232-17

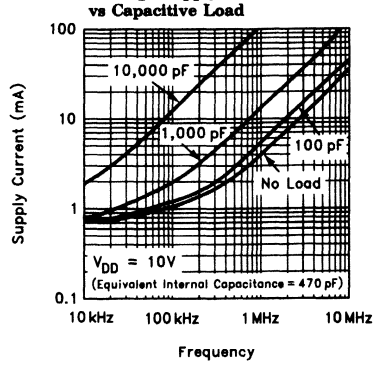
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



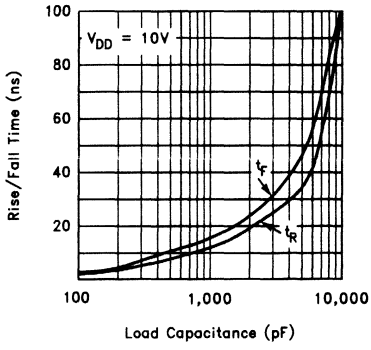
7232-11

Average Supply Current vs Capacitive Load



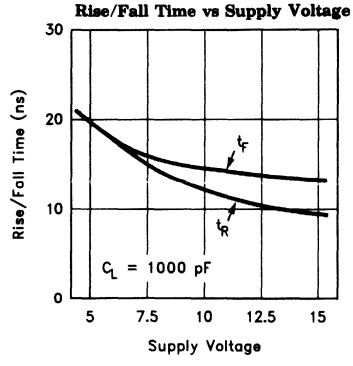
7232-12

Rise/Fall Time vs Load



7232-5

Rise/Fall Time vs Supply Voltage

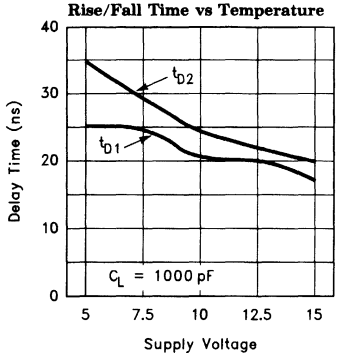


7232-13

EL7232C
Dual Channel, High Speed, High Current Line Driver w/3-State

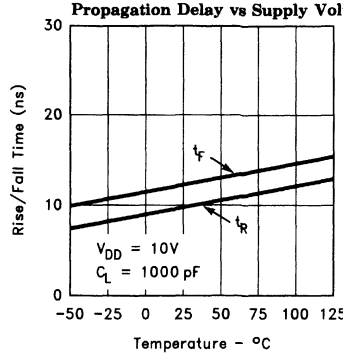
Typical Performance Curve — Contd.

Rise/Fall Time vs Temperature



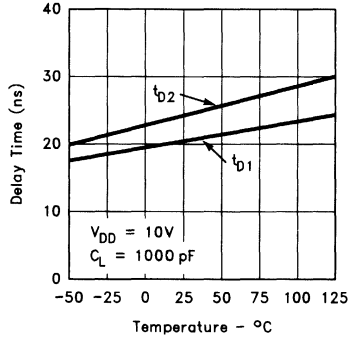
7232-14

Propagation Delay vs Supply Voltage



7232-15

Propagation Delay vs Temperature



7232-16

EL7242C/EL7252C

Dual Input, High Speed, Dual Channel Power MOSFET Drivers

Features

- Logic AND/NAND input
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Isolated drains
- Low output impedance
- Low quiescent current
- Wide operating voltage—4.5V–16V

Applications

- Short circuit protected switching
- Under-voltage shut-down circuits
- Switch-mode power supplies
- Motor controls
- Power MOSFET switching
- Switching capacitive loads
- Shoot-thru protection
- Latching drivers

Ordering Information

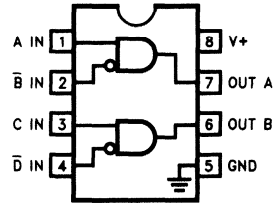
Part No.	Temp. Range	Pkg.	Outline #
EL7242CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7242CS	−40°C to +85°C	8-Pin SOIC	MDP0027
EL7252CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7252CS	−40°C to +85°C	8-Pin SOIC	MDP0027

General Description

The EL7242C/EL7252C dual input, 2-channel drivers achieve the same excellent switching performance of the EL7212 family while providing added flexibility. The 2-input logic and configuration is applicable to numerous power MOSFET drive circuits. As with other Elantec drivers, the EL7242C/EL7252C are excellent for driving large capacitive loads with minimal delay and switching times. "Shoot-thru" protection and latching circuits can be implemented by simply "cross-coupling" the 2-channels.

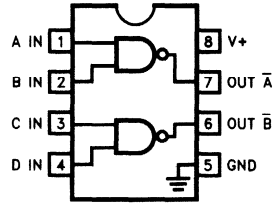
Connection Diagrams

EL7242C



7242-1

EL7252C



7242-2

EL7242C/EL7252C
Dual Input, High Speed, Dual Channel Power MOSFET Driver

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

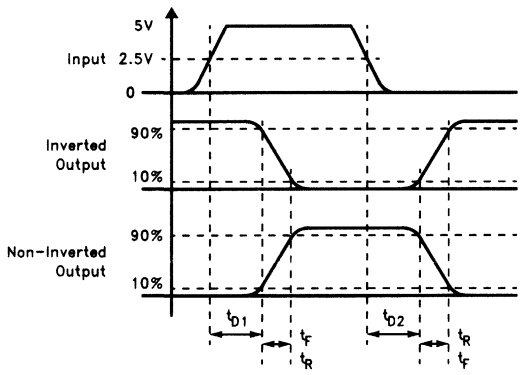
DC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HVS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		4	6	I	Ω
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs High		1	2.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

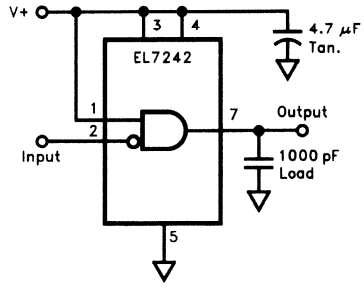
Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF			10 20	IV	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF			10 20	IV	ns
t_{D-ON}	Turn-On Delay Time			20	25	IV	ns
t_{D-OFF}	Turn-Off Delay Time			20	25	IV	ns

Timing Table



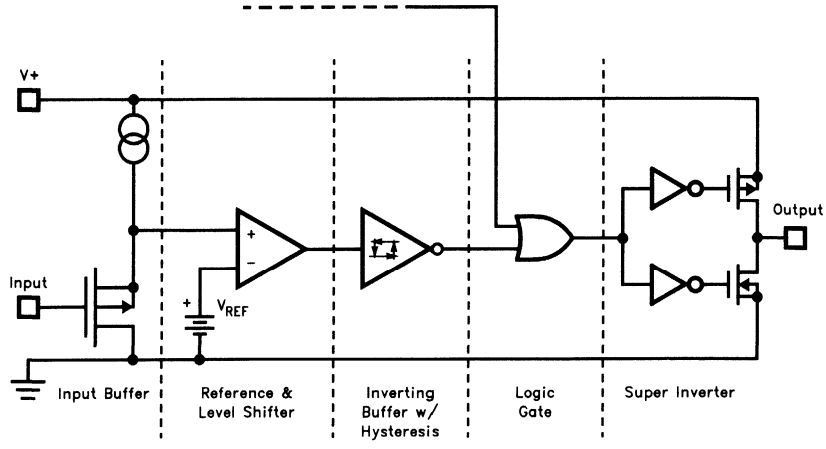
7242-3

Standard Test Configuration



7242-4

Simplified Schematic

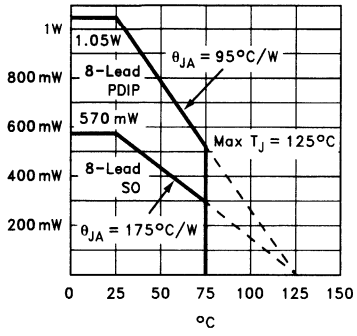


7242-5

EL7242C/EL7252C
Dual Input, High Speed, Dual Channel Power MOSFET Driver

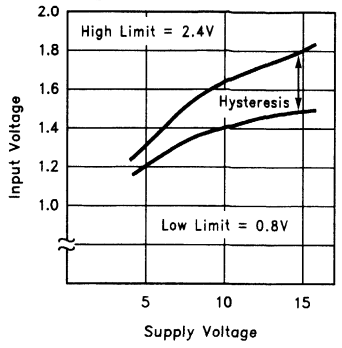
Typical Performance Curve

Max Power/Derating Curves



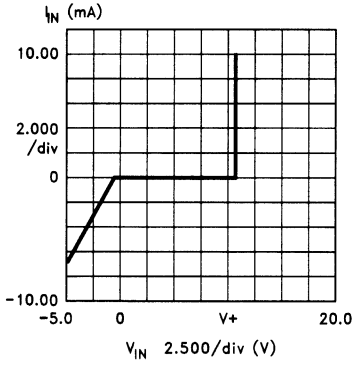
7242-17

Switch Threshold vs Supply Voltage



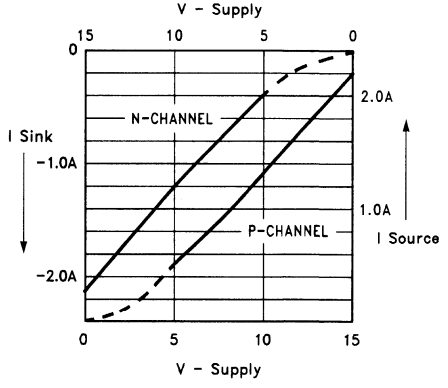
7242-6

Input Current vs Voltage



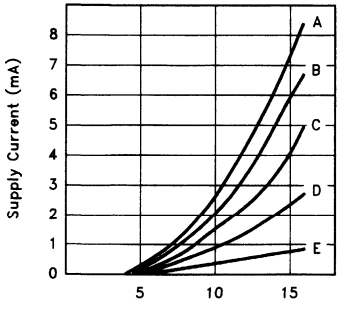
7242-7

Peak Drive vs Supply Voltage



7242-8

Quiescent Supply C

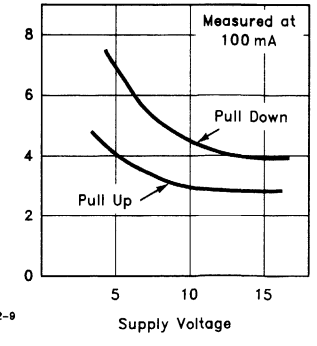


CASE:

Device	Input Level	Curve
EL7202	GND	A
EL7202	GND, V+	B
EL7202	V+	C
EL7212	GND	C
EL7212	GND, V+	D
EL7212	V+	E
EL7222	GND	B
EL7222	GND, V+	C
EL7222	V+	D

7242-9

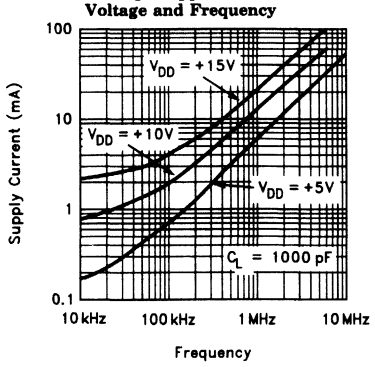
"ON" Resistance vs Supply Voltage



7242-18

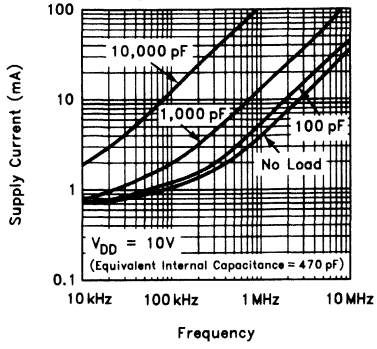
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



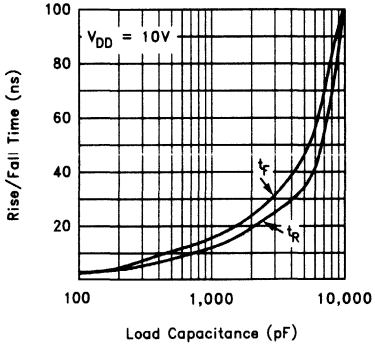
7242-10

Average Supply Current vs Capacitive Load



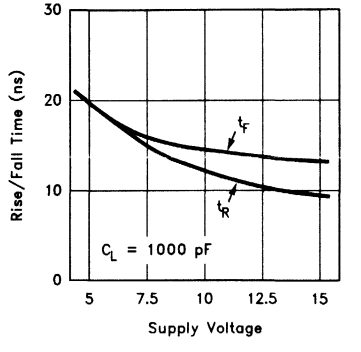
7242-11

Rise/Fall Time vs Load



7242-16

Rise/Fall Time vs Supply Voltage

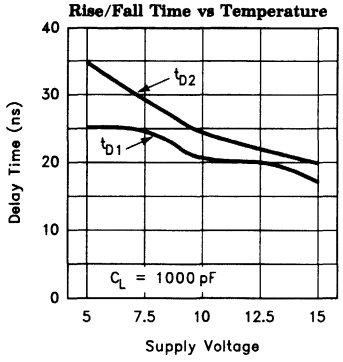


7242-12

EL7242C/EL7252C
Dual Input, High Speed, Dual Channel Power MOSFET Driver

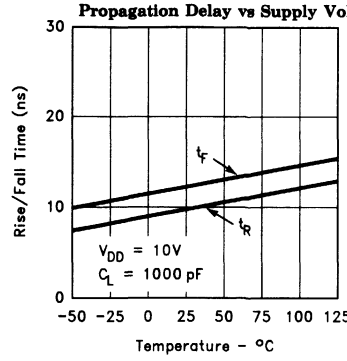
Typical Performance Curve — Contd.

Rise/Fall Time vs Temperature



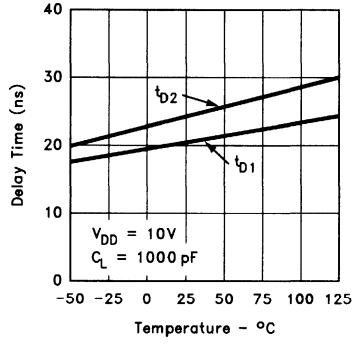
7242-13

Propagation Delay vs Supply Voltage



7242-14

Delay vs Temperature



7242-15

Features

- Separate drain connections
- 3V and 5V Input compatible
- Clocking speeds up to 10 MHz
- 20 ns Switching/delay time
- 2A Peak drive
- Low output impedance
- Low quiescent current
- Wide operating voltage

Applications

- Asymetrical switching
- Cascoded switching
- Resonant charging
- Floating load circuits
- Bridge circuits

Ordering Information

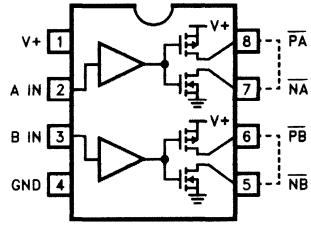
Part No.	Temp. Range	Pkg.	Outline #
EL7262CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7262CS	−40°C to +85°C	8-Pin SO	MDP0027
EL7272CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL7272CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL7262C/EL7272C, dual channel, power MOSFET drivers achieve the same excellent switching performance of the EL7202 family, with the added flexibility derived through the isolated drain architecture. The outputs can be configured in numerous ways, depending upon the application. The EL7262C and EL7272C are available in 8-pin P-DIP and 8-lead SO packages.

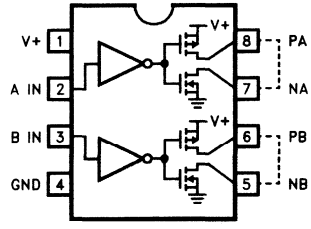
Connection Diagrams

EL7262C



7262-1

EL7272C



7262-2

EL7262C/EL7272C

Dual Channel, High Speed, Power MOSFET w/Isolated Drains

Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	−0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SOIC	670 mW
Storage Temperature Range	−65°C to +150°C	PDIP	1050 mW
Ambient Operating Temperature	−40°C to +85°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

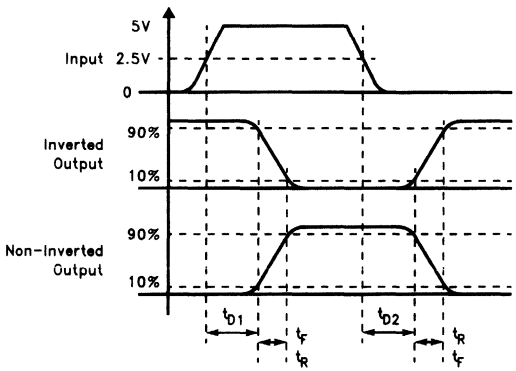
DC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
Input							
V_{IH}	Logic "1" Input Voltage		2.4			I	V
I_{IH}	Logic "1" Input Current	@V+		0.1	10	I	µA
V_{IL}	Logic "0" Input Voltage				0.8	I	V
I_{IL}	Logic "0" Input Current	@0V		0.1	10	I	µA
V_{HYS}	Input Hysteresis			0.3		V	V
Output							
R_{OH}	Pull-Up Resistance	I_{OUT} = −100 mA		3	6	I	Ω
R_{OL}	Pull-Down Resistance	I_{OUT} = +100 mA		4	6	I	Ω
I_{OFF}	Output Leakage	V_{OUT} = V+ V_{OUT} = 0V		0.2	10	I	µA
I_{PK}	Peak Output Current	Source Sink		2 2		IV	A
I_{DC}	Continuous Output Current	Source/Sink	100			I	mA
Power Supply							
I_S	Power Supply Current	Inputs EL7262 High EL7272		1 4.5	2.5 7.5	I	mA
V_S	Operating Voltage		4.5		16	I	V

AC Electrical Characteristics T_A = 25°C, V = 15V unless otherwise specified

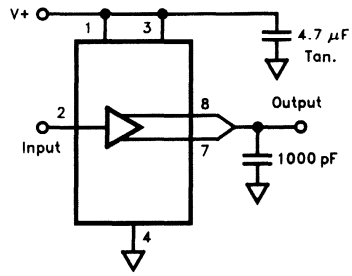
Parameter	Description	Test Conditions	Min	Typ	Max	[illegible]	Units
Switching Characteristics							
t_R	Rise Time	C_L = 500 pF C_L = 1000 pF		7.5 10	 20	[illegible]	ns
t_F	Fall Time	C_L = 500 pF C_L = 1000 pF		10 13	 20	[illegible]	ns
t_{D-ON}	Turn-On Delay Time	See Timing Table		18	25	[illegible]	ns
t_{D-OFF}	Turn-Off Delay Time	See Timing Table		20	25	[illegible]	ns

Timing Table



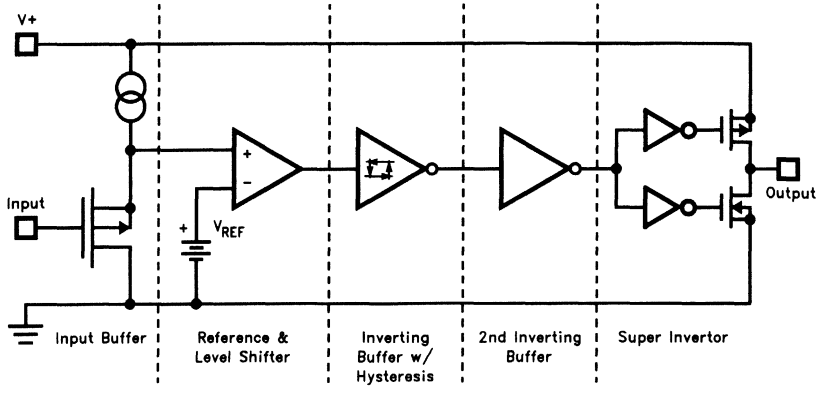
7262-3

Standard Test Configuration



7262-4

Simplified Schematic

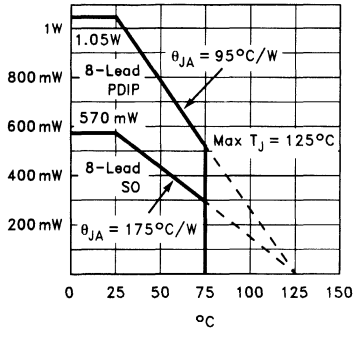


7262-5

EL7262C/EL7272C
Dual Channel, High Speed, Power MOSFET w/Isolated Drains

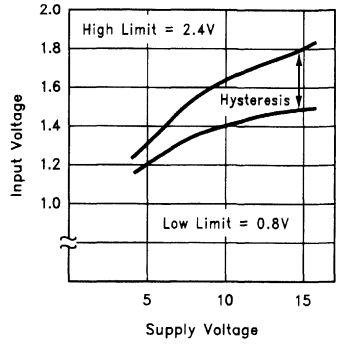
Typical Performance Curve

Max Power/Derating Curves



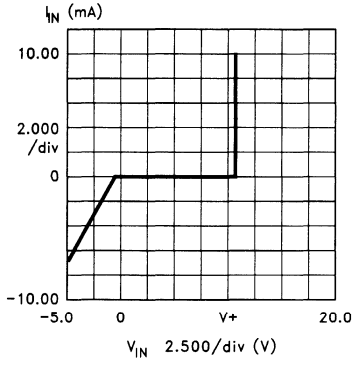
7262-12

Switch Threshold vs Supply Voltage



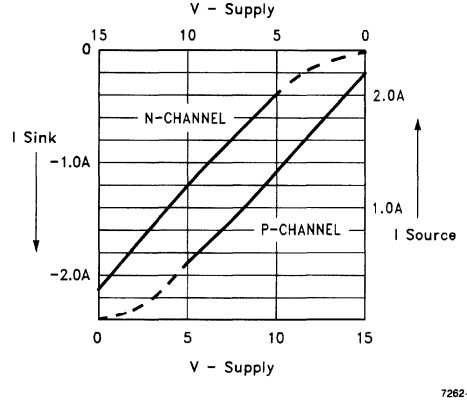
7262-6

Input Current vs Voltage



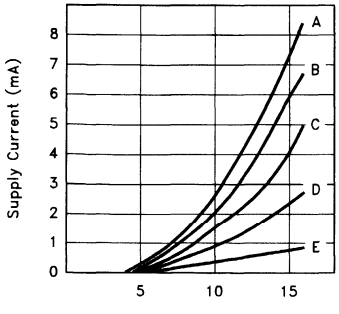
7262-7

Peak Drive vs Supply Voltage



7262-8

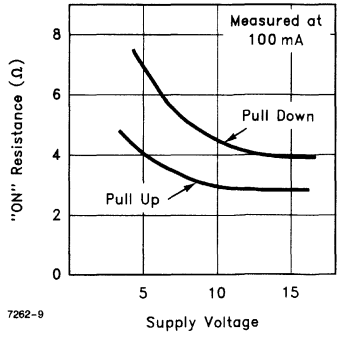
Quiescent Supply C



CASE:

Device	Input Level	Curve
EL7262	GND	C
EL7262	GND, V+	D
EL7262	V+	E
EL7272	GND	A
EL7272	GND, V+	B
EL7272	V+	C

"ON" Resistance vs Supply Voltage

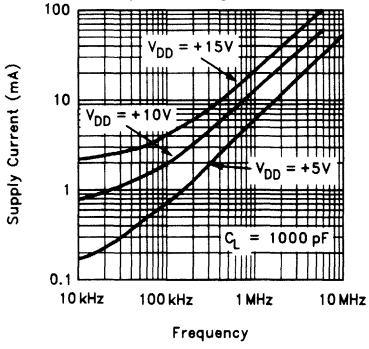


7262-9

7262-10

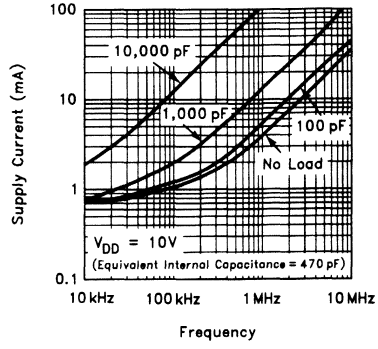
Typical Performance Curve — Contd.

Average Supply Current vs Voltage and Frequency



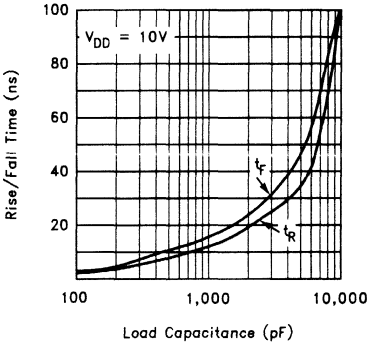
7262-13

Average Supply Current vs Capacitive Load



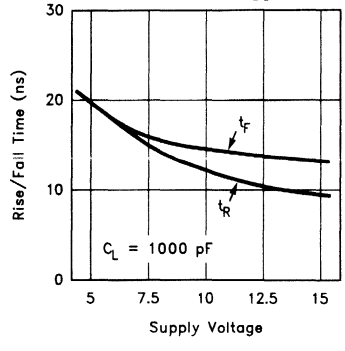
7262-14

Rise/Fall Time vs Load



7262-11

Rise/Fall Time vs Supply Voltage

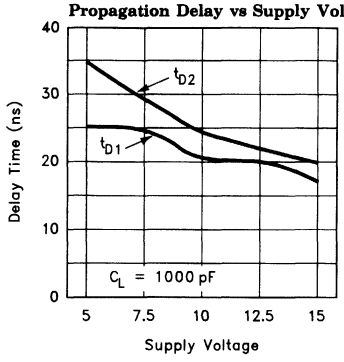


7262-15

EL7262C/EL7272C
Dual Channel, High Speed, Power MOSFET w/Isolated Drains

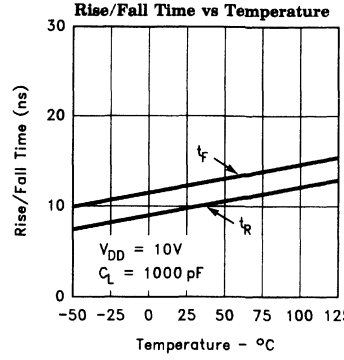
Typical Performance Curve — Contd.

Propagation Delay vs Supply Voltage



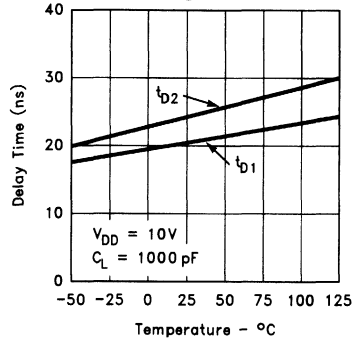
7262-16

Rise/Fall Time vs Temperature



7262-17

Delay vs Temperature



7262-18

Application Specific Video

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Video Circuits

ELANTEC Part Number	Description	Temp. Range		V_{OS} (Max)	I_b (Max)	A_{vol} R_{OL}	I_S (Max)	V_O (Min)	−3 dB BW (Typ)	SR (Typ)	dG @ 3.58 MHz	dP @ 3.58 MHz	S to H t_{PD}	Package
EL2090C	100 MHz Complete DC Restored Amplifier TTL/CMOS Restore Sig.	0°C to +75°C	Video Amp	70 mV	5 μA	56 dB	17 mA	10V	100 MHz	600 V/μs	0.01%	0.02°	N/A	14-Pin P-DIP
			S & H Amp	10 mV	2.5 μA	84 dB	—	10V	1.3 MHz	N/A	N/A	N/A	20 ns (Typ)	16-Lead SOL
EL4390C	Triple 60 MHz Video Amplifier w/DC Restore	0°C to +75°C	Video Amp	15 mV	65 μA	220 kΩ	27 mA	±12V	80 MHz	900 V/μs	0.06%	0.10°	—	16-Pin P-DIP
			S & H Amp	35 mV	5 μA	120 kΩ	—	—	4 MHz	—	—	—	25 ns	16-Pin SOL
EL4089C	Single	0°C to +75°C	Video Amp	25 mV	5 μA	220 kΩ	9 mA	±12V	60 MHz	500 V/μs	0.02%	0.03°	—	8-Pin P-DIP
			S & H Amp	7 mV	12 μA	70 dB	—	—	1.0 MHz	—	—	—	25 ns	8-Pin SO
EL4393C	Triple 60 MHz Video Amplifier	0°C to +75°C		12 mV	65 μA	217 kΩ	27 mA	±12V	70 MHz	960 V/μs	0.03%	0.088°	40 ns	16-Pin P-DIP 16-Pin SOL
EL2099C	Video Distribution Amplifier	0°C to +75°C		25 mV	25 μA	140 kΩ	45 mA	±9V	50 MHz	1000 V/μs	0.03%	0.05°	—	5-Pin TO-220

ELANTEC Part Number	Description	−3 dB BW	FPBW or Slew Rate	Gain Range	I_{OUT} or V_{OUT}	I_S	dG, dP @ 3.58 MHz	Temperature Range	Package
EL2082C	Current-Mode Variable Gain Control with Disable/Tristate	150 MHz	150 MHz	−60 to +6 dB	±4 mA	17 mA	0.05%, 0.05°	0°C to +75°C	8-Pin P-DIP 8-Lead SO
EL2082C								−55°C to +125°C	8-Pin P-DIP 8-Lead SO
EL2210C, EL2410C	Dual, Quad Video Op Amps	60 MHz	150 V/ns	1+	±2.5V	7 mA per Amplifier	0.1% 0.2°	−40°C to +85°C	8-Pin P-DIP, SO 14-Lead P-DIP, SO
EL2211C, EL2411C	Dual, Quad Video Op Amps	100 MHz	150 V/ns	2+	±2.5V	7 mA per Amplifier	0.04% 0.15°	−40°C to +85°C	8-Pin P-DIP, SO 14-Lead P-DIP, SO
EL4083C	Current-Mode 4 Quadrant Multiplier with Programmable Bias	200 MHz	170 MHz	±100%	±4 mA	4−45 mA	0.05% 0.05°	0°C to +75°C	8-Pin P-DIP 8-Lead SO
EL4084C	Current-Mode 4 Quadrant Multiplier with Programmable Bias and Emitter Coupled Disable/Tristate	200 MHz	170 MHz	±100%	±4 mA	4−45 mA	0.05% 0.05°	0°C to +75°C	14-Pin P-DIP 14-Lead SO
EL4094C	2-Input Fader/ Variable Gain Control	60 MHz	500 V/ns	0 to 1	±3V	17 mA	0.02% 0.04° @100% Gain	0°C to +75°C	8-Pin P-DIP 8-Lead SO
EL4095C	General Purpose Fader/Keyer/Variable Gain Control	60 MHz	500 V/ns	User Settable	±3V	18 mA	0.01%, 0.01° @ 100% Gain	0°C to +75°C	14-Pin P-DIP 14-Lead SO

Device	Bandwidth (MHz)	Rise and Fall Time	Gain	Package	Supply Voltage	Comments
EL5003C	200 Large-Signal 300 Small-Signal	1.5 ns	0.1–7	14-Pin P-DIP	+12V	Single Amplifier with Brightness and Contrast control (for use with DC-Coupled high-voltage stages).

ELANTEC Part Number	Description	Temperature Range	Features	Package
EL4581C	Video Sync Separator with 50% Slicing	−40°C to +85°C	Composite Sync Vertical Odd/Even Back Porch Filter 1.5 mA Supply Current	8-Pin P-DIP 8-Lead SOIC
EL4583C	Video Sync Separator with 50% Slicing and Horizontal Pulse Output	−40°C to +85°C	Independent Filter Composite Sync Vertical Back Porch Odd/Even Horizontal Out No Signal Detect Signal Level Output 2.1 mA Supply	16-Pin P-DIP 16-Lead SOIC

ELANTEC Part Number	Description	−3 dB BW	Switching Time	dG, dP @ 3.58 MHz	I_S (Max)	Package
EL4421C	2:1 Multiplexer/Amplifier, A_V = +1	85 MHz	10 ns	0.05%, 0.05°	15 mA	8-Pin P-DIP 8-Pin SO
EL4422C	2:1 Multiplexer/Amplifier, A_V = +2	80 MHz	10 ns	0.05%, 0.05°	15 mA	8-Pin P-DIP 8-Pin SO
EL4441C	4:1 Multiplexer/Amplifier, A_V = +1	85 MHz	12 ns	0.05%, 0.05°	17 mA	14-Pin P-DIP 14-Pin SO
EL4442C	4:1 Multiplexer/Amplifier, A_V = +2	80 MHz	12 ns	0.05%, 0.05°	17 mA	14-Pin P-DIP 14-Pin SO
EL4443C	4:1 Multiplexer/Amplifier with Uncommitted Inputs, A_V = +1	85 MHz	12 ns	0.05%, 0.05°	17 mA	14-Pin P-DIP 14-Pin SO
EL4444C	4:1 Multiplexer/Amplifier with Uncommitted Inputs, A_V = +2	80 MHz	12 ns	0.05%, 0.05°	17 mA	14-Pin P-DIP 14-Pin SO

The following video application specific IC's are defined, designed and tested to meet the needs of the video marketplace.

The video designer will find video amplifiers, video buffers and high speed comparators in the appropriate sections of this catalog.

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2082C
Current-Mode Multiplier

Features

- Flexible inputs and outputs, all ground referred
- 150 MHz large and small-signal bandwidth
- 46 dB of calibrated gain control range
- 70 dB isolation in disable mode @ 10 MHz
- 0.15% diff gain and 0.05° diff phase performance at NTSC using application circuit
- Operates on ±5V to ±15V power supplies
- Outputs may be paralleled to function as a multiplexer

Applications

- Level adjust for video signals
- Video faders and mixers
- Signal routing multiplexers
- Variable active filters
- Video monitor contrast control
- AGC
- Receiver IF gain control
- Modulation/demodulation
- General "cold" front-panel control of AC signals

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2082CN	0°C to +75°C	8-Pin P-DIP	*MDP0031
EL2082CS	0°C to +75°C	8-Pin SO	*MDP0027

General Description

The EL2082 is a general purpose variable gain control building block, built using an advanced proprietary complementary bipolar process. It is a two-quandrant multiplier, so that zero or negative control voltages do not allow signal feedthrough and very high attenuation is possible. The EL2082 works in current mode rather than voltage mode, so that the input impedance is low and the output impedance is high. This allows very wide bandwidth for both large and small signals.

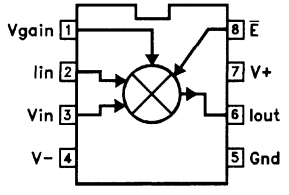
The I_{IN} pin replicates the voltage present on the V_{IN} pin; therefore, the V_{IN} pin can be used to reject common-mode noise and establish an input ground reference. The gain control input is calibrated to 1 mA/mA signal gain for 1V of control voltage. The disable pin ($\overline{E}$) is TTL-compatible, and the output current can comply with a wide range of output voltages.

Because current signals rather than voltages are employed, multiple inputs can be summed and many outputs wire-or'ed or mixed.

The EL2082 operates from a wide range of supplies and is available in standard 8-pin plastic DIP or 8-lead SO.

Connection Diagram

8-Pin DIP/SO



2082-1

Top View

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V_S^+ and V_S^-	+33V	T_{ST}	Storage Temperature	−65°C to +150°C
V_{IN}, I_{OUT}	Voltage	$\pm V_S$		Lead Temperature	
V_E, V_{GAIN}	Input Voltage	−1 to +7V		DIP Package	300°C
I_{IN}	Input Current	±5 mA		(Soldering: <10 seconds)	
P_D	Maximum Power Dissipation	See Curves		SO Package	
T_A	Operating Temperature Range	0°C to +75°C		Vapor Phase (60 seconds)	215°C
T_J	Operating Junction Temperature	150°C		Infrared (15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

(V_S = ±15V, V_G = 1V, V_E = 0.8V, V_{OUT} = 0, V_{IN} = 0, I_{IN} = 0)

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{IO}	Input Offset Voltage	Full	−20		20	II	mV
I_{OO}	Output Offset Current	Full	−100		100	II	µA
R_{INI}	I_{IN} Input Impedance; I_{IN} = 0, 0.35 mA	Full	75	95	115	II	Ω
V_{CMRR}	Voltage Common-Mode Rejection Ratio V_{IN} = −10V, +10V	Full	45	55		II	dB
I_{CMRR}	Offset Current Common-Mode Rejection Ratio, V_{IN} = −10V, +10V	Full		0.5	5	II	µA/V
V_{PSRR}	Offset Voltage Power Supply Rejection Ratio, V_S = ±5V to ±15V	Full	60	80		II	dB
I_{PSRR}	Offset Current Power Supply Rejection Ratio, V_S = ±5V to ±15V	Full		1	10	II	µA/V
I_{BVIN}	V_{IN} Bias Current	Full	−10		10	II	µA
R_{INV}	V_{IN} Input Impedance; V_{IN} = −10V, +10V	Full	0.5	1.0		II	MΩ
Nlini	Signal Nonlinearity; I_{IN} = −0.7 mA, −0.35 mA, 0 mA, +0.35 mA, +0.7 mA	Full		0.10	0.4	II	%
R_{OUT}	Output Impedance V_{OUT} = −10V, +10V	Full	0.25	0.5		II	MΩ

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EL2082C
Current-Mode Multiplier

DC Electrical Characteristics — Contd.

(V_S = ±15V, V_G = 1V, V_E = 0.8V, V_{OUT} = 0, V_{IN} = 0, I_{IN} = 0)

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OUT}	Output Swing; V_{GAIN} = 2V, I_{IN} ±2 mA, R_L = 4.0K	Full	−11		+11	II	V
V_{IOG}	V_{OS}, Gain Control, Extrapolated from V_{GAIN} = 0.1V, 1V	Full	−15		15	II	mV
A_I	Current Gain, I_{IN} ±350 μA	Full	0.9	1.0	1.1	II	mA/mA
Nling	Nonlinearity of Gain Control, V_{GAIN} = 0.1V, 0.5V, 1V	Full		2	5	II	%
I_{SO}	Input Isolation with V_{GAIN} = −0.1V	Full	−80	−96		II	dB
V_{INH}	$\overline{E}$ Logic High Level	Full	2.0			II	V
V_{INL}	$\overline{E}$ Logic Low Level	Full			0.8	II	V
I_{LH}	Input Current of $\overline{E}$, V_E = 5V	Full	−50		50	II	μA
I_{LL}	Input Current of $\overline{E}$, V_E = 0	Full	−50		50	II	μA
I_{ODIS}	I_{OUT}, Disabled $\overline{E}$ = 2.0V	Full			±1	II	μA
I_S	Supply Current	Full		13	16	II	mA

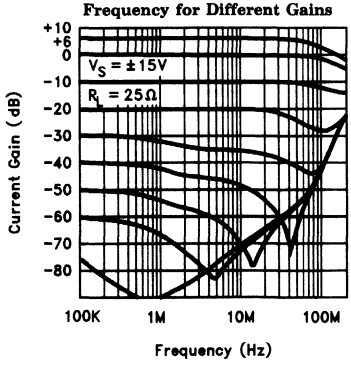
AC Electrical Characteristics

(R_L = 25Ω, C_L = 4 pF, C_{IIN} = 2 pF, T_A = 25°C, V_G = 1V, V_S = ±15V)

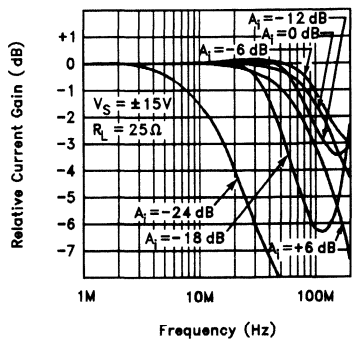
Parameter	Description	Min	Typ	Max	Test Level	Units
BW1	Current Mode Bandwidth −3 dB		150		V	MHz
BW2	±0.1 dB		30		V	MHz
BWp	Power, I_{IN} = 1 mA p-p		150		V	MHz
BWg	Gain Control Bandwidth		20		V	MHz
SRG	Gain Control Slew Rate V_G from 0.2V to 2V		12		V	(mA/mA)/μs
T_{REC}	Recovery Time from V_G < 0		250		V	ns
T_{EN}	Enable Time from $\overline{E}$ Pin		200		V	ns
T_{DIS}	Disable Time from $\overline{E}$ Pin		30		V	ns
D_G	Differential Gain, NTSC with I_{IN} = −0.35 mA to +0.35 mA		0.25		V	%
D_P	Differential Phase, NTSC with I_{IN} = −0.35 mA to +0.35 mA		0.05		V	Degree

Typical Performance Curves

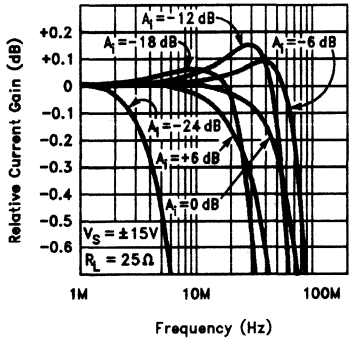
Current Gain vs Frequency for Different Gains



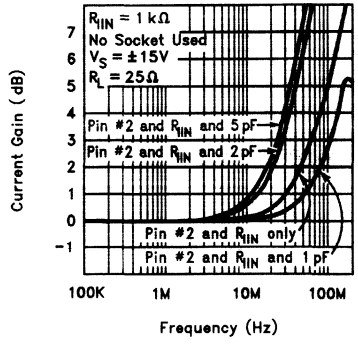
Current Gain vs Frequency



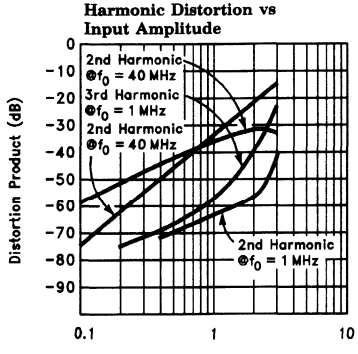
Current Gain Flatness



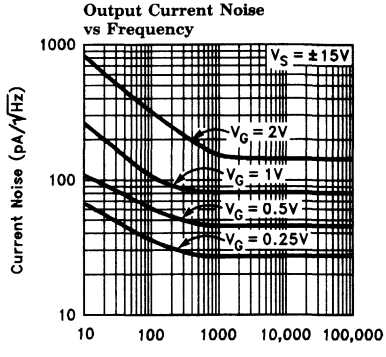
Frequency Response in Voltage Input Mode



Harmonic Distortion vs Input Amplitude



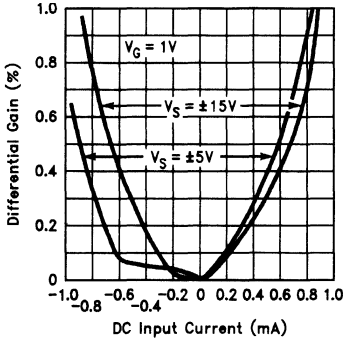
Output Current Noise vs Frequency



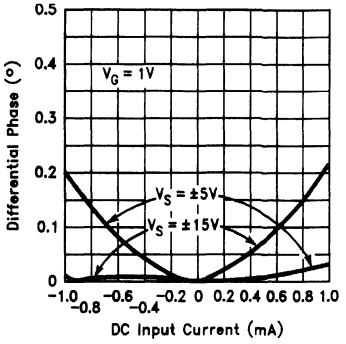
2082-2

Typical Performance Curves — Contd.

Differential Gain Error vs DC Offset Current

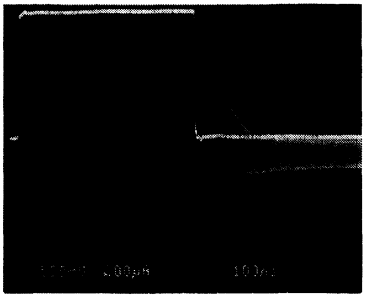


Differential Phase Error vs DC Offset Current



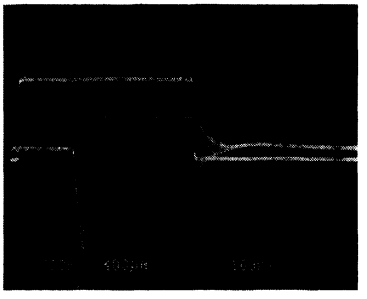
2082-3

Gain Pin Transient Response



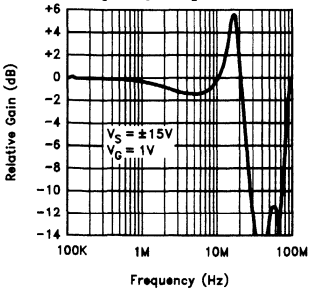
2082-4

Gain Control Recovery From Vg = −0.1V

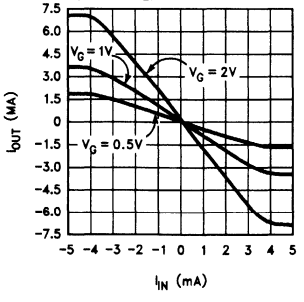


2082-5

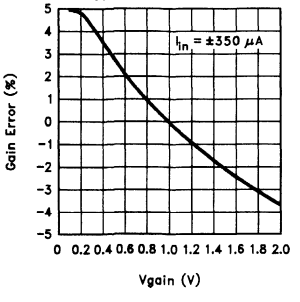
Gain Control Pin Frequency Response



I_{OUT} vs I_{IN}



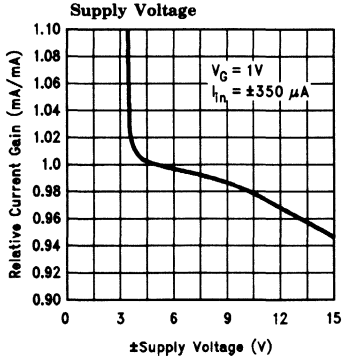
Normalized Gain Error vs V_{GAIN} Voltage



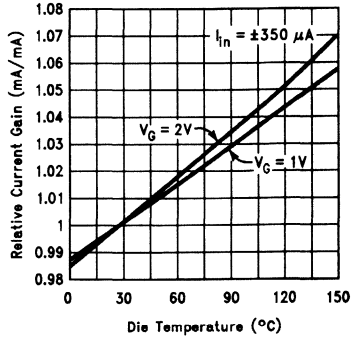
2082-6

Typical Performance Curves — Contd.

Current Gain vs Supply Voltage

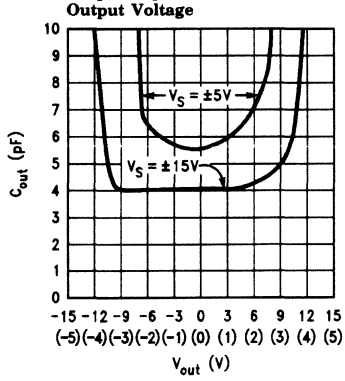


Current Gain vs Temperature



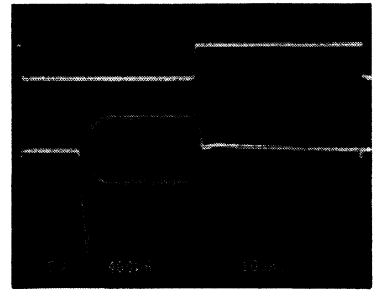
2082-7

Output Capacitance vs Output Voltage



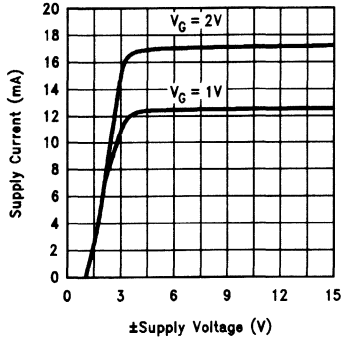
2082-8

Enable Pin Response

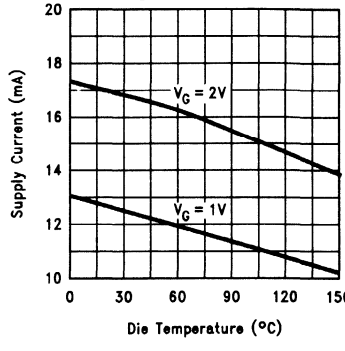


2082-9

Supply Current vs Supply Voltage



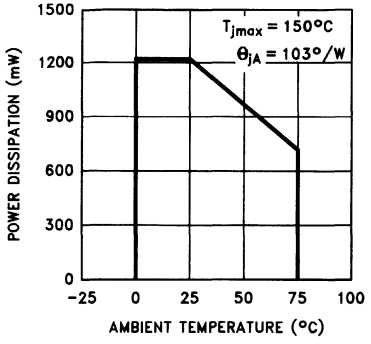
Supply Current vs Die Temperature



2082-10

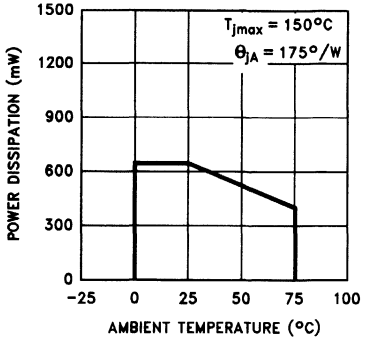
Typical Performance Curves — Contd.

8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



2082-11

8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature



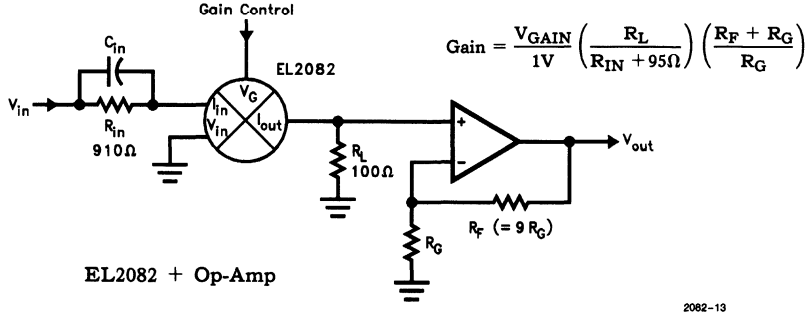
2082-12

Applications Information

The EL2082 is best thought of as a current-conveyor with variable current gain. A current input to the I_{IN} pin will be replicated as a current driven out the I_{OUT} pin, with a gain controlled by V_{GAIN}. Thus, an input of 1 mA will produce an output current of 1 mA for V_{GAIN} = 1V. An input of 1 mA will produce an output of 2 mA for V_{GAIN} = 2V. The useable V_{GAIN} range is zero to +2V. A negative level on V_{GAIN}, even only −20 mV, will yield very high signal attenuation.

The EL2082 in Conjunction with Op-Amps

This resistor-load circuit shows a simple method of converting voltage signals to currents and vice versa:



EL2082 + Op-Amp

2082-13

R_{IN} would typically be 1 kΩ for video level inputs, or 10 kΩ for ±10V instrumentation signals. The higher the value of R_{IN} (the lower the input current), the lower the distortion levels of the EL2082 will be. An approximate expression of the nonlinearity of the EL2082 is:

$$\text{Nonlinearity (\%)} = 0.3 * I_{IN}\,(\text{mA})^2$$

Optimum input current level is a tradeoff between distortion and signal-to-noise-ratio. The distortion and input range do not change appreciably with V_{GAIN} levels; distortion is set by input currents alone.

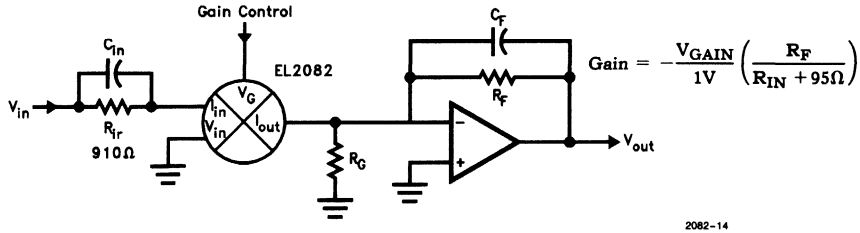
Applications Information — Contd.

The output current could be terminated with a 1 kΩ load resistor to achieve a nominal voltage gain of 1 at the EL2082, but the I_{OUT}, load, and stray capacitances would limit bandwidth greatly. The lowest practical total capacitance at I_{OUT} is about 12 pF, and this gives a 13 MHz bandwidth with a 1 kΩ load. In the above example a 100Ω load is used for an upper limit of 130 MHz. The operational amplifier gives a gain of +10 to bring the overall gain to unity. Wider bandwidth yet can be had by installing C_{IN}. This is a very small capacitor, typically 1 pf–2 pF, and it bolsters the gain above 100 MHz. Here is a table of results for this circuit used with various amplifiers:

Operational Amplifier	Power Supplies	Rf	Rg	C_{IN}	−3 dB Bandwidth	0.1 dB Bandwidth	Peaking
EL2020	±5V	620	68	—	34 MHz	5.6 MHz	0
EL2020	±15V	620	68	—	40 MHz	7.4 MHz	0
EL2130	±5V	620	68	—	73 MHz	11 MHz	1.0 dB
EL2030	±15V	620	68	—	93 MHz	12 MHz	1.3 dB
EL2090	±15V	240	27	—	60 MHz	10 MHz	0.5 dB
EL2120	±5V	220	24	—	57 MHz	10 MHz	0.4 dB
EL2120	±15V	220	24	—	65 MHz	11 MHz	0.3 dB
EL2070	±5V	200	22	2 pF	150 MHz	30 MHz	0.4 dB
EL2071	±5V	1.5K	240	2 pF	200 MHz	30 MHz	0
EL2075	±5V	620	68	2 pF	270 MHz	30 MHz	1.5 dB

Maximum bandwidth is maintained over a gain range of +6 to −16 dB; bandwidth drops at lower gains. If wider gain range with full bandwidth is required, two or more EL2082's can be cascaded with the I_{OUT} of one directly driving the I_{IN} of the next.

The EL2082 can also be used with an I ⟶ V operational circuit:



Inverting
EL2082 + Op-Amp

The circuit above gives a negative gain. The main concern of this connection involves the total I_{OUT} and stray capacitances at the amplifier's input. When using traditional op-amps, the pole caused by these capacitances can make the amplifier less stable and even cause oscillations in amplifiers whose gain-bandwidth is greater than 5 MHz. A typical cure is to add a capacitor Cf in the 2 pF–10 pF range. This will reduce overall bandwidth, so a capacitor C_{IN} can be added to regain frequency response. The ratio Cf/C_{IN} is made equal to R_{IN}/R_f.

Applications Information — Contd.

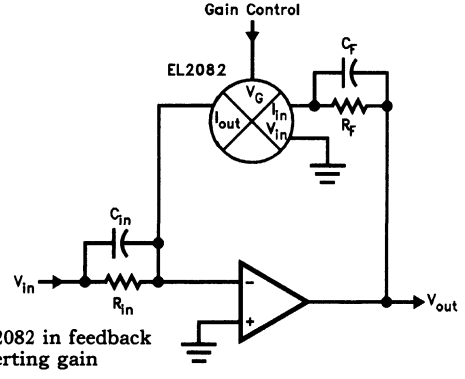
Current-feedback amplifiers eliminate this difficulty. Because their -input is a very low impedance, capacitance at the summing point of an inverting operational circuit is far less troublesome. Here is a table of results of various current-feedback circuits used in the inverting circuit:

Operational Amplifier	Power Supplies	Rf	R_{IN}	Rg	−3 dB Bandwidth	0.1 dB Bandwidth	Peaking
EL2020	±5V	1k	910	—	29 MHz	4.3 MHz	0
EL2020	±15V	1k	910	—	34 MHz	5.3 MHz	0
EL2130	±5V	1k	910	—	61 MHz	9.7 MHz	0
EL2030	±15V	1k	910	—	82 MHz	12.3 MHz	0
EL2171	±5V	2k	1.8k	1k	114 MHz	11 MHz	1.2 dB

with the EL2171 the EL2082 had ±15V supplies and the EL2171 required a 150Ω output load.

The EL2120 and EL2090 are suitable in this circuit but they are compensated for 300Ω feedback resistors. R_{IN} would have to be reduced greatly to obtain unity gain and the increased signal currents would cause the EL2082 to display much increased distortion. They could be used if the input resistor were maintained at 910Ω and Rf reduced for a $-\frac{1}{3}$ gain, or if Rf = 1k and an overall bandwidth of 25 MHz were acceptable.

The EL2082 can also be used within an op-amp's feedback loop:



EL2082 in feedback inverting gain

$$\text{Gain} = -\frac{1V}{V_{GAIN}}\left(\frac{R_F + 95\Omega}{R_{IN}}\right)$$

With voltage-mode op-amps, the same concern about capacitance at the summing node exists, so Cf and C_{IN} should be used. As before, current-feedback amplifiers tend to solve the problem. However, in this circuit the inherent phase lag of the EL2082 detracts from the phase margin of the op-amp, and some overall bandwidth reduction may result. The EL2082 appears as a 3.0 ns delay, well past 100 MHz. Thus, for a 20 MHz loop bandwidth, the EL2082 will subtract 20 MHz × 3.0 ns × 360 degrees = 21.6 degrees. The loop path should have at least 55 degrees of phase margin for low ringing in this connection. Loop bandwidth is always reduced by the ratio $R_{IN}/(R_{IN} + Rf)$ with voltage mode op-amps.

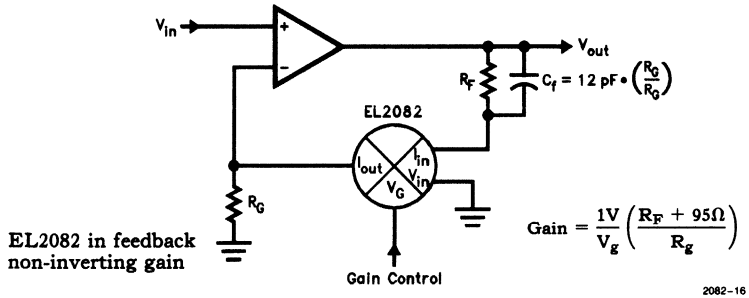
Applications Information — Contd.

Current-feedback op-amps again solve the summing-junction capacitance problem in this connection. The loop bandwidth here becomes a matter of transimpedance over frequency and its phase characteristics. Unfortunately, this is generally poorly documented in amplifier data sheets. A rule of thumb is that the transimpedance falls to the value of the recommended feedback resistor at a frequency of $F_{-3\ dB}/4$ to $F_{-3\ dB}/2$, where $F_{-3\ dB}$ is the unity-gain closed-loop bandwidth of the amplifier. The phase margin of the op-amp is usually close to 90 degrees at this frequency.

In general, Rf is initially the recommended value for the particular amplifier and is then empirically adjusted for amplifier stability at maximum V_{GAIN}, then R_{IN} is set for the overall circuit gain required. Sometimes a very small Cf can be used to improve loop stability, but it often must be in series with another resistor of value around Rf/2.

A virtue of placing the EL2082 in feedback is that the input-referred noise will drop as gain increases. This is ideal for level controls that are used to set the output to a constant level for a variety of inputs as well as AGC loops. Furthermore, the EL2082 has a relatively constant input signal amplitude for a variety of input levels, and its distortion will be relatively constant and controllable by setting Rf. Note that placing the EL2082 in the feedback path causes the circuit bandwidth to vary inversely with gain.

The next circuit shows use of the EL2082 in the feedback path of a non-inverting op-amp:



EL2082 in feedback non-inverting gain

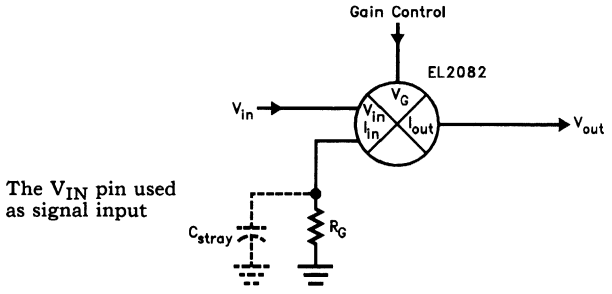
This example has the same virtues with regards to noise and distortion as the preceding circuit; and its bandwidth shrinks with increasing gain as well. The typical 12 pF sum of EL2082 output capacitance in parallel with stray capacitance necessitates the inclusion of Cf to prevent a feedback pole. Because of this 12 pF capacitance at the op-amp -input, current-feedback op-amps will generally not be useable. As before, the loop bandwidth and phase margin must accommodate the extra phase lag of the EL2082.

EL2082C
Current-Mode Multiplier

Applications Information — Contd.

Using the V_{IN} Pin

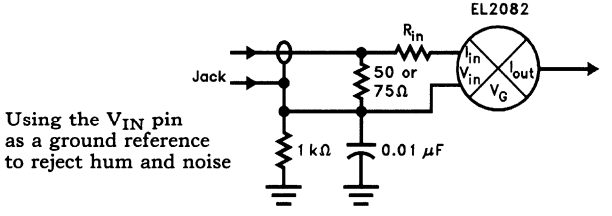
The V_{IN} pin can be used instead of the I_{IN} pin so:



$$Gm = \frac{I_{OUT}}{V_{IN}} = \frac{-Vg}{1v}\left(\frac{1}{R_g + 95\Omega}\right)$$

This connection is useful when a high input impedance is required. There are a few caveats when using the V_{IN} pin. The first is that V_{IN} has a 250 V/μs slew rate limitation. The second is that the inevitable C_{STRAY} across Rg causes a gain zero and gain INCREASES above the $1/(2\pi\ C_{STRAY}\ Rg)$ frequency and can peak as much as 20 dB with large C_{STRAY}. A graph of gain vs. frequency for several C_{STRAYS} is included in the typical performance curves. In general, if wide bandwidth and frequency flatness is desired, the I_{IN} pin should be used.

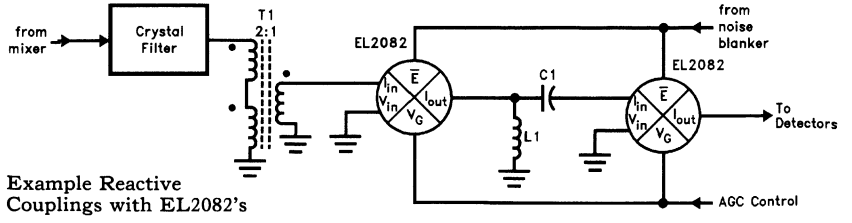
The V_{IN} pin does make an excellent ground reference pin, for instance when low-frequency noise is to be rejected. The next schematic shows the EL2082 V_{IN} pin rejecting possible 60 Hz hum induced on an RF input cable:



This example shows V_{IN} rejecting low-frequency field-induced noise but not adding peaking since the 0.01 μF bypass capacitor shunts high-frequency signals to local ground.

Reactive Couplings with the EL2082

The following sketch is an excerpt of a receiver IF amplifier showing methods of connecting the EL2082 to reactive networks:



Applications Information — Contd.

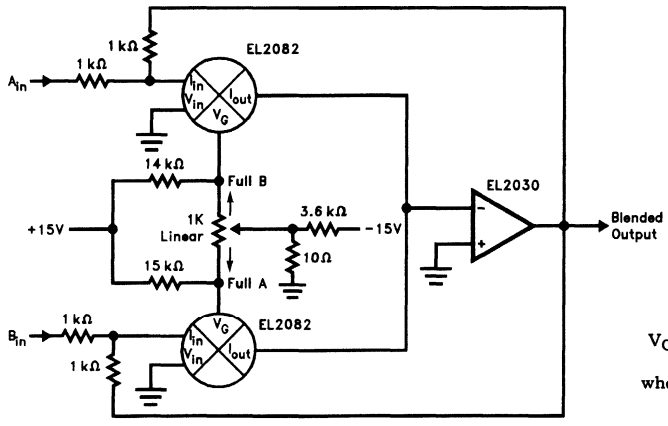
The I_{IN} pin of the EL2082 looks like 95Ω well past 100 MHz, and the output looks like a simple current-source in parallel with about 5 pF. There is no particular problem with any resistance or reactance connected to I_{IN} or I_{OUT}. The mixer output is generally sent to a crystal filter, which required a few hundred ohm terminating impedance. The impedance of the I_{IN} pin of the first EL2082 is transformed to about 400Ω by the 2:1 transformer T1. The two EL2082's are used as variable-gain IF amplifiers, with small gains offered by each. The output of the first EL2082 is coupled to the second by the resonant matching network L1–C1. For a Q of 5, Xc1 = x11 = 5 × 95Ω, approximately. The impedance seen at the first EL2082's I_{OUT} will be about $Q^2 \times 95\Omega$, or 2.5k, and by impedance transformation alone the first gain cell delivers 28 dB of gain at Vg = 1V. More gain cells can be used for a wider range of (calibrated) AGC compliance.

The $\overline{E}$ input can be used as a high-speed noise blanker gate.

Linearized Fader/Gain Control

The following circuit is an example of placing two EL2082's in the feedback network of an op-amp to significantly reduce their distortions:

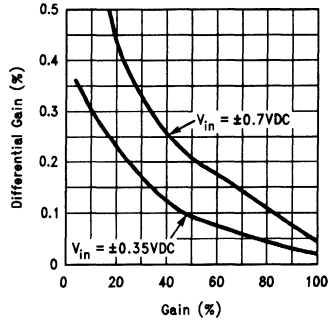
Linearized Gain Control/Fader



$V_{OUT} = K \bullet V_A + (1-K) \bullet V_B$
where $0 \le K \le 1$

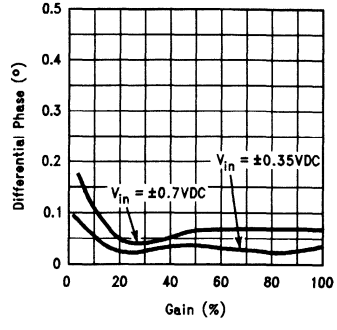
2082-20

Dual EL2082 Fader with EL2030
NTSC Differential Gain Error



2082-21

Dual EL2082 Fader with EL2030
NTSC Differential Phase Error



2082-22

Applications Information — Contd.

The circuit sums two inputs A and B, such that the sum of their respective path gains is unity, as controlled by the potentiometer. When the potentiometer's wiper is fully down, the slightly negative voltage at the Vg of the B-side EL2082 cuts off the B signal to better than 70 dB attenuation at 3.58 MHz. The A-side EL2082 is at unity gain, so the only (error) signal presented to the op-amp's -input is the same (error) signal at the I_{IN} of the A-side EL2082. The circuit thus outputs $-A_{IN}$. Since the error signal required by the op-amp is very small, even at video frequencies, the current through the A-side EL2082 is small and distortion is minimized.

At 50% potentiometer setting, equal error output signals flow from the EL2082's, since the op-amp still requires little net -input current. The EL2082's essentially buck each other to establish an output, and 50% gain occurs for both the A and B inputs. The EL2082's now contribute distortion, but less than in previous connections. The op-amp sees a constant 1k feedback resistor regardless of potentiometer setting, so frequency response is stable for all gain settings.

A single-input gain control is implemented by simply grounding B_{IN}.

Distortion can be improved by increasing the input resistors to lower signal currents. This will lower the overall gain accordingly, but will not affect bandwidth, which is dependent upon the feedback resistors. Reducing the signal input amplitude is an analagous tactic, but the noise floor will effectively rise.

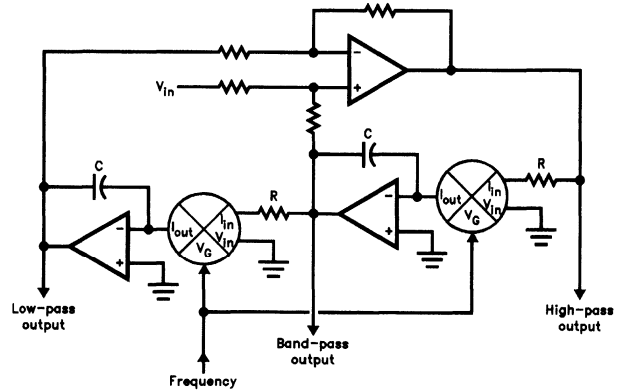
Another strategy to reduce distortion in video systems is to use DC restoration circuitry, such as the EL2090 ahead of the fader inputs to reduce the range of signals to be dealt with; the −0.7V to +0.7V possible range of inputs (due to capacitor coupling) would be changed to a stabilized −0.35V to +0.35V span.

The EL2020, EL2030, and EL2120 (at reduced bandwidth since it is compensated for 300Ω feedback resistors) all give the same video performance at NTSC operation.

Variable Filters

This circuit is the familiar state-variable configuration, similar to the bi-quad:

Voltage Tuneable Bi-Quad Filter



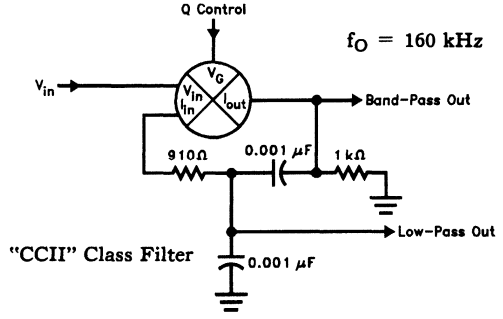
$$F_0 = \frac{Vg}{1V}\left(\frac{1}{2\pi\,(R + 95\Omega)C}\right)$$

2082-23

Applications Information — Contd.

Frequency-setting resistors R are each effectively adjusted in value by an EL2082 to effect voltage-variable tuning. Two gain controls yields a linear frequency adjustment; using one gives a square-root-of-control voltage tuning. The EL2082's could be placed in series with the integrator capacitors instead to yield a tuning proportional to 1/Vg.

The next circuit is one of a new class of "CCII" filters that use the current-conveyor element. Basic information is available in the April 1991, volume 38, number 4 edition of the IEEE Transactions on Circuits and Systems journal, pages 456 through 461 of the article "The Single CCII Biquads with High-Input Impedance", by Shen-Iuan Liu and Hen-Wai Tsao.

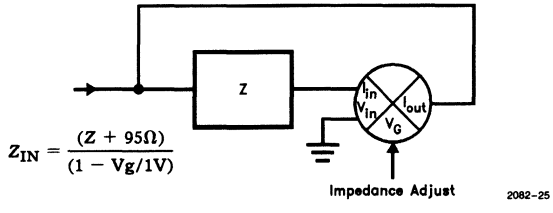


This interesting filter uses the current output of the EL2082 to generate a bandpass voltage output and the intermediate node provides a second-order low-pass filter output. Both outputs should be buffered so as not to warp characteristics, although the V_{IN} of the next EL2082 can be driven directly in the case of cascaded filters. The V_{GAIN} input acts as a Q and peaking adjust point around the nominal 1V value. The resistor at I_{OUT} could serve as the frequency trim, and Q trimmed subsequently with V_{GAIN}.

Negative Components

The following circuit converts a component or two-terminal network to a variable and even negative replica of that impedance:

Variable or Negative Impedance Converter



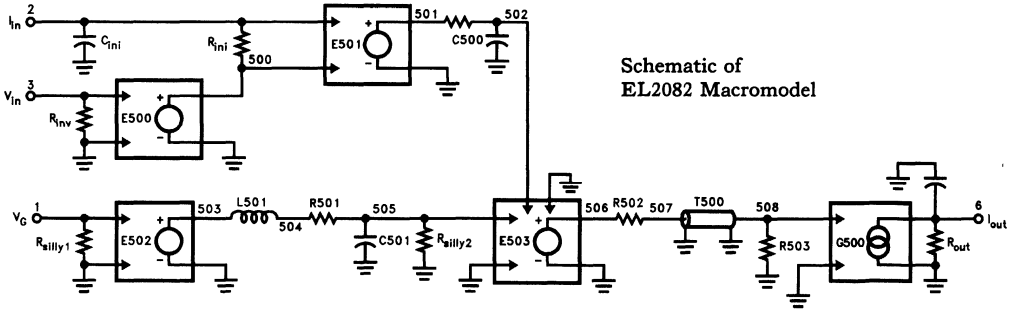
Applications Information — Contd.

A negative impedance is simply an impedance whose current flows reverse to the normal sense. In the above circuit, the current through Z is replicated by the EL2082 and inverted (I_{OUT} flows inverted to the sense of I_{IN} in the EL2082) and summed back to the input. When Vg = 0 or Vg < 0, the input impedance is simply $Z+95\Omega$. When Vg = 1V, the negative of the current through Z is summed with the input and the input impedance is "infinite". When Vg = 2V, twice the negative of the current through Z is summed with the input resulting in an input impedance of $-Z-95\Omega$.

Thus variable capacitors can be simulated by substituting the capacitor as Z. "Negative" capacitors result for Vg>1V, and capacitance needs to be present in parallel with the input to prevent oscillations. Inductors or complicated networks also work for Z, but a net negative impedance will result in oscillations.

EL2082 Macromodel

This macromodel has been designed to work with PSPICE (copywritten by the Microsim Corporation). E500 buffers in the V_{IN} voltage and presents it to the R_{INI} resistor to emulate the I_{IN} pin. E501 supplies the non-linearity of the current channel and replicates the I_{IN} current to a ground referenced voltage. R500 and C500 provide the bandwidth limitation on the current signal. E502 supplies the V_{GAIN} non-linearity and drives the L501/R501/C501 to shape the gain control frequency response. E503 does the actual gain-control multiplication, and drives delay line T500 to better simulate the actual phase characteristics of the part G500 creates the current output, and R_{OUT} with C_{OUT} provide proper output parasitics.



Schematic of
EL2082 Macromodel

The model is good at frequency and linearity estimates around Vg = 1V and nominal temperatures, but has several limitations:

The Vg channel does not give zero gain for Vg < 0; the output gain reverses–don't use Vg < 0
The Vg channel is not slew limited
Frequency response does not vary with supply voltage
The V_{IN} channel is not slew limited
Noise is not modeled
Temperature effects are not modeled
CMRR and PSRR are not modeled
Frequency response does not vary with Vg

Unfortunately, the polynomial expressions and two-input multiplication may not be available on every simulator. Results have been confirmed by laboratory results in many situations with this macromodel, within its capabilities.

EL2082 Macromodel

```
*:                          Vgain
*                           |    Iin
*                           |    |    Vin
*                           |    |    |                Iout
*                           |    |    |                |
.SUBCKT EL2082macro  (1     2    3    4    5    6    7    8)
***
*** I-to-I gain cell macromodel ***
***
******
Cini 2 0 2P
C500 502 0 0.9845P
C501 505 0 1000P
Cout 6 0 5P
******
L501 503 504 0.1U
******
Rsilly1 1 0 1E9
Rsilly2 505 0 1E9
Rini 2 500 95
Rinv 3 0 2Meg
Rout 6 0 1Meg
R500 501 502 1000
R501 504 505 5
R502 506 507 50
R503 508 0 50
******
E500 500 0 3 0 1
E501 501 0 POLY(1) (2,500) 0 2  0 -.8
E502 503 0 POLY(1) (1,0) 0 1.05 -.05
E503 506 0 POLY(2) (505,0) (502,0) 0 0 0 0 1
G500 6 0 508 0 -0.0105
T500 508 0 507 0 Z0=50 TD=1.95N
******
.ENDS
```

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2090C
100 MHz DC-Restored Video Amplifier

Features

- Complete video level restoration system
- 0.01% differential gain and 0.02° differential phase accuracy at NTSC
- 100 MHz bandwidth
- 0.1 dB flatness to 20 MHz
- Sample-and-hold has 15 nA typical leakage and 1.5 pC charge injection
- System can acquire DC correction level in 10 μs, or 5 scan lines of 2 μs each, to ½ IRE
- V_S = ±5V to ±15V
- TTL/CMOS hold signal

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2090CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2090CM	0°C to +75°C	16-Lead SOL	MDP0027

General Description

The EL2090C is the first complete DC-restored monolithic video amplifier sub-system. It contains a very high-quality video amplifier and a nulling sample-and-hold amplifier specifically designed to stabilize video performance. When the HOLD logic input is set to a logic 0 during a horizontal sync, the sample-and-hold amplifier may be used as a general-purpose op-amp to null the DC offset of the video amplifier. When the HOLD input goes to a logic 1 the sample-and-hold stores the correction voltage on the hold capacitor to maintain DC correction during the subsequent scan line.

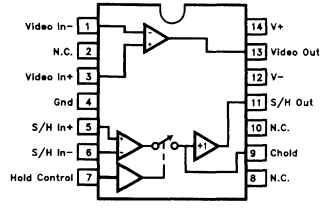
The video amplifier is optimized for video characteristics, and performance at NTSC is nearly perfect. It is a current-feedback amplifier, so that −3 dB bandwidth changes little at various closed-loop gains. The amplifier easily drives video signal levels into 75Ω loads. With 100 MHz bandwidth, the EL2090 is also useful in HDTV applications.

The sample-and-hold is optimized for fast sync pulse response. The application circuit shown will restore the video DC level in five scan lines, even if the HOLD pulse is only 2 μs long. The output impedance of the sample-and-hold is low and constant over frequency and load current so that the performance of the video amplifier is not compromised by connections to the DC restore circuitry.

The EL2090C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL2090C is specified for operation over the 0°C to 75°C temperature range.

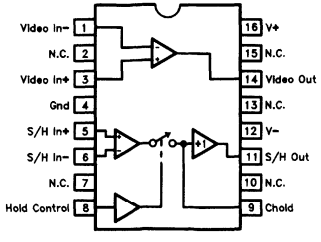
Connection Diagrams

14-Pin DIP Package



2090-1

16-Pin SOL Package



2090-2

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Operating Junction Temperature	
Voltage between V_{IN}+, S/H_{IN}+,		Plastic DIP or SOL	150°C
S/H_{IN}−, C_{HOLD}, and GND pins	(V+) + 0.5V to (V−) −0.5V	Storage Temperature Range	−65°C to +150°C
		Lead Temperature	
V_{OUT} Current	60 mA	DIP Package	
Current into V_{IN}− and HOLD Pins	5 mA	(Soldering, <10 seconds)	300°C
Current S/H_{OUT}	16 mA	SOL Package	
Internal Power Dissipation	See Curves	Vapor Phase (<60 seconds)	215°C
Operating Ambient Temperature Range	0°C to 75°C	Infrared (< 15 seconds)	220°C

Important Note

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level — **Test Procedure**

I — 100% production tested and QA sample tested per QA test plan QCX2002.

II — 100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX2002.

III — QA sample tested per QA test plan QCX2002.

IV — Parameter is guaranteed (but not tested) by Design and Characterization Data.

V — Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V; R_L = 150Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_S	Total Supply Current	Full		14	17	II	mA
Video Amplifier Section (Not Restored)							
V_{OS}	Input Offset Voltage	Full		8	70	II	mV
I_{B+}	$+V_{IN}$ Input Bias Current	Full		2	15	II	µA
I_{B-}	$-V_{IN}$ Input Bias Current	Full		30	150	II	µA
R_{OL}	Transimpedance	25°C		300		V	V/mA
A_{VOL}	Open-Loop Voltage Gain; V_{OUT} = ±2V	Full	56	65		II	dB
V_O	Output Voltage Swing V_S = ±15V; R_L = 2 kΩ	Full	±12	±13		II	V
	V_S = ±5V; R_L = 150Ω	Full	±3.0	±3.5		II	V
I_{SC}	Short-Circuit Current; $+V_{IN}$ Set to ±2V; $-V_{IN}$ to Ground through 1 kΩ	25°C	±50	±90	±160	II	mA
Sample-And-Hold Section							
V_{OS}	Input Offset Voltage	Full		2	10	II	mV
I_B	Input Bias Current	Full		0.5	2.5	II	µA
I_{OS}	Input Offset Current	Full		0.05	0.5	II	µA
$R_{IN, DIFF}$	Input Differential Resistance	25°C		200		V	kΩ
$R_{IN, COMM}$	Input Common-Mode Resistance	25°C		100		V	MΩ
V_{CM}	Common-Mode Input Range	Full	±11	±12.5		II	V

4

EL2090C
100 MHz DC-Restored Video Amplifier

Open Loop DC Electrical Characteristics

V_S = ±15V; R_L = 150Ω, T_A = 25°C unless otherwise specified — Contd.

Parameter	Description	Temp.	Min	Typ	Max	Test Level	Units
Sample-And-Hold Section — Contd.							
A_{VOL}	Large Signal Voltage Gain	Full	15k	50k		II	V/V
CMRR	Common-Mode Rejection Ratio V_{CM} = ±11V	Full	75	95		II	dB
PSRR	Power-Supply Rejection Ratio V_S = ±5V to ±15V	Full	75	95		II	dB
V_{thresh}	HOLD Pin Logic Threshold	Full	0.8	1.4	2.0	II	V
I_{droop}	Hold Mode Droop Current	Full		10	50	II	nA
I_{charge}	Charge Current Available to Chold	Full	±90	±135		II	µA
V_O	Output Swing; R_L = 2k	Full	±10	±13		II	V
I_{SC}	Short-Circuit Current	25°C	±10	±17	±40	II	mA

Closed Loop AC Electrical Characteristics

V_S = ±15V; C_L = 15 pF; C_{stray} ($-V_{IN}$) = 2.5 pF; R_F = R_G = 300Ω; R_L = 150Ω; C_{hold} = 100 pF; T_A = 25°C

Parameter	Description	Min	Typ	Max	Test Level	Units
Video Amplifier Section						
SR	SlewRate; V_{OUT} from −2 to +2V		600		V	V/µs
BW	Bandwidth; −3 dB ±1 dB ±0.1 dB	75 35 10	100 60 20		III III III	MHz MHz MHz
Peaking dG	Differential Gain; V_{IN} from −0.7V to 0.7V; F = 3.58 MHz		0.01		V	%
dθ	Differential Phase; V_{IN} from −0.7V to 0.7V; F = 3.58 MHz		0.02		V	°
Sample-And-Hold Section						
BW	Gain-Bandwidth Product		1.3		V	MHz
ΔQ	Sample to Hold Charge Injection (Note 1)		1.5	5	III	pC
ΔT	Sample to Hold or Hold to Sample Delay Time		20		V	ns
T_s	Sample to Hold Settling Time to 2 mV		200		V	ns

Note 1: The logic input is between 0V and 5V, with a 220Ω resistor in series with the HOLD pin and 39 pF capacitor from HOLD pin to ground.

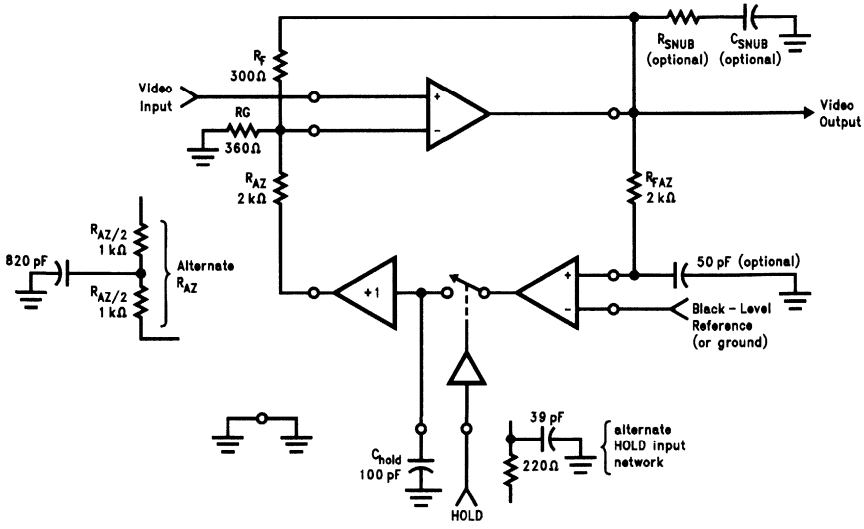
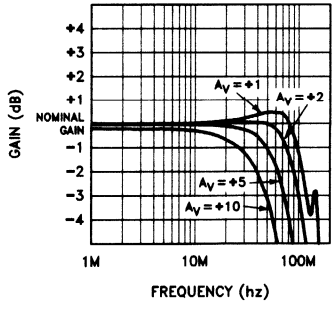


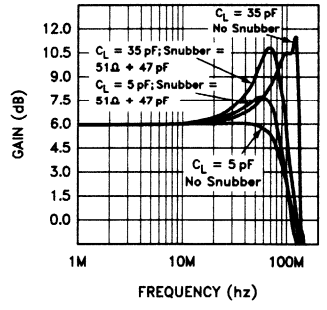
Figure 1. Typical Application (A_V = +2)

Typical Performance Curves

Relative Frequency Response for Various Gains

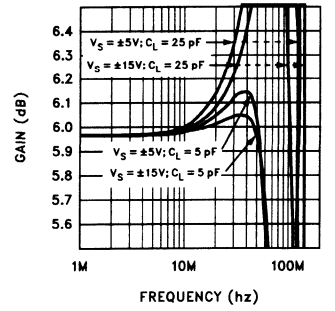


Frequency Response with Different Loads (A_V = +2)

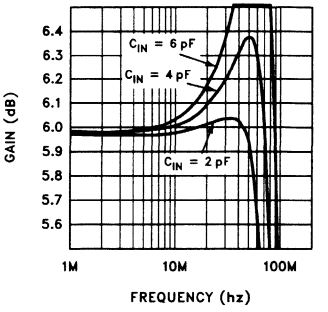


2090-4

Frequency Response Flatness for Various Load and Supply Conditions



Frequency Response Flatness vs C_{IN}−, A_V = +2



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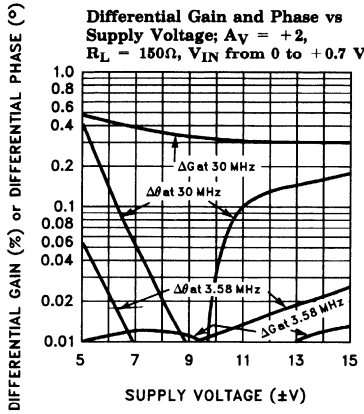
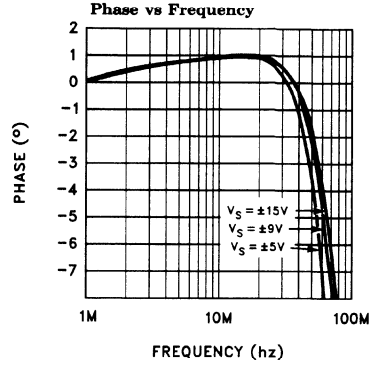
EL2090C
100 MHz DC-Restored Video Amplifier

Typical Performance Curves — Contd.

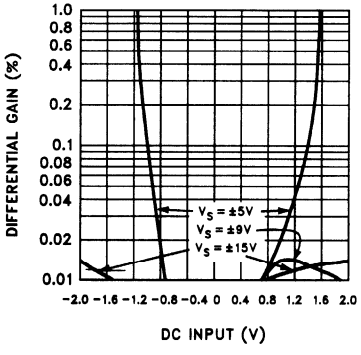
Differential Gain and Phase vs Supply Voltage; A_V = +2, R_L = 150Ω, V_{IN} from 0 to +0.7 V_{DC}



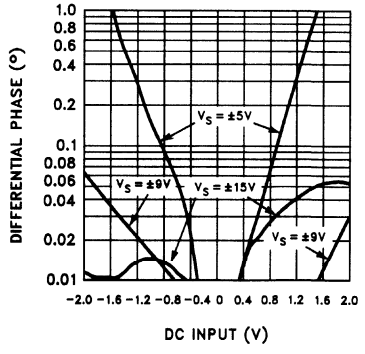
Deviation from Linear Phase vs Frequency



Differential Gain vs DC Input Offset; A_V = +2, F_O = 3.58 MHz, R_L = 150Ω

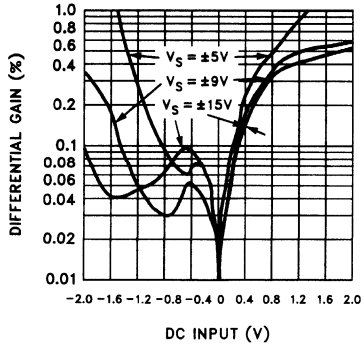


Differential Phase vs DC Input Offset; A_V = +2, F_O = 3.58 MHz, R_L = 150Ω

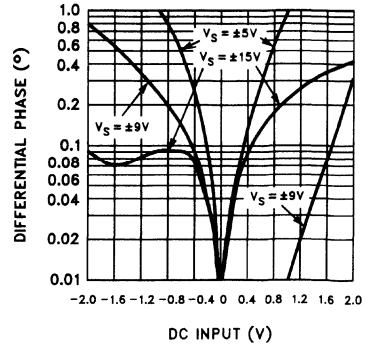


2090-12

Differential Gain vs DC Input Offset; A_V = +2 and F_O = 30 MHz, R_L = 150Ω



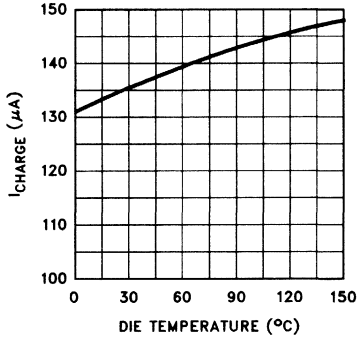
Differential Phase vs DC Input Offset; A_V = +2, F_O = 30 MHz, R_L = 150Ω



2090-6

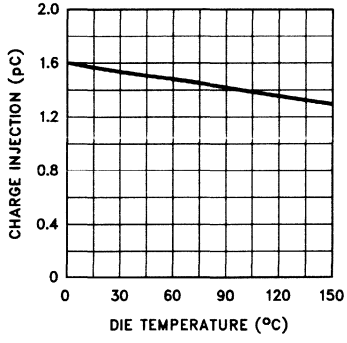
Typical Performance Curves — Contd.

S/H Available Charge Current vs Temperature

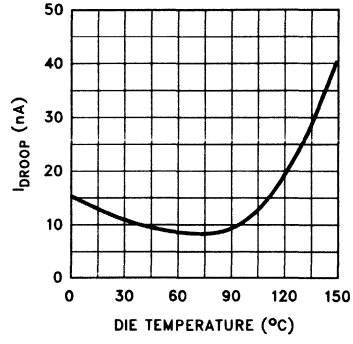


2090-7

Sample-to-Hold Change Injection vs Temperature

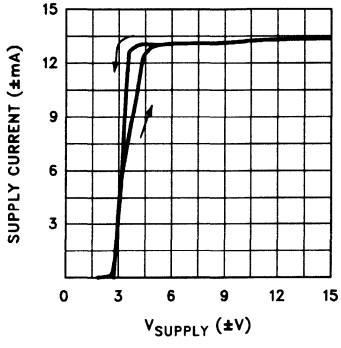


Typical Droop Current vs Temperature, V_S = ±15V

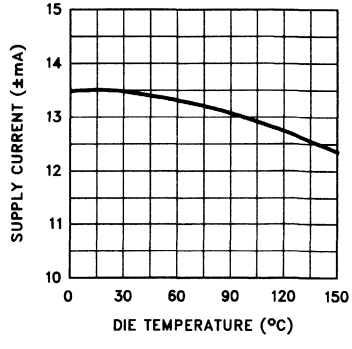


2090-8

Supply Current vs Supply Voltage



Supply Current vs Temperature; V_S = ±15V



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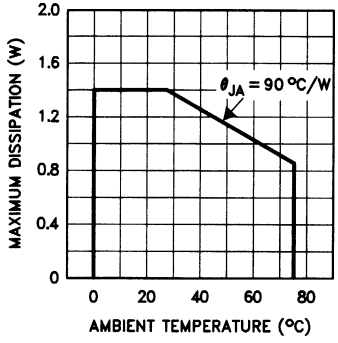
EL2090C
100 MHz DC-Restored Video Amplifier

Typical Performance Curves — Contd.

Maximum Power Dissipation vs Ambient Temperature— 14-Pin PDIP and 16-Pin SOL



Applications Information

The EL2090C is a general purpose component and thus the video amplifier and sample-and-hold pins are uncommitted. Therefore much of the ultimate performance as a DC-restored video amplifier will be set by external component values and parasitics. Some application considerations will be offered here.

The DC feedback from the sample-and-hold can be applied to either positive or negative inputs of the video amplifier (with appropriate phasing of the sample-and-hold amplifier inputs). We will consider feedback to the inverting video input. During a sample mode (the HOLD input at a logic low), the sample-and-hold acts as a simple nulling op-amp.

Ideally, the DC feedback resistor Raz is a high value so as not to couple a large amount of the AC signal on the video input back to the sample-and-hold amplifier output. The sample-and-hold output is a low impedance at high frequencies, but variations of the DC operating point will change the output impedance somewhat. No more than a few ohms output impedance change will occur, but this can cause gain variations in the 0.01% realm. This DC-dependent gain change is in fact a differential gain effect. Some small differential phase error will also be added. The best approach is to maximize the DC feedback resistor value so as to isolate the sample-and-hold from the video path as much as possible. Values of 1 kΩ or above for Raz will cause little to no video degradation.

This suggests that the largest applicable power supply voltages be used so that the output swing of the sample-and-hold can still correct for the variations of DC offset in the video input with large values of Raz. The typical application circuit shown will allow correction of ±1V inputs with good isolation of the sample-and-hold output. Good isolation is defined as no video degradation due to the insertion of the sample-and-hold loop. Lower supply voltages will require a smaller value of DC feedback resistor to retain correction of the full input DC variation. The EL2090 differential phase performance is optimum at ±9V supplies, and differential gain only marginally improves above this voltage. Since all video characteristics mildly degrade with increasing die temperature, the ±9V levels are somewhat better than ±15V supplies. However, ±15V supplies are quite usable.

Ultimate video performance, especially in HDTV applications, can also be optimized by setting the black-level reference such that the signal span at the video amplifier's output is set to its optimum range. For instance, setting the span to ±1V of output is preferable to a span of 0V to +2V. The curves of differential gain and phase versus input DC offset will serve as guides.

The DC feedback resistor may be split so that a bypass capacitor is added to reduce the initially small sample-and-hold transients to even smaller levels. The corruption can be reduced to as low as 1 mV peak seen at the video amplifier output. The size of the capacitor should not be so large as to de-stabilize the sample-and-hold feedback loop, nor so small as to reduce the video amplifier's gain flatness. A resistor or some other video isolation network should be inserted between the video amplifier output and the sample-and-hold input to prevent excessive video from bleeding through the autozero section, as well as preventing spurious DC correction due to video signals confusing the sample-and-hold during autozero events. Figure 1 shows convenient component values. A full 3.58 MHz trap is not necessary for suppressing NTSC chroma burst interaction with the sample-and-hold input; the simple R-C network suggested in Figure 1 suffices.

Applications Information — Contd.

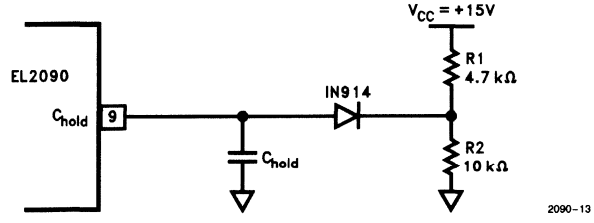
The HOLD input to the sample-and-hold has a 1.4V threshold and is clamped to a diode below ground and 6V above ground. The hold step characteristics are not sensitive to logic high nor low levels (within TTL or CMOS swings), but logic slewrates greater than 1000V/μs can couple noise and hold step into the sample-to-hold output waveforms. The logic slewrate should be greater than 50V/μs to avoid hold jitter. To avoid artificially high droop in hold mode, the Chold pin and Chold itself should be guarded with circuit board traces connected to the output of the sample-and-hold. Low-leakage hold capacitors should be used, such as mica or mylar, but not ceramic. The excellent properties of more expensive polystyrene, polypropylene, or teflon capacitors are not needed.

The user should be aware of a combination of conditions that may make the EL2090 operate incorrectly upon power-up. The fault condition can be described by noticing that the sample-and-hold output (pin 11) appears locked at a voltage close to V_{CC}. This voltage is maintained regardless of changes at the inputs to the sample-and-hold (pins 5 and 6) or to the HOLD control input (pin 7). Two conditions must occur to bring this about:

1. A large value of Chold—usually values of 1000 pF or more. This is not an unusual situation. Many users want to reduce the size of the hold step and increasing Chold is the most direct way to do this. Increasing Chold also reduces the slew rate of the sample and hold section but because of the limited size of the video signal, this is usually not a limitation.
2. A sampling interval (dictated by the HOLD pin) that is too small. By small, we mean less than 2 μs.

For a sampling interval that is wide enough, there is enough time for the loop to close and for the amplifier to discharge whatever charge was dumped onto Chold it during the initial power spike and to then ramp up (or down) to the voltage that is proper for a balanced loop. When the sampling interval is too small, there is insufficient time for internal devices to recover from their initial saturated state from power-up because the feedback is not closed long enough. Therefore, typical recovery times for the loop are 2 μs or greater. Summarizing, the two things that could prevent proper saturation recovery are (as mentioned above) too large a capacitor which slows the charge and discharge rate of the stored voltage at Chold and too small a sampling interval in which the entire feedback loop is closed.

The circuit shown below prevents the fault condition from occurring by preventing the node from ever saturating. By clamping the value of Chold to some value lower than the supply voltage less



EL2090C
100 MHz DC-Restored Video Amplifier

Applications Information — Contd.

a saturation voltage, we prevent this node from approaching the positive rail. The maximum voltage is set by the resistive voltage divider (between V+ and GND) R1 and R2 plus a diode. This value can be adjusted if the maximum size of the input signal is known. The diode used is an off-the-shelf 1N914 or 1N916.

As is true of all 100 MHz amplifiers, good bypassing of the supplies to ground is mandatory. 1 μF tantalums are sufficient, and 0.01 μF leaded chip capacitors in parallel with medium value electrolytics are also good. Leads longer than $\frac{1}{2}$ can induce a characteristic 150 MHz resonance and ringing.

The V_{IN-} of the video amplifier should have the absolute minimum of parasitic capacitance. Stray capacitance of more than 3 pF will cause peaking and compromise the gain flatness. The bandwidth of the amplifier is fundamentally set by the value of Rf. As demonstrated by the frequency response versus gain graph, the peaking and bandwidth is a weak function of gain. The EL2090 was designed for Rf = 300Ω giving optimum gain flatness at Av = +2. Unity-gain response is flattest for Rf = 360Ω; gains of +5 can use Rf = 270Ω. In situations where the peaking is accentuated by load capacitance or −input capacitance the value of Rf will have to be increased, and some bandwidth will be sacrificed.

The V_{IN+} of the video amplifier should not look into an inductive source impedance. If the source is physically remote and a terminated input line is not provided, it may be necessary to connect an input "snubber" to ground. A snubber is a resistor in series with a capacitor which de-Q's the input resonance. Typical values are 100Ω and 30 pF.

The output of the video amplifier is sensitive to capacitive loads greater than 25 pF, and a snubber to ground or a resistor in series with the output is useful to isolate reactive loads.

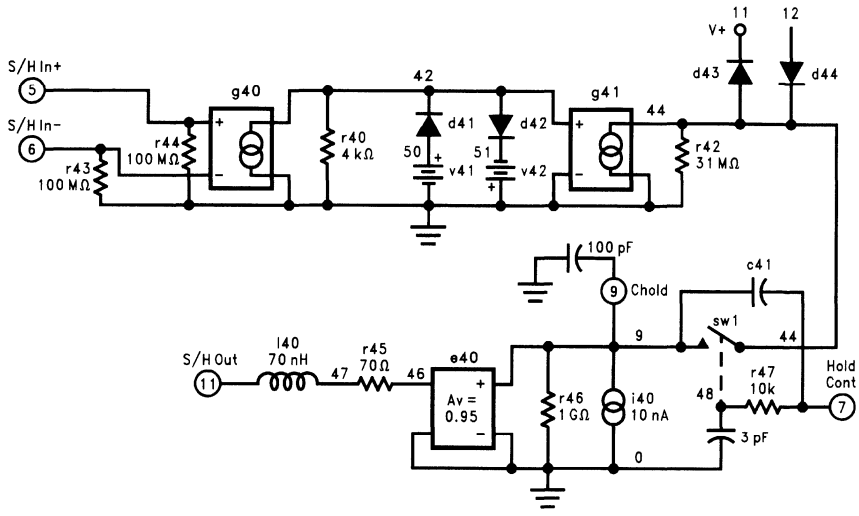
EL2090 Macromodel

```
* Revision A, October 1992
.param vclamp = {-0.002 * (TEMP-25)}
*
* Connections:      Vidin+
*                   |   Vidin-
*                   |   |   +Vsupply
*                   |   |   |   -Vsupply
*                   |   |   |   |   Vid Out
*                   |   |   |   |   |   S/H In+
*                   |   |   |   |   |   |   S/H In-
*                   |   |   |   |   |   |   |   S/H Out
*                   |   |   |   |   |   |   |   |   Hold Control
*                   |   |   |   |   |   |   |   |   |   Chold
*                   |   |   |   |   |   |   |   |   |   |
.subckt EL2090/EL   3   1   14  12  13  5   6   11  7   9
*
******** Video Amplifier ********************
*
e1 20 0 3 0 1.0
vis 20 34 0V
h2 34 38 vxx 1.0
r10 1 36 25
l1 36 38 20nH
iinp 3 0 10µA
iinm 1 0 5µA
h1 21 0 vis 600
r2 21 22 1K
d1 22 0 dclamp
d2 0 22 dclamp
e2 23 0 22 0 0.00166666666
l5 23 24 0.7µH
c5 24 0 0.5pF
r5 24 0 600
g1 0 25 24 0 1.0
rol 25 0 400K
cdp 25 0 7.7pF
q1 12 25 26 qp
q2 14 25 27 qn
q3 14 26 28 qn
q4 12 27 29 qp
r7 28 13 4
r8 29 13 4
ios1 14 26 2.5mA
ios2 27 12 2.5mA
ips 14 12 7.2mA
ivos 0 33 5mA
vxx 33 0 0V
r11 33 0 1K

********** Sample & Hold **************************
*
g40 49 0 5 6 1e-3
vcur 49 42 0v
r43 6 0 100Meg
r44 5 0 100Meg
r40 42 0 4K
d41 50 42 diode
d42 42 51 diode
v41 50 0 {vclamp}
v42 0 51 {vclamp}
g41 44 0 42 0 200e-6
r42 44 0 31Meg
d45 9 14 diode
d46 12 9 diode
s1 44 9 48 0 swa
e40 46 0 9 0 0.95
i40 0 9 10nA
r45 46 47 70
l40 47 11 70nH
c40 7 9 0.32pF
r47 7 48 10K
c41 48 0 3pF
*
* Models
*
.model qn npn(is=5e-15 bf=500 tf=0.1nS)
.model qp pnp(is=5e-15 bf=500 tf=0.1nS)
.model dclamp d(is=1e-30 ibv=0.02 bv=2.75 n=4)
.model diode d
.model swa vswitch(von=1.2v voff=1.6v roff=1e12 ron=100)
.ends
```

EL2090C
100 MHz DC-Restored Video Amplifier

EL2090 Macromodel — Contd.



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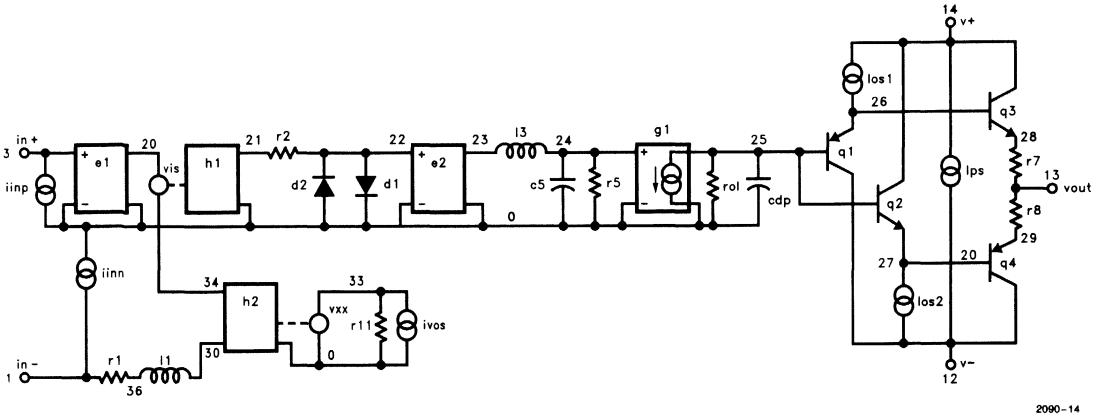
Sample and Hold Amplifier

EL2090 Macromodel — Contd.



Video Amplifier

4

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2099C
Video Distribution Amplifier

Features

- 50 MHz −3 dB bandwidth, $A_V = +2$
- Differential gain 0.03%
- Differential phase 0.05°
- Output short circuit current 800 mA
- Can drive six 75Ω double terminated cables ±11V
- Slew rate = 1000V/μs
- Wide supply voltage range ±5V to ±15V

Applications

- Video line driver
- ATE pin driver
- High speed data acquisition

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2099CT	0°C to +75°C	5-Pin TO-220	MDP0028

General Description

The EL2099C is a high speed, monolithic operational amplifier* featuring excellent video performance and high output current capability. Built using Elantec's Complementary Bipolar process, the EL2099C uses current mode feedback to achieve wide bandwidth, and is stable in unity gain configuration.

Operation from power supplies ranging from ±5V to ±15V makes the EL2099C extremely versatile. With supplies at ±15V, the EL2099C can deliver ±11V into 25Ω at slew rates of 1000V/μs. At ±5V supplies, output voltage range is ±3V into 25Ω. Its speed and output current capability make this device ideal for video line driver and automatic test equipment applications.

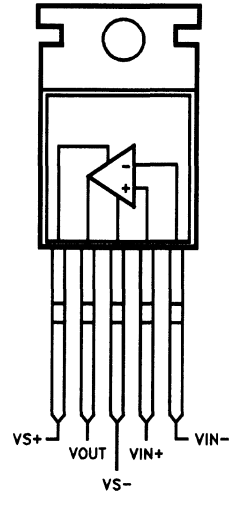
Differential Gain and Phase of the EL2099C are 0.03% and 0.05° respectively, and −3 dB bandwidth is 50 MHz. These features make the EL2099C especially well suited for video distribution applications.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits.*

*U.S. Patent #5,179,355

Connection Diagram

5-Pin TO-220



Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S+ and V_S-	+33V	Internal Power Dissipation	See Curves
Voltage at V_S+	+16.5V	Operating Ambient Temperature Range	0°C to +75°C
Voltage at V_S-	−16.5V	Operating Junction Temperature	150°C
Voltage between $V_{IN}+$ and $V_{IN}-$	±6V	Storage Temperature Range	−65°C to +150°C
Current into $V_{IN}+$ or $V_{IN}-$	±10 mA	Lead Temperature (Soldering, <10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, R_L = 25Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	25°C		5	20	I	mV
		T_{MIN}, T_{MAX}			25	IV	mV
TC V_{OS}	Average Offset Voltage Drift	Full		20		V	µV/°C
$+I_{IN}$	+Input Current	25°C		5	15	I	µA
		T_{MIN}, T_{MAX}			25	IV	µA
$-I_{IN}$	−Input Current	25°C		8	35	I	µA
		T_{MIN}, T_{MAX}			50	IV	µA
CMRR	Common Mode Rejection Ratio (Note 1)	25°C	50	60		I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	25°C	60	70		I	dB
R_{OL}	Transimpedance	25°C	85	140		I	kΩ
$+R_{IN}$	+Input Resistance (Note 3)	25°C	700	1000		I	kΩ
		T_{MIN}, T_{MAX}	600			IV	kΩ
$+C_{IN}$	+Input Capacitance	25°C		3		V	pF
CMIR	Common Mode Input Range	25°C		±12.5		V	V

EL2099C
Video Distribution Amplifier

Open Loop DC Electrical Characteristics — Contd.

V_S = ±15V, R_L = 25Ω, T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_O	Output Voltage Swing V_S = ±15V	25°C	±9	±11		I	V
	Output Voltage Swing V_S = ±5V	25°C	±2.4	±3.0		I	V
I_{OUT}	Output Current	25°C	360	440		I	mA
I_{SC}	Output Short-Circuit Current	25°C	600	800		I	mA
		T_{MIN}, T_{MAX}		800		V	mA
I_S	Supply Current	25°C		32	45	I	mA

Closed Loop AC Electrical Characteristics

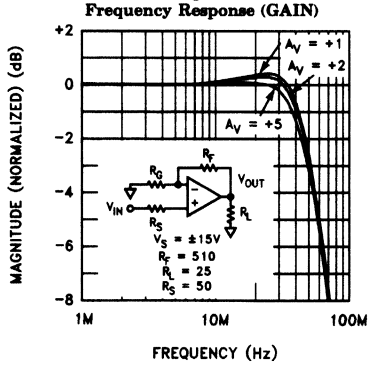
V_S = ±15V, A_V = +2, R_F = 510Ω, R_L = 25Ω, T_A = 25°C unless otherwise specified

Paremeter	Description	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Notes 4, 7)	500	1000		IV	V/μs
BW	−3 dB Bandwidth (Note 7)		50		V	MHz
Peaking	(Note 7)		0.3		V	dB
t_r, t_f	Rise Time, Fall Time (Notes 5, 7)		7		V	ns
dG	Differential Gain; DC Input Offset from 0V through +0.714V, AC Amplitude 286 mV_{p-p}, f = 3.58 MHz (Notes 6, 7)		0.03		V	%
dP	Differential Phase; DC Input Offset from 0V through +0.714V, AC Amplitude 286 mV_{p-p}, f = 3.58 MHz (Notes 6, 7)		0.05		V	deg. (°)

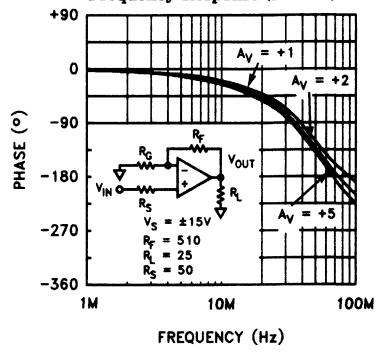
Note 1: The input is moved from −10V to +10V.
Note 2: The supplies are moved from ±5V to ±15V.
Note 3: V_{IN} = ±5V. See typical performance curve for larger values of V_{IN}.
Note 4: Slew Rate is with V_{OUT} from +5V to −5V and measured at 20% and 80%.
Note 5: Rise and Fall Times are with V_{OUT} between −0.5V and +0.5V and measured at 10% and 90%.
Note 6: See typical performance curves for other conditions.
Note 7: All AC tests are performed on a "warmed up" part, except for Slew Rate, which is pulse tested.

Typical Performance Curves (T_A = 25°C, R_L = 25Ω, A_V = +2, R_F = 510 unless otherwise specified)

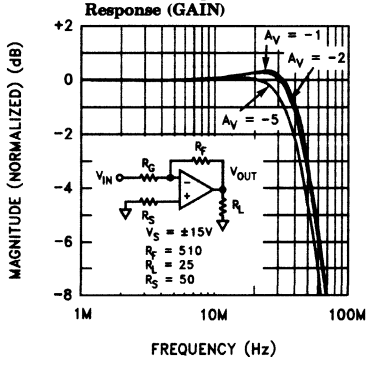
Non-Inverting
Frequency Response (GAIN)



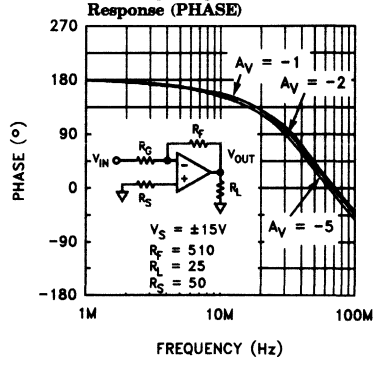
Non-Inverting
Frequency Response (PHASE)



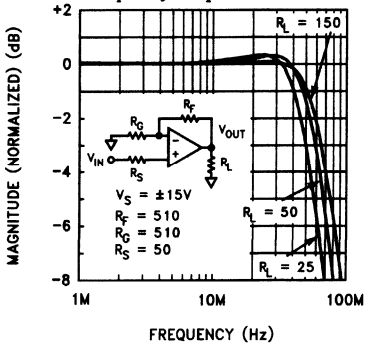
Inverting Frequency
Response (GAIN)



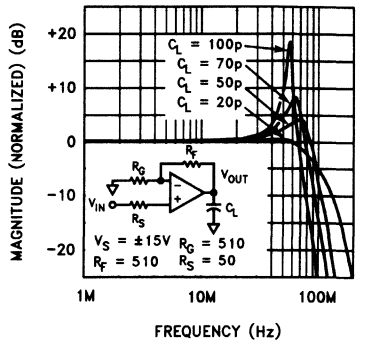
Inverting Frequency
Response (PHASE)



Frequency Response for Various R_L



Frequency Response for Various C_L



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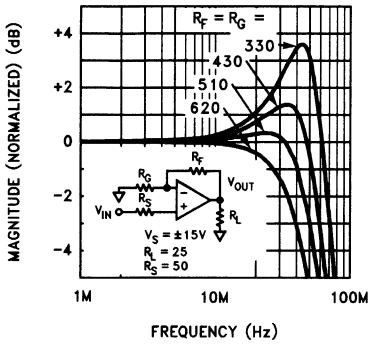
4

EL2099C
Video Distribution Amplifier

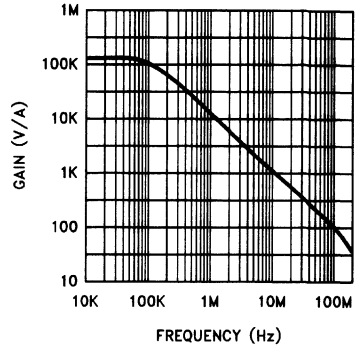
Typical Performance Curves

(T_A = 25°C, R_L = 25Ω, A_V = +2, R_F = 510 unless otherwise specified) — Contd.

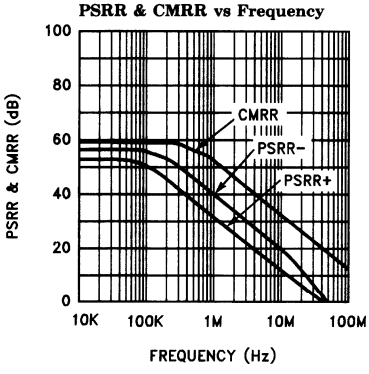
Frequency Response for Various R_F & R_G



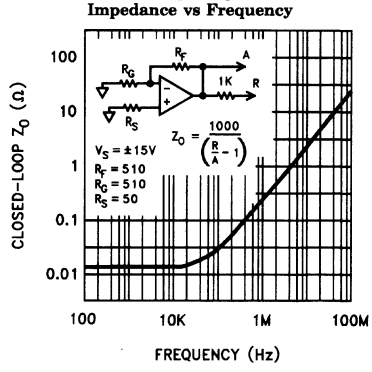
Transimpedance (R_{OL})



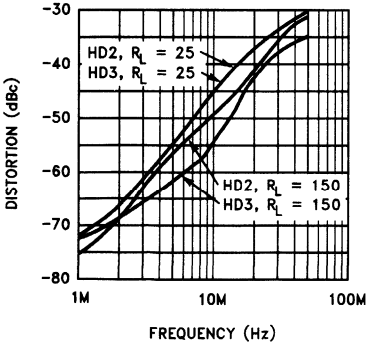
PSRR & CMRR vs Frequency



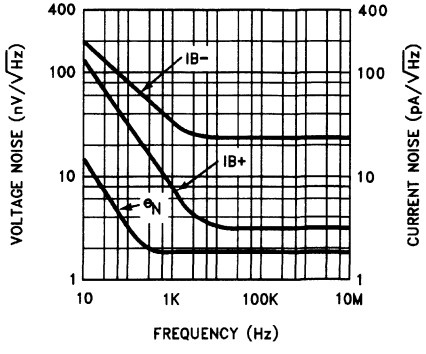
Closed-Loop Output Impedance vs Frequency



2nd and 3rd Harmonic Distortion vs Frequency



Voltage and Current Noise vs Frequency

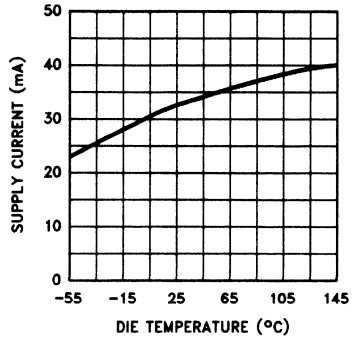


2099-3

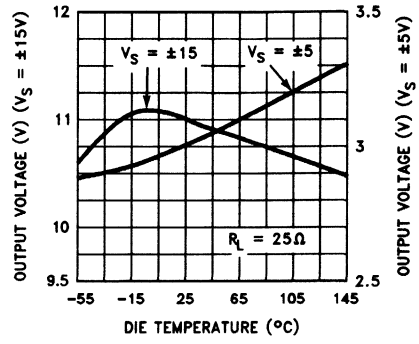
Typical Performance Curves

(T_A = 25°C, R_L = 25Ω, A_V = +2, R_F = 510 unless otherwise specified) — Contd.

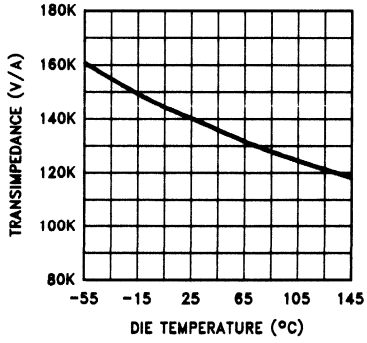
Supply Current vs Die Temperature



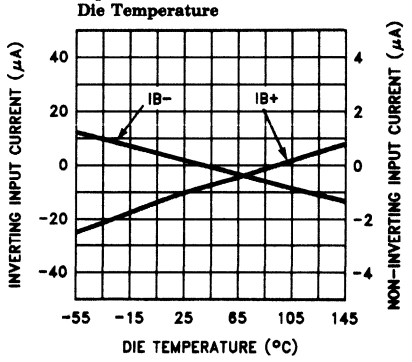
Output Voltage vs Die Temperature



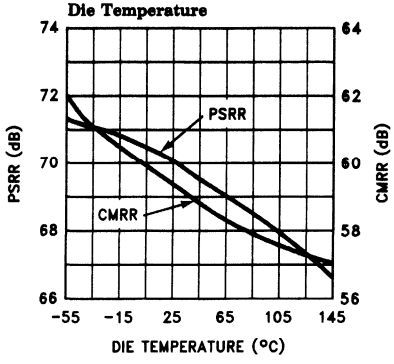
Transimpedance (R_{OL}) vs Die Temperature



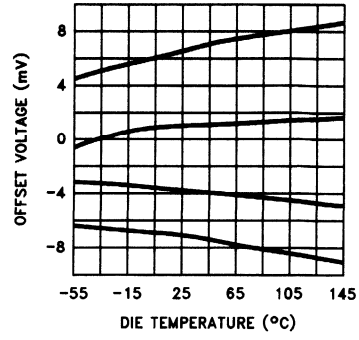
Input Current vs Die Temperature



PSRR & CMRR vs Die Temperature



Offset Voltage vs Die Temperature (4 Samples)



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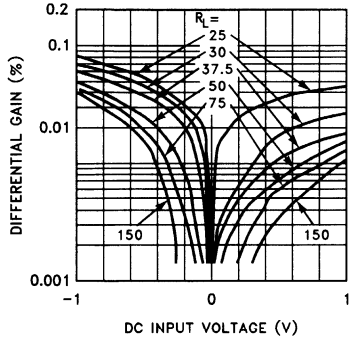
EL2099C
Video Distribution Amplifier

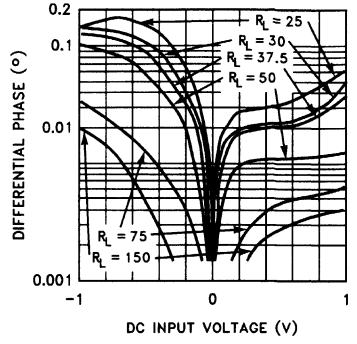
Typical Performance Curves

(T_A = 25°C, R_L = 25Ω, A_V = +2, R_F = 510 unless otherwise specified) — Contd.

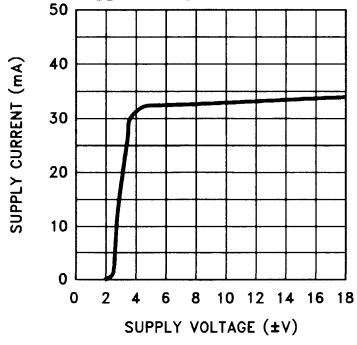
Differential Gain vs DC Input Voltage for Various R_Ls



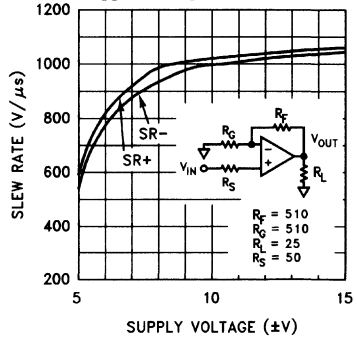
Differential Phase vs DC Input Voltage for Various R_Ls



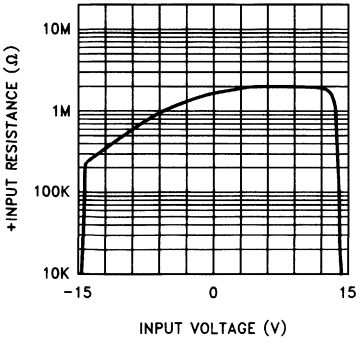
Supply Current vs Supply Voltage



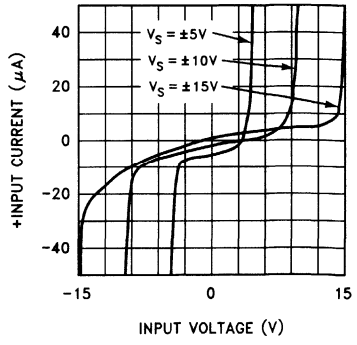
Slew Rate vs Supply Voltage



+Input Resistance vs Input Voltage



+Input Bias Current vs Input Voltage

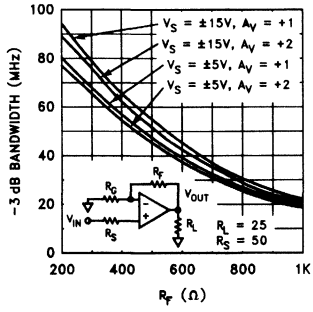


2099-5

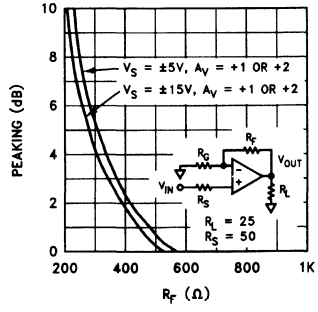
Typical Performance Curves

(T_A = 25°C, R_L = 25Ω, A_V = +2, R_F = 510 unless otherwise specified) — Contd.

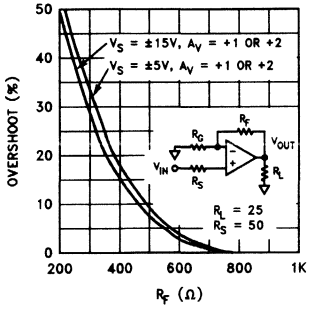
−3 dB Bandwidth vs R_F



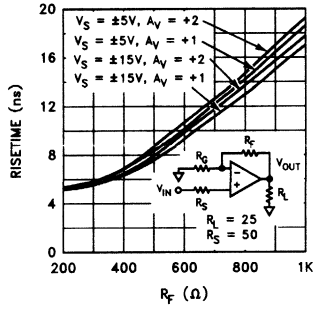
Peaking vs R_F



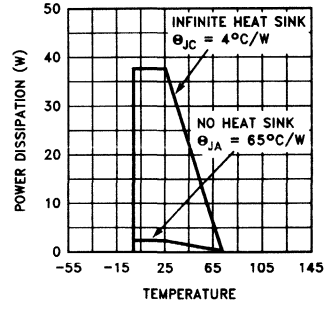
Overshoot vs R_F



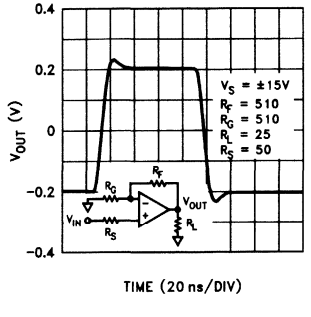
Rise Time vs R_F



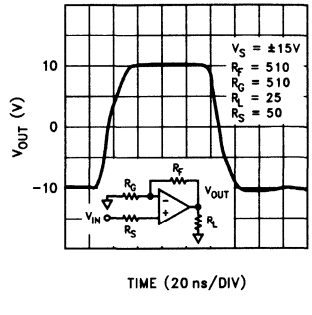
5-Lead TO-220 Maximum Power Dissipation vs Ambient Temperature



Small Signal Pulse Response



Large Signal Pulse Response



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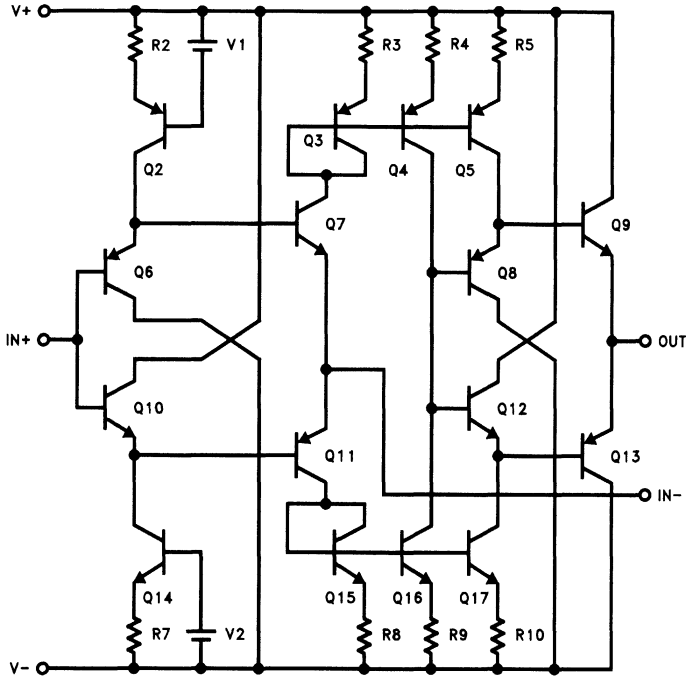
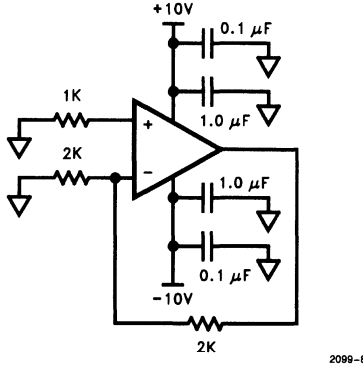
EL2099C
Video Distribution Amplifier

Simplified Schematic



Burn-In Circuit



Applications Information

Product Description

The EL2099C is a current mode feedback amplifier that has high output current drive capability. It is built using Elantec's proprietary dielectric isolation process that produces NPN and PNP complimentary transistors. The high output current can be useful to drive many standard video loads in parallel, as well as digital sync pulses that are 8V or greater.

+ Input Resistor Value

A small value resistor located in the + Input lead is necessary to keep the EL2099C from oscillating under certain conditions. A 50Ω resistor is recommended for all applications, although smaller values will work under some circumstances. All tests listed in this datasheet are performed with 50Ω in the + Input lead, as well as all typical performance curves. The 50Ω resistor along with the + Input bias current creates an additional typical Offset Voltage of only 250 μV at T = 25°C, and a maximum of 1.25 mV over temperature variations.

Feedback Resistor Values

The EL2099C has been designed and specified with R_F = 510Ω and A_V = +2. This value of feedback resistor yields extremely flat frequency response with little to no peaking. However, 3 dB bandwidth is reduced somewhat because of this. Wider bandwidth, at the expense of slight peaking, can be accomplished by reducing the value of the feedback resistor. For example, at a gain of +2, reducing the feedback resistor to 330Ω increases the −3 dB bandwidth to 70 MHz with 3 dB of peaking. Inversely, larger values of feedback resistor will cause roll off to occur at a lower frequency. There is essentially no peaking with R_F > 510Ω.

Power Supplies

The EL2099C may be operated with single or split supplies as low as ±5V (10V total) to as high as ±18V (36V total). Bandwidth and slew rate are almost constant from V_S = ±10V to ±18V, and decrease slightly as supplies are reduced to ±5V, as shown in the characteristic curves. It is not necessary to use equal value split supplies. For example, −5V and −12V would be fine for 0V to 1V video signals.

Good power supply bypassing should be used to reduce the risk of oscillation. A 1 μF to 10 μF tantalum capacitor in parallel with a 0.1 μF ceramic capacitor is recommended for bypassing each supply pin. They should be kept as close as possible to the device pins.

Due to the internal construction of the TO-220 package, the tab of the EL2099C is connected to the V_S- pin. Therefore, care must be taken to avoid connecting the tab to the ground plane of the system.

Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended. Lead lengths should be as short as possible. For good AC performance, parasitic capacitances should be kept to a minimum, especially at the inverting input, which is sensitive to stray capacitance. This implies keeping the ground plane away from this pin. Metal film and carbon resistors are both acceptable, while use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low inductance for best performance.

Driving Cables and Capacitive Loads

The EL2099C was designed with driving multiple coaxial cables in mind. With 440 mA of output drive and low output impedance, driving six 75Ω double terminated coaxial cables to ±11V with one EL2099C is practical.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, the back termination series resistor will decouple the EL2099C from the capacitive cable and allow extensive capacitive drive. For a discussion on some of the other ways to drive cables, see the application section on driving cables in the EL2003 data sheet.

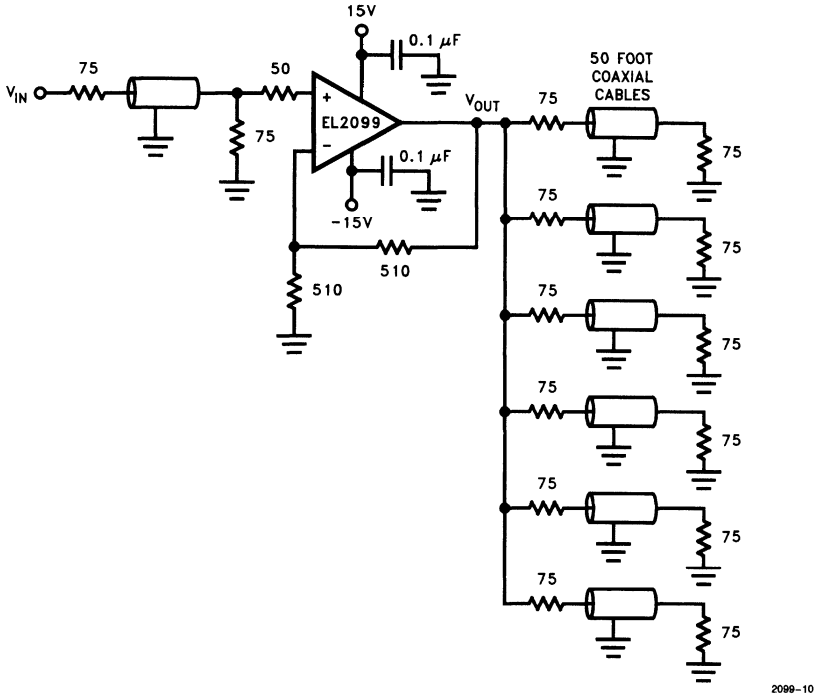
EL2099C
Video Distribution Amplifier

Applications Information — Contd.

Other applications may have high capacitive loads without termination resistors. In these applications, an additional small value (5Ω–50Ω) resistor in series with the output will eliminate most peaking.

The schematic below shows the EL2099C driving 6 double terminated cables, each of average length of 50 feet.

This represents driving an effective load of 25Ω to over ±10V. The resulting performance is shown in the scope photo. Notice that double termination results in reflection free performance.



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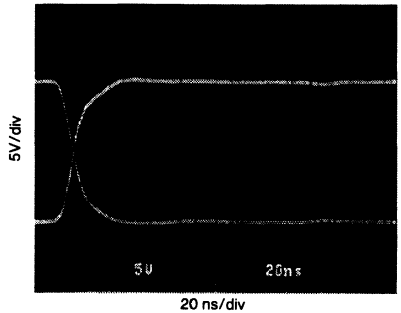


2099-11

EL2099 Macromodel

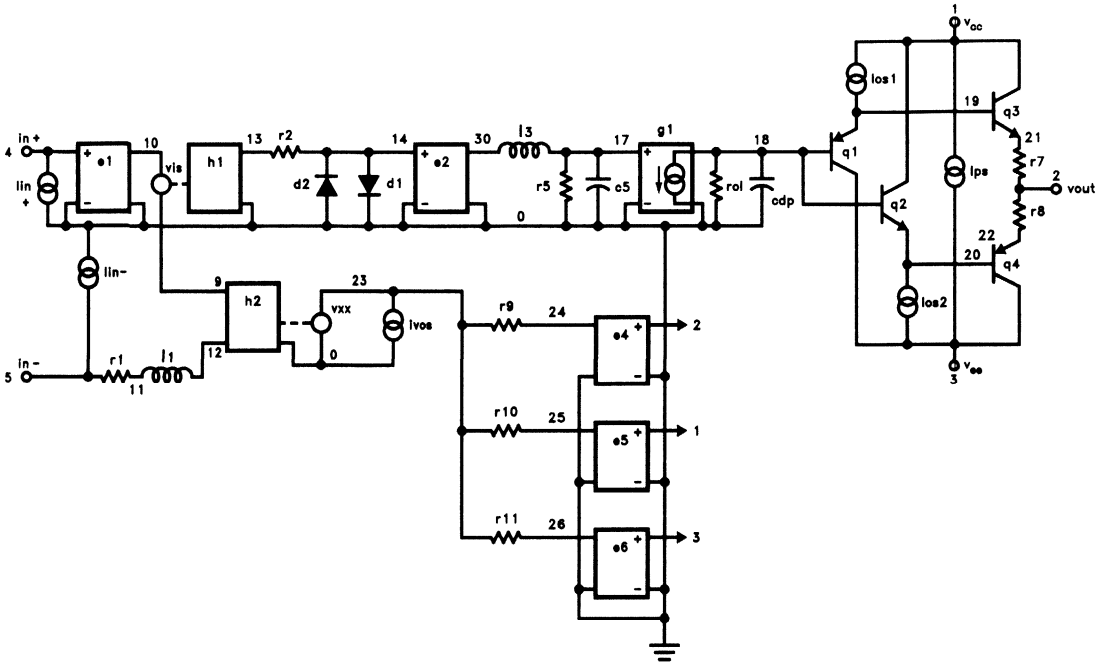
```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     output
*                   |     |     |     |     |
.subckt M2099       4     5     1     3     2
*
* Input Stage
*
e1 10 0 4 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 5 11 50
l1 11 12 48nH
iinp 4 0 5µA
iinm 5 0 -8µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
*e2 30 0 14 0 0.001667
13 30 17 1.5µH
c5 17 0 1pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
ro1 18 0 150K
cdp 18 0 8pF
*
* Output Stage
*
q1 3 18 19 qp
q2 1 18 20 qn
q3 1 19 21 qn
q4 3 20 22 qp
r7 21 2 1
r8 22 2 1
```

EL2099 Macromodel — Contd.

```
ios1 1 19 5mA
ios2 20 3 5mA
*
* Supply Current
*
ips 1 3 19mA
*
* Error Terms
*
ivos 0 23 5mA
vxx 23 0 0V
e4 24 0 2 0 1.0
e5 25 0 1 0 1.0
e6 26 0 3 0 1.0
r9 24 23 3K
r10 25 23 1K
r11 26 23 1K

* Models
*
.model qn npn (is=5e-15  bf=200  tf=0.1nS)
.model qp pnp (is=5e-15  bf=200  tf=0.1nS)
.model dclamp d (is=1e-30  ibv=0.266  bv=5  n=4)
.ends
```

EL2099 Macromodel — Contd.



2099-9

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4083/EL4084

Current Mode Four Quadrant Multiplier

Features

- Novel current mode design
  Virtual ground current summing inputs
  Differential ground referenced current outputs
- High speed (both inputs)
  200 MHz bandwidth
  12 ns 1% settling time
- Low distortion
  THD < 0.03% @ 1 MHz
  THD < 0.1% @ 10 MHz
- Low noise (R_L = 50Ω)
  100 dB dynamic range
  10 Hz to 20 kHz
  73 dB dynamic range
  10 Hz to 10 MHz
- Wide supply conditions
  ±5 to ±15V operation
  Programmable bias current
- Built-in high performance switching
  > 50 dB input(s) to output(s) isolation @ 100 MHz
  20 ns ON/OFF, OFF/ON switching time
- 0.2 dB gain tolerance to 25 MHz

Applications

- Four quadrant multiplication
- Gain control
- Controlled signal summing and multiplexing
- HDTV video fading and switching
- Mixing/modulating/demodulating (phase detection)
- Frequency doubling
- Division
- Squaring
- Square rooting
- RMS and power measurement
- Vector addition-RMS summing
- CRT focus and geometry correction
- Polynomial function generation
- AGC circuits

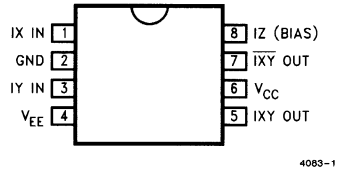
General Description

The 4083/84 makes use of an Elantec fully complimentary oxide isolated bipolar process to produce a patent pending current in, current out four quadrant multiplier. Input and output signal summing and direct interface to other current mode devices can be accomplished by simple connection to reduce component count and preserve bandwidth. The selection of an appropriate series resistor value allows an input to accept a voltage signal of any size and optimize dynamic range. The differential outputs offer significant performance improvements which greatly extend the usable gain control range at high frequencies. A fast, high isolation switching function has been incorporated into the design. The bias current is programmable to accommodate the voltage and power dissipation constraints of the package and available systems supplies.

The devices can implement all the classic four quadrant multiplier applications and are uniquely well suited to gain control, signal summing and multiplexing of broadband signals.

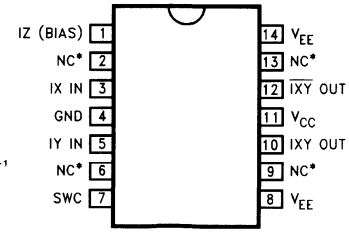
Connection Diagrams

EL4083
8-Pin SO/P DIP



Top View

EL4084
14-Pin SO/P DIP



Top View

* In package trim pins
MAKE NO CONNECTION!

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4083CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL4083CS	−40°C to +85°C	8-Pin SO	MDP0027
EL4084CN	−40°C to +85°C	14-Pin P-DIP	MDP0031
EL4084CM	−40°C to +85°C	14-Pin SO	MDP0027

June 1993 Rev A

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V_S+ and V_S−	+33V	T_{ST}	Storage Temperature	−65°C to +150°C
$I_{Z(BIAS)}$	Z, Bias Current	+2.4 mA		Lead Temperature	
I_X	X Input Current	±2.4 mA		DIP Package	300°C
I_Y	Y Input Current	±2.4 mA		(Soldering: <10 seconds)	
P_D	Maximum Power Dissipation	See Curves		SO Package	
T_A	Operating Temperature Range			Vapor Phase (60 seconds)	215°C
	EL4083	−40°C to +85°C		Infrared (15 seconds)	220°C
	EL4084	−40°C to +85°C			
T_J	Operating Junction Temperature				
	EL4083	150°C			
	EL4084	150°C			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics (T_A = 25°C, V_S = ±5, I_Z = 1.6 mA) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Test Level	Units
Power Supplies						
Operating Supply Voltage Range		±4.5		±16.5	I	V
I_{CC}	V_S = ±15V, I_Z = 0.2 mA	7.2	8.5	9.5	I	mA
I_{CC}	V_S = ±5V, I_Z = 1.6 mA	42.0	44.0	45	I	mA
I_{EE}	V_S = ±15V, I_Z = 0.2 mA	9.5	10.0	12	I	mA
I_{EE}	V_S = ±5V, I_Z = 1.6 mA	45	47	48	I	mA
Multiplier Performance						
5) Transfer Function	$(I_{XY}-I_{\overline{XY}}) = K(I_X \times I_Y)/I_Z$					
K Value		0.92	0.965	0.985	I	
1) Total Error	−2 mA < I_X, I_Y <2 mA		±0.5	±2	I	%FS
vs. Temp	T_{MIN} to T_{MAX}		±1.5	±3	IV	%FS
2) Linearity			0.25	0.5	I	%FS
3) Bandwidth	−3 dB (See Figure 2)	200	225		III	MHz
5)X Feedthrough DC to I_{XY} or $I_{\overline{XY}}$	I_X = ±2 mA, I_Y = 0 (unnulled)		0.15	1.6	I	%FS
5)Y Feedthrough DC to I_{XY} or $I_{\overline{XY}}$	I_Y = ±2 mA, I_X = 0 (unnulled)		0.15	1.6	I	%FS
4) AC Feedthrough, X to I_{XY} or $I_{\overline{XY}}$	I_X = 4 mApp, I_Y = nulled					
	f = 3.58 MHz		−80		V	dB
	f = 100 MHz		−28		V	dB
4) AC Feedthrough, X to $(I_{XY}-I_{\overline{XY}})$	I_X = 4 mApp, I_Y = nulled DC < f < 1 GHz		−50		V	dB
4) AC Feedthrough, Y to I_{XY} or $I_{\overline{XY}}$	I_Y = 4 mApp, I_X = nulled					
	f = 3.58 MHz		−64		V	dB
	f = 100 MHz		−26		V	dB
4) AC Feedthrough, Y to $(I_{XY}-I_{\overline{XY}})$	I_Y = 4 mApp, I_X = nulled DC < f < 1 GHz		−50		V	dB

EL4083/EL4084
Current Mode Four Quadrant Multiplier

Electrical Characteristics — Contd. (T_A = 25°C, V_S = ±5, I_Z = 1.6 mA) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Test Level	Units
Inputs (I_X, I_Y)						
Full Scale Range	FRS = 1.25 × I_Z (Nominal)		±2		I	mA
Clipping Level	C_L = 2 × I_Z	2.85	3.2		I	mA
Z_{IN} (I_X)		30	40	48	I	Ω
Z_{IN} (I_Y)		30	36	48	I	Ω
Input Offset Voltages	at Input Pins, I_Z = 1.6 mA	−4		+4	I	mV
(V_{OSX},V_{OSY})	I_Z = 0.2 mA	−12		+12	I	mV
5)Input Offset Currents	R_{SX} = R_{SY} = 1K, V_X = V_Y = 0,		±10	±40	I	μA
I_{XOS}, I_{YOS}	T_{MIN} to T_{MAX}		±20		V	nA/°C
Nonlinearity						
I_X	I_Y = 2 mA, − 2 mA < I_X < 2 mA		0.1	0.6	I	%FS
I_Y	I_X = 2 mA, − 2 mA < I_Y < 2 mA		0.1	0.4	I	%FS
Distortion, I_X (to I_{XY} or $I_{\overline{XY}}$)	I_Y = 2 mA, − 2 mA < I_X < 2 mA					
	f = 3.58 MHz		−55		V	dB
	f = 100 MHz		−25		V	dB
Distortion, I_Y (to I_{XY} or $I_{\overline{XY}}$)	I_X = 2 mA, − 2 mA < Iy < 2 mA					
	f = 3.58 MHz		−56		V	dB
	f = 100 MHz		−26		V	dB
Distortion, I_X (to (I_{XY} − $I_{\overline{XY}}$)	I_Y = 2 mA, −2 mA < I_X < 2 mA					
	f = 3.58 MHz		−66		V	dB
	f = 100 MHz		−35		V	dB
Distortion, I_Y (to (I_{XY} − $I_{\overline{XY}}$)	I_X = 2 mA, −2 mA < I_Y < 2 mA					
	f = 3.58 MHz		−66		V	dB
	f = 100 MHz		−34		V	dB
Diff Gain	@3.58 MHz					
I_X	I_Z = 0.2 mA, I_Y = 0.25 mA		0.2		V	%
I_Y	I_Z = 0.2 mA, I_X = 0.25 mA		0.17		V	%
I_X	I_Z = 1.6 mA, I_Y = 2 mA		0.1		V	%
I_Y	I_Z = 1.6 mA, I_X = 2 mA		0.05		V	%
Diff Phase	@3.58 MHz					
I_X	I_Z = 0.2 mA, I_Y = 0.25 mA		0.5		V	deg °
I_Y	I_Z = 0.2 mA, I_X = 0.25 mA		0.5		V	deg °
I_X	I_Z = 1.6 mA, I_Y = 2 mA		0.05		V	deg °
I_Y	I_Z = 1.6 mA, I_X = 2 mA		0.05		V	deg °
Outputs (I_{XY}, I_{YX})						
5)Output I_{OS}	I_X = I_Y = 0		−15	±120	I	μA
5)Diff Output I_{OS}	I_X = I_Y = 0, (I_{XY}-$I_{\overline{XY}}$)		±0.1	±80	I	μA
Voltage Compliance		±1.5	±2.0		V	V
Max Output Current Swing		±2.85	±3.2		I	mA
Noise Spectral Density						
10 Hz < f < 10 MHz	R_L = 50Ω		125		V	pA/rootHz
I_Z (Bias)						
Current Range	Tested	0.2		1.6	I	mA
Input Voltage	I_Z = 0.2 mA			±25	I	mV
Input Voltage	I_Z = 1.6 mA			±25	I	mV

Electrical Characteristics — Contd. (T_A = 25°C, V_S = ±5, I_Z = 1.6 mA) unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Test Level	Units
Switching (Specifications Apply for EL4084 only)						
I_{SW} (off)		0.87			I	mA
I_{SW} (on)				0.2	I	mA
Switching Voltage			0		V	mV
Z_{IN} (swc)	At Switch Control	400	500	600	I	Ω
I (Internal Pulldown)		0.38	0.5	0.62	I	mA
D.C. Output Leakage						
I_{XY}, $I_{\overline{XY}}$	Part Switched Off			±3	I	µA
Off Feedthrough I_X to I_{XY}, $I_{\overline{XY}}$	I_Y = 2 mA, −2 mA < I_X < 2 mA A.C. ~1 kHz, Switch Off			±1	I	µA
Off Feedthrough I_Y to I_{XY}, $I_{\overline{XY}}$	I_X = 2 mA, −2 mA < I_Y < 2 mA A.C. ~1 kHz, Switch Off			±1	I	µA
Off Feedthrough I_X to I_{XY}-$I_{\overline{XY}}$	I_Y = 2 mA, −2 mA < I_X < 2 mA A.C. ~1 kHz, Switch Off			±1	I	µA
Off Feedthrough I_Y to I_{XY}-$I_{\overline{XY}}$	I_X = 2 mA, −2 mA < I_Y < 2 mA A.C. ~1 kHz, Switch Off			±1	I	µA
T (on/off)			20		V	ns
T (off/on)			20		V	ns

Note 1: Error is defined as the maximum deviation from the ideal transfer function expressed as a percentage of the full scale output.

Note 2: Linearity is defined as the error remaining after compensating for scale factor (gain) variation and input and output referred offset errors.

Note 3: Bandwidth is guaranteed using the squaring mode test circuit of Figure 4.

Note 4: Relative to full scale output with full scale sinewave on signal input and zero port input nulled. Specification represents feedthrough of the fundamental.

Note 5: Specifications are provisional for the EL4083. Corresponding specs for the EL4084 are TBD. EL4084 production specifications will appear in the 1994 data book.

EL4083/EL4084
Current Mode Four Quadrant Multiplier

EL4083/4084 Block Diagram

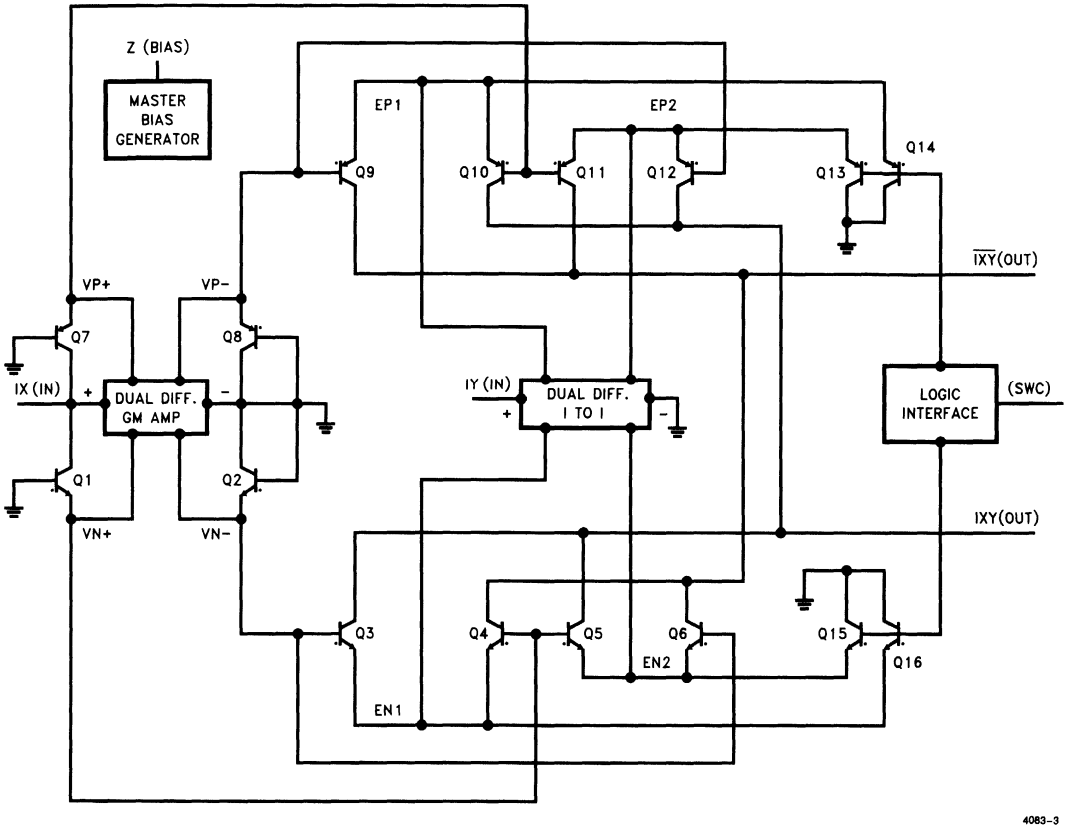


Figure 1

AC Test Fixture

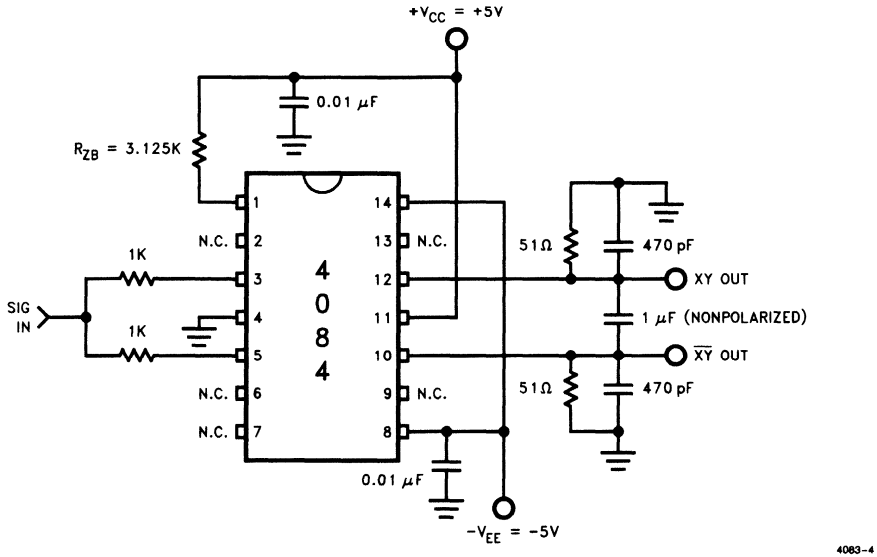


Figure 2. AC Bandwidth Test Fixture

Burn-In Circuit

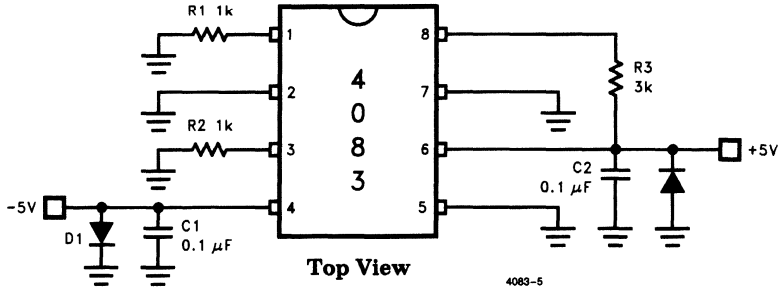


Figure 3. Burn-In Circuit P-DIP

EL4083/EL4084
Current Mode Four Quadrant Multiplier

8-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

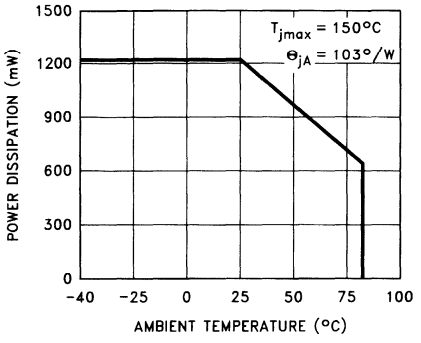


Figure 4a.

8-Lead SO
Maximum Power Dissipation
vs Ambient Temperature

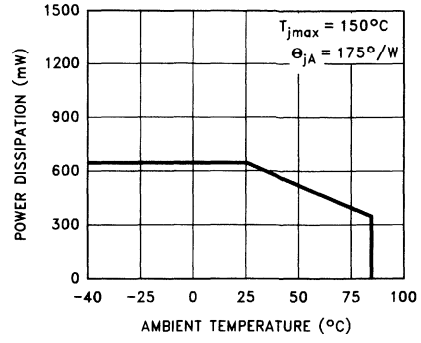


Figure 4b.

14-Pin Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

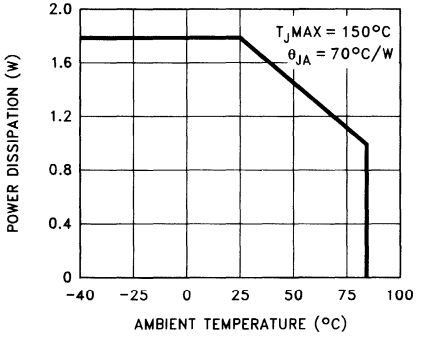


Figure 5a.

14-Lead SO
Maximum Power Dissipation
vs Ambient Temperature

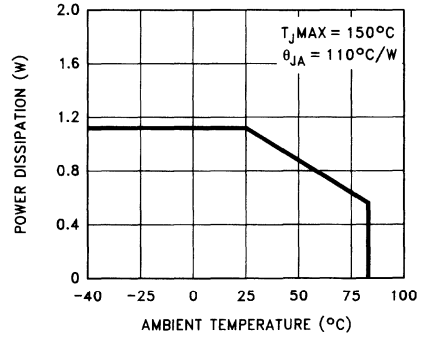


Figure 5b.

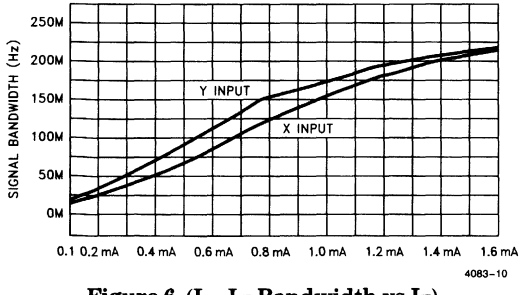


Figure 6. (I_X, I_Y Bandwidth vs I_Z)

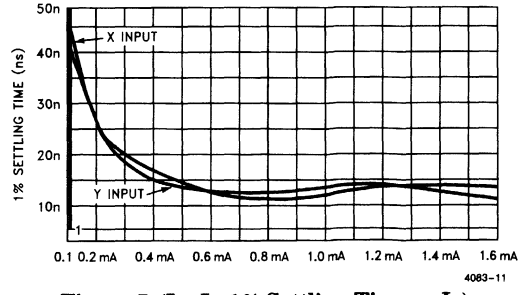


Figure 7. (I_X, I_Y 1% Settling Time vs I_Z)

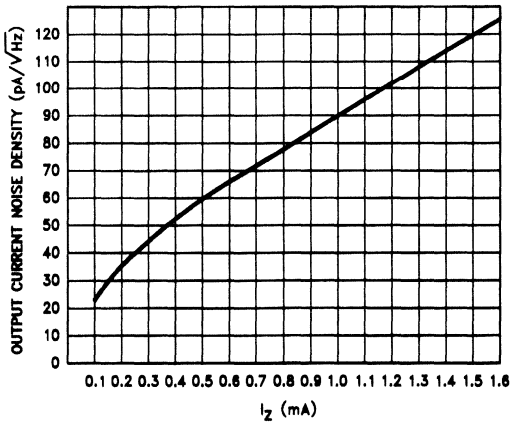
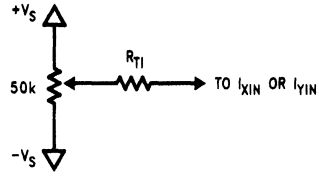


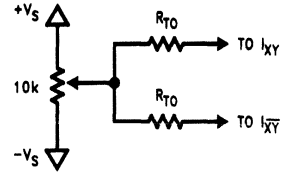
Figure 8. Output Noise Density vs I_Z Bias

Input Offset Trim(s)



$R_{TI} = (V_S \times 1.6\ mA)/(16\ \mu A \times I_Z)$

Output Offset Trim



$R_{TO} = (V_S \times 1.6\ mA)/(30\ \mu A \times I_Z)$

Figure 9. Optional External Trim Networks

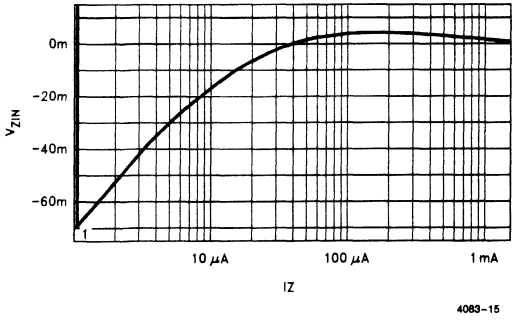


Figure 10. V_{ZIN} vs I_Z (Typical)

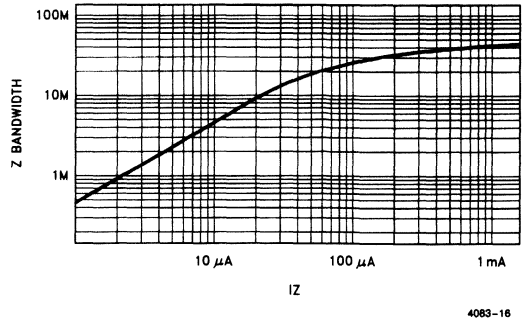


Figure 11. I_{ZIN} Bandwidth vs I_Z

EL4083/EL4084
Current Mode Four Quadrant Multiplier

General Operating Information

I_Z Input (Bias, Divisor) and Power Supplies

The I_Z pin is a low impedance ($<20\Omega$) virtual ground current input. It can accept positive current from a resistor connected to a positive voltage source or the positive supply. The instantaneous bias for the multiplier gain core is proportional to this current value. Negative applied current will put the multiplier portion of the circuit in a zero bias state and the voltage at the pin will be clamped at a diode drop below ground. The part will respond in a similar manner to currents from a current source such as the output of a transconductance amplifier or one of its own outputs. The overall transfer equation for the EL4083/4084 is:

$$K(I_X \times I_Y)/I_Z = (I_{XY}-I_{\overline{XY}}),\ K \sim 1$$

As can be seen from the equation, the Z input can serve as a divisor input. However, it is different from the other two inputs in that the value of its current determines the supply current of the part and the bandwidth and compliance range of the outputs and other two inputs. Table 1 gives the equations describing these and other important relationships. These dependencies can complicate and/or limit the usefulness of this pin as a computational input. The I_Z dependence of the impedance of the multiplying inputs can be particularly troublesome. See the I_Z divider and the RMS#2 circuit sections of the application note for some ways of dealing with this.

The primary intended use for the Z input is as a programming pin similar in function to those on programmable op amps. This enables one to trade off power consumption against bandwidth and settling time and allow the part to function within its power dissipation rating over its full operational supply range ($\pm 4.5V$ – $\pm 16.5V$). The E4083/4084 has been designed to function well for I_Z values in the range of 200 $\mu A < I_Z <$ 1.6 mA which corresponds to I_X and I_Y signal bandwidths of about 50 MHz to over 200 MHz. Higher values of I_Z may cause problems at temperature extremes while lower values down to zero will progressively degrade the input referred D.C. offsets and reduce speed. Below about 50 μA of bias current the internal servo amplifier loop which maintains the I_Z pin at ground will lose regulation and the voltage at the pin will start to move negative (see Figure 10). This is accompanied by a significant increase in input impedance of the pin. Figure 11 shows the A.C. bandwidth of the I_Z input as a function of the D.C. value of I_Z. Figures 6 and 7 show the bandwidth and 1% settling time of the multiplying inputs, I_X and I_Y, as functions of I_Z.

I_X and I_Y (Multiplier) Inputs and Offset Trimming

The I_X and I_Y pins are low impedance (I_Z dependent) virtual ground current inputs that accept bipolar signals. The input referred clip value is equal to $I_Z \times 2$ while the full scale value has been chosen to be $1.25 \times I_Z$ to maintain excellent distortion and linearity performance. Operating at higher full scale values will degrade these two pa-

Table 1. Basic Design Equations and Relationships

Positive Supply Current	$I_S+ = 3.4\ mA + I_Z \times 26$
Negative Supply Current	$I_S- = 4.5\ mA + I_Z \times 27$
Power Dissipation (See Figures 4 and 5)	$PWR = (+V_S - (-V_S)) \times (4\ mA + I_Z \times 26.5)$
Multipling Input(s) Impedance	$R_{ZX} = R_{ZY} = (32\Omega) \times 1.6\ mA/I_Z$
Multiplying Input(s) Clip Point	$I_X\ (clip) = I_Y\ (clip) = I_Z \times 2$
Multiplying Input(s) Full Scale Value	$I_X\ (fs) = I_Y\ (fs) = I_Z \times 1.25$ (nominal)
Multiplying Input Resistor Values	$R_X = V_X\ (peak)/I_X\ (fs)$
(In Terms of Peak Input Signal)	$R_Y = V_Y\ (peak)/I_Y\ (fs)$
Full Scale Output (Single Ended)	$I_{XY} = I_{\overline{XY}} = I_X\ (fs) \times I_Y\ (fs)/(I_Z \times 2)$
Full Scale Output (Differential)	$(I_{XY} - I_{\overline{XY}}) = I_X\ (fs) \times I_Y\ (fs)/I_Z$
I_Z (Bias) Input Voltage vs I_Z	(See Figure 10)
I_Z Signal Bandwidth vs I_Z	(See Figure 11)
I_X, I_Y Signal Bandwidth vs I_Z	(See Figure 6)
I_X, I_Y 1% Settling Time vs I_Z	(See Figure 7)

General Operating Information

— Contd.

rameters and, to some extent, bandwidth while improving the signal to noise performance, feedthrough and control range.

The EL4083/4084 is fundamentally different from conventional voltage mode multipliers in that the available input range can be tailored to accommodate voltage sources of almost any size by selecting appropriate input series resistor values. If desired, one can interface with voltages that are much greater than the supplies from which the part is powered. Current source signals can be connected directly to the multiplier inputs. The parts' dynamic range can also be tailored to a large extent for a current signal by the appropriate selection of I_Z. These inputs act in the same manner as a virtual ground input of an operational amplifier and thus can serve as a summing node for any number of voltage and/or current signals. Outputs of components such as current output DACs, transconductance amplifiers and current conveyors can be directly connected to the inputs.

Ideally, a multiplier should give zero output if either one of its multiplying inputs is zero. A nonzero output under these conditions is caused by a combination of input and output referred offsets. An output referred offset can be thought of as a fixed value added to the output and thus only affects D.C. accuracy. An input referred offset at a multiplying input allows signal to feedthrough from the other multiplying input to the output(s). The EL4083/4084 is trimmed during testing at Elantec for X and Y input referred offset for I_Z = 1.6 mA. The 4084 is trimmed in package and is the premium D.C. accuracy part. The internal trim networks provide a current to each input which nulls the feedthrough caused by internal device mismatches. These current values are ratioed to the value of I_Z so that the input referred nulls are largely maintained at different values of I_Z. However, there will be some mistracking in the trim networks so that the input referred null point will deviate away from zero at values of I_Z lower than 1.6 mA. Figure 9 shows optional external input and output referred offset trim networks which can be used as needed to improve performance. As mentioned, the output referred offset only affects D.C. accuracy which may not be an issue in A.C. applications. In gain control applications one may only need to null feedthrough with respect to the gain control input. The usable untrimmed gain control range of the 4084 is in excess of 50 dB.

In gain control (VCA) applications the X input should be used as the control input and the signal applied to the Y input since it has slightly higher bandwidth and better linearity and distortion performance.

Current Outputs (I_{XY}, $I_{\overline{XY}}$), Feedthrough and Distortion

Another unique feature of the EL4083/4084 is the differential ground referenced current output structure. These outputs can drive 50Ω terminated lines and reactive loads such as transformers, baluns, and LC tank and filter circuits directly.* Unlike low impedance follower buffers, these outputs do not interact with the load to produce ringing or instability. If a high level low impedance output is required, the outputs can be recovered differentially and converted to a single ended output with a fast op amp such as the EL2075 (see Figure 23). The outputs can also drive current input devices such as CMF amps, current conveyors and its own inputs directly by simple connection.

Figures 12 and 14 show the nulled gain and feedthrough characteristics of the I_{XY} and $I_{\overline{XY}}$ outputs which are virtually identical and differ only in phase. Figure 12 is with the A.C. signal applied to the X input with Y used as the gain control and in Figure 14 these signals are reversed. Note that in both cases the signal feedthrough rolls up and peaks near the cutoff frequency. This is quite typical of the performance of all previous four quadrant multipliers. Figures 13 and 15 show the corresponding gain/feedthrough characteristics for the differentially recovered output signal I_{XY}-$I_{\overline{XY}}$. Note that in this case the peak feedthrough at high frequencies is lower by more than 40 dB.

* See EL2082 Data Sheet—Receiver IF Amplifier (Figure 19). The EL2082 also has a current output.

EL4083/EL4084
Current Mode Four Quadrant Multiplier

General Operating Information

— Contd.

Figures 16 and 17 show the total harmonic distortion for the single-ended and differential recovered outputs for a full scale A.C. input signal on one input and a full scale D.C. control signal on the other. Note that above about one megahertz to the cutoff frequency the THD of the differentially recovered signal is as much as 10 dB lower than the single-ended signals.

Switch Control and Off Isolation (On EL4084 Only)

The switch control can change the outputs between full on and a high isolation off state in 20 ns. The switch pin appears as a 500Ω resistance to ground that is internally loaded by a 500 μA current source to the negative supply. The D.C. voltage at the open pin is about −250 mV. Also connected internally to the pin are one base each of two complementary differential pairs with the other bases connected to ground. This input has been designed so that the outputs are on if the pin is left unconnected. Also, the required on/off switching voltage at the pin is only about 500 mV to prevent package feedthrough of the switching signal. The recommended interface is a series resistor from the pin to the switch control voltage source whose chosen value will source about 1 mA into the 500Ω pin resistance when the source voltage is high. This will force the outputs to their off state. The current consumption of the part in the off state is higher by about 650 μA.

Figure 18 and 19 shows the full level, full gain input to single ended output isolation of the EL4084 with the outputs switched off. Also shown is the off isolation under the same conditions for the differentially recovered output signal. Note that at high frequencies there is about a 40 dB improvement that is similar to the signal feedthrough improvement in Figures 13 and 15. The fact that the multiplier inputs are virtual grounds prevents package feedthrough from ruining these effects in practice.

The switch "glitch" or feedthrough is also greatly improved by recovering the output signal differentially. The switching transients on the single-ended outputs can be as much as 50% of full scale with about a 5 ns duration. For the differential output, the amplitude is less than one fifth of this. In general the switching transient for the single-ended outputs can be large enough so that a system may need to ignore the output during the switching interval so that the "glitch" is not confused with signal. For the differentially recovered output, this may not be necessary. Figures 20 and 21 show the on/off/on switching response for a 100 MHz signal driving the I_X input. The two single ended outputs are shown in Figure 20 while Figure 21 is the differentially recovered output. The waveforms for the signal driving the I_Y input are very similar.

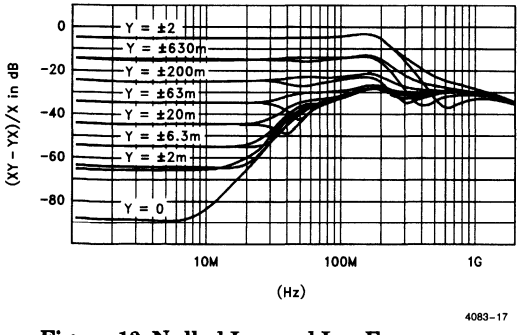


Figure 12. Nulled I_{XY} and $I_{\overline{XY}}$ Frequency Response (Signal on XIN, Gain Controlled by YIN)

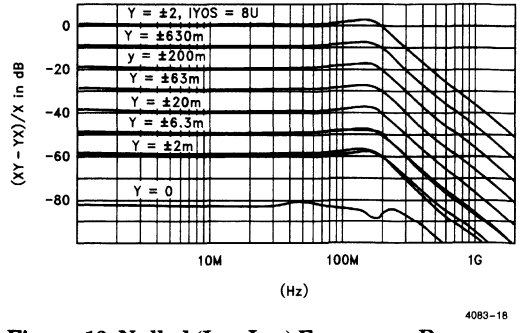


Figure 13. Nulled (I_{XY}-$I_{\overline{XY}}$) Frequency Response (Signal on XIN, Gain Controlled by YIN)

General Operating Information — Contd.

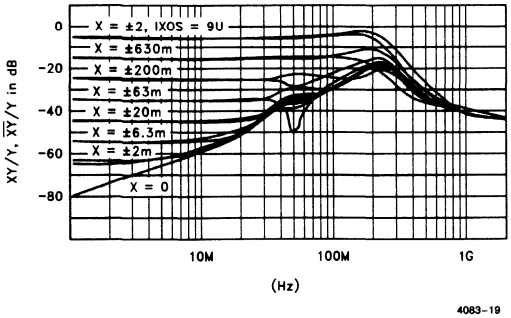


Figure 14. Nulled I_{XY} and $I_{\overline{XY}}$ Frequency Response (Signal on YIN, Gain Controlled by XIN)

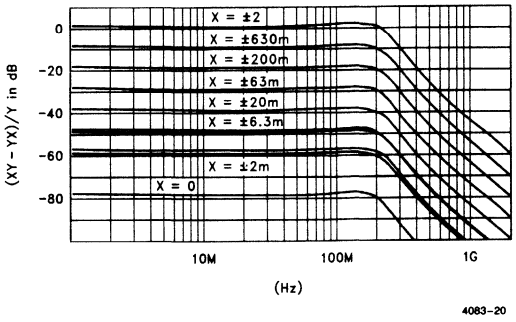


Figure 15. Nulled (I_{XY}–$I_{\overline{XY}}$) Frequency Response (Signal on YIN, Gain Controlled by XIN)

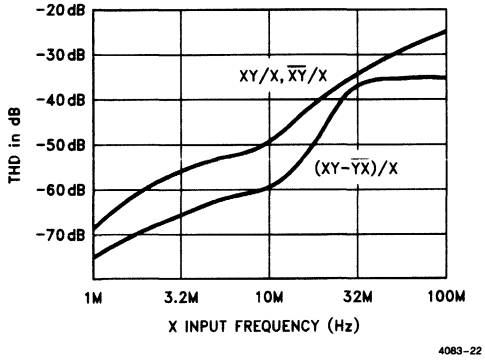


Figure 16. (Full Level XIN THD vs Frequency)

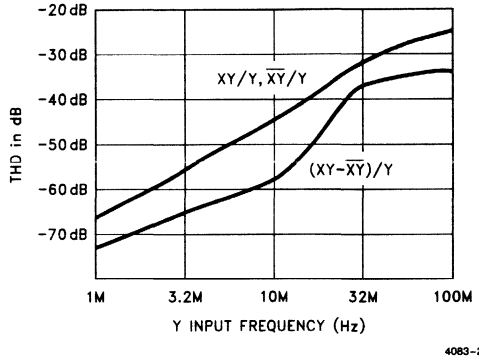


Figure 17. (Full Level YIN THD vs Frequency)

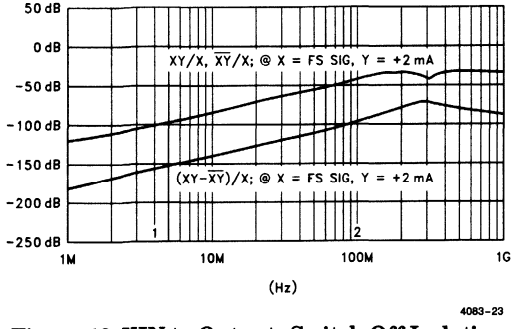


Figure 18. XIN to Outputs Switch Off Isolation

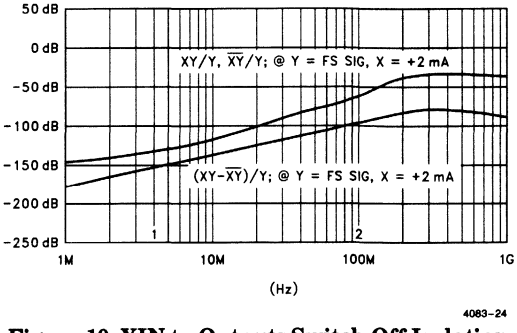


Figure 19. YIN to Outputs Switch Off Isolation

EL4083/EL4084
Current Mode Four Quadrant Multiplier

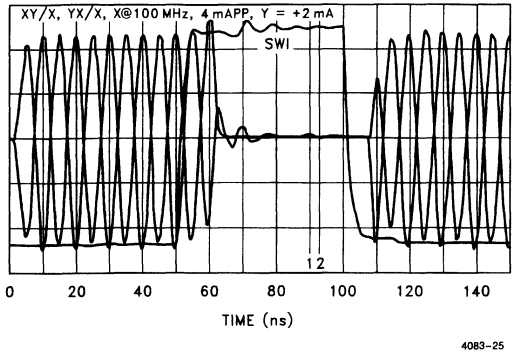


Figure 20. I_{XY} and $I_{\overline{XY}}$ ON/OFF/ON Switching Response

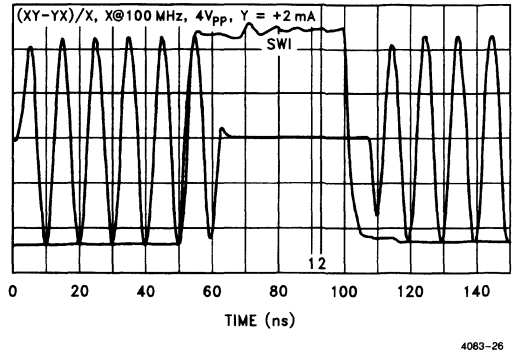


Figure 21. $I_{XY}-I_{\overline{XY}}$ ON/OFF/ON Switching Response

Applications

Basic Product Functions

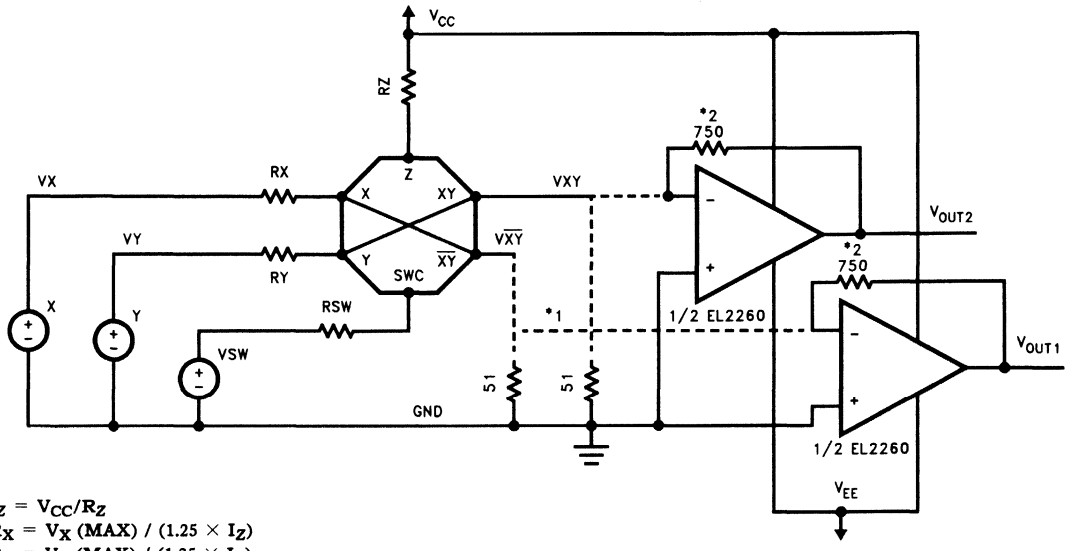
Figures 22 and 23 are the basic schematics for many of the applications of the EL4083/4084. These can perform signal mixing, frequency doubling, modulation, demodulation, gain control/voltage-controlled amplification, video switching, multiplication and squaring. Figure 22 has resistively terminated differential outputs and has the widest bandwidth. The figure also shows the option of using the EL2260 dual CMF amplifier to recover the outputs differentially at very low impedance. This has a maximum 3 dB bandwidth of 130 MHz and settles to 1% in 25 ns. Figure 23 uses an EL2075 at the outputs as a differential to single ended converter with gain to take advantage of the performance enhancements of the differentially recovered output mentioned above and to provide a high level low impedance drive. The 3 dB bandwidth of this circuit is over 150 MHz using good layout techniques. However, to achieve this bandwidth one must restrict the output swing to little more than 1 Vpp to avoid running into the 500V/μs minimum slew rate of the EL2075. The EL2038 has a minimum slew rate of 750V/μs and, unlike the EL2075, will work on supplies up to $\pm$15V. However, it has only half the EL2075's gain bandwidth product. Table 2 shows the input signal assignments for the applications listed above.

Table 2. Input Signal Assignments for Figures 22 and 23 Circuits

Application	V_X	V_Y	V_{SW}*
Mixer	Signal 1	Signal 2	X
Frequency Doubler	Signal	Signal	X
Modulator	Modulating Signal	Carrier	X
Demodulator	Local Oscillator	Modulated Signal	X
Gain Control/VCA	Gain Control	Signal	X
Video Switch	Gain Voltage	Signal	Switch Control
Multiplier	Signal 1	Signal 2	X
Squarer	Signal	Signal	X

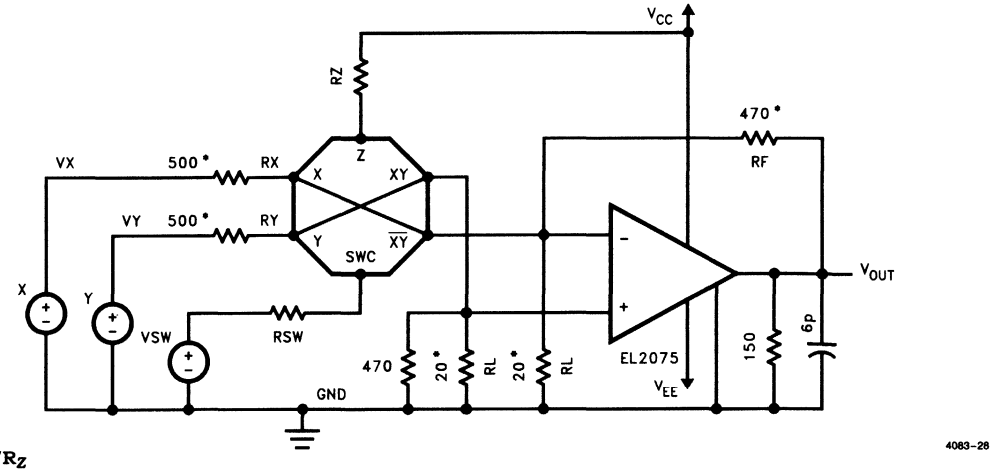
* X means not connected if function is not used.

Applications — Contd.



$I_Z = V_{CC}/R_Z$
$R_X = V_X$ (MAX) / (1.25 × I_Z)
$R_Y = V_Y$ (MAX) / (1.25 × I_Z)
RSW = VSW (HIGH) /1 mA
*1. 51Ω Resistors omitted when using EL2260
*2. Optimum value of RF determined by supplies and amount or tolerable peaking
(−3 dB BW ~ 90 MHz @ V_S = ±5V, BW ~ 150 MHz @ ±15V)

Figure 22. Basic Schematic (Dual Diff Outs)



$I_Z = V_{CC}/R_Z$
$R_X = V_X$ (MAX) / (1.25 × I_Z)
$R_Y = V_Y$ (MAX) / (1.25 × I_Z)
RSW = VSW (HIGH) /1 mA
*Optimized for Wide Bandwidth

Figure 23. Basic Schematic (Single Ended Converted)
(150 MHz VCA/Switch)

Other Applications

Elantec has also published an applications note covering other applications of the EL4083/4084. These include dividers, squaring and square rooting circuits, several RMS and power measurement circuits, and a wideband AGC circuit. Also presented are two polynomial computation examples for video and some HDTV quality fader and summing circuits with switching capability. The EL4083/4084 have been found flexible enough to easily implement all of the classic four quadrant multiplier applications and also offer interesting new applications possibilities.

EL4083/4084 Macromodel

This macromodel is compatible with PSPICE (copywritten by Microsim Corporation) . It has been designed to work accurately for fixed values of I_Z (bias) in the range of 200 μA to 1.6 mA. The additional simulation burden imposed by including provision for a time varying I_Z was thought not worthwhile. The value of I_Z is specified to the model by the parameter NS. The relation between I_Z and NS is; I_Z = 200 μA$\times$NS. All other inputs can accept time varying signals.

The model will provide good transient and frequency response and settling time estimates as well as time domain switching results. Input and output impedance and overload responses are correctly modeled. The D.C. current drawn from supplies for a given value of I_Z is also correct.

Noise, PSRR and the temperature dependence of A.C. parameters such as frequency response and settling time are not modeled. Linearity and distortion results from the model will be worse than the real part by about a factor of three and do not show the correct frequency dependence. Also the A.C. results of the switch off isolation do not show degradation with frequency.

The macromodel is constructed from simple controlled sources, passive components and stripped transistor and diode models. As such it should be usable, perhaps with slight modification, on all but student or demonstration simulators where the model's size may be a problem.

Macromodel

```
Circuit Name: MACMOD6C - START OF DECK
IBGP 57 0 2.46m
IBGN 0 58 2.2m
IISWI 54 58 555u
IISWB 30 58 629u
IZSU 26 58 10u
DD100__D12 27 28 M1MP5DIODE AREA = 1
.MODEL M1MP5DIODE D TT = 60p IS = 1f CJO = 300f VJ = 600m XTI = 3 EG = 1.11 RS = 80m
DD99__D15 32 56 M1MP5DIODE AREA = 2
DD98__D11 24 25 M1MP5DIODE AREA = 1
DD97__D19 55 33 M1MP5DIODE AREA = 2
DD96__D18 33 55 M1MP5DIODE AREA = 2
DD95__D10 0 24 M1MP5DIODE AREA = 1
DD94__D13 0 29 M1MP5DIODE AREA = 1
DD93__D9 0 26 M1MP5DIODE AREA = 1
DD92__D14 56 32 M1MP5DIODE AREA = 2
DD91__D3 0 11 M1MP5DIODE AREA = 8
DD90__D4 47 12 M1MP5DIODE AREA = 8
DD89__D8 46 21 M1MP5DIODE AREA = 8
DD88__D7 0 20 M1MP5DIODE AREA = 8
QQ87__Q5 44 62 37 58 M2MPNP1 AREA = 2
.MODEL M2MPNP1 PNP CJC = 1.79p TF = 50.16666666666 7p IS =1f BF = 90 CJS = 480f
QQ86__Q6 45 61 37 58 M2MPNP1 AREA = 2
QQ85__Q14 0 32 49 58 M2MPNP1 AREA = 400m
QQ84__Q13 0 32 48 58 M2MPNP1 AREA = 400m
QQ83__Q1 0 9 61 58 M2MPNP1 AREA = 2
QQ82__Q2 0 9 62 58 M2MPNP1 AREA = 2
QQ81__Q8 45 62 36 58 M2MPNP1 AREA = 2
QQ80__Q7 44 61 36 58 M2MPNP1 AREA = 2
QQ79__Q11 45 59 35 58 M3MNPN1 AREA = 2
.MODEL M3MNPN1 NPN CJC = 1.3p TF = 120p IS = 1.3f BF = 150 CJS = 480f
QQ78__Q16 0 33 51 58 M3MNPN1 AREA = 400m
QQ77__Q15 0 33 50 58 M3MNPN1 AREA = 400m
QQ76__Q3 0 18 59 58 M3MNPN1 AREA = 2
QQ75__Q4 0 18 60 58 M3MNPN1 AREA = 2
QQ74__Q9 45 60 34 58 M3MNPN1 AREA = 2
QQ73__Q10 44 59 34 58 M3MNPN1 AREA = 2
QQ72__Q12 44 60 35 58 M3MNPN1 AREA = 2
```

Macromodel — Contd.

```
FI71 57 58 VFI7I 21
VFI7I 73 58 0.0
F170 59 58 VFI70 1
VFI70 72 41 0.0
FI69 60 58 VFI69 1
VFI69 41 42 0.0
FI68 43 58 VFI68 1
VFI68 42 73 0.0
FI67 33 32 VFI67 1
VFI67 31 0 0.0
FI66 57 40 VFI66 1
VFI66 39 72 0.0
FI65 57 62 VFI65 1
VFI65 38 39 0.0
FI64 26 65 VFI64 1
VFI64 74 24 0.0
F163 31 0 VFI63 1
VFI63 28 30 0.0
FI62 0 31 VFI62 1
VFI62 29 30 0.0
FI61 34 58 VFI61 1
VFI61 70 71 0.0
FI60 35 58 VFI60 1
VFI60 69 70 0.0
FI59 57 36 VFI59 1
VFI59 67 68 0.0
FI58 57 37 VFI58 1
VFI58 68 69 0.0
FI57 57 61 VFI57 1
VFI57 71 38 0.0
FI56 61 62 VFI56 500m
VFI56 1 2 0.0
FI55 59 60 VFI55 500m
VFI55 2 3 0.0
FI54 36 37 VFI54 500m
VFI54 5 6 0.0
FI53 35 34 VFI53 500m
VFI53 6 7 0.0
FI52 0 10 VFI52 1
VFI52 11 13 0.0
FI51 10 0 VFI51 1
VFI51 12 13 0.0
FI50 13 0 VFI50 2
VFI50 65 66 0.0
FI49 22 0 VFI49 2
VFI49 66 67 0.0
FI48 19 0 VFI48 1
VFI48 21 22 0.0
FI47 0 19 VFI47 1
VFI47 20 22 0.0
RR46__LOCATION 48 36 35 TC = 0 0
RR45__LOCATION 49 37 35 TC = 0 0
RR44__LOCATION 53 3 4.5 TC = 0 0
RR43__RSU 58 0 16K TC = 0 0
RR42__LOCATION 45 4 100 TC = 0 0
RR41__LOCATION 44 8 100 TC = 0 0
RR40__LOCATION 34 51 35 TC = 0 0
RR39__LOCATION 35 50 35 TC = 0 0
RR38__LOCATION 64 15 100 TC = 0 0
RR37__LOCATION 15 16 450 TC = 0 0
RR36__LOCATION 16 5 45 TC = 0 0
RR35__LOCATION 7 17 45 TC = 0 0
RR34__LOCATION 19 7 6.25 TC = 0 0
RR33__LOCATION 63 52 100 TC = 0 0
RR32__LOCATION 52 1 1.5K TC = 0 0
RR31__LOCATION 10 3 6.25 TC = 0 0
DD30__D6 23 0 M4MDCAP AREA = 6
.MODEL M4MDCAP D TT = 100n
CJO = 1p VJ = 800m RS = 200
DD29__D5 0 23 M4MDCAP AREA = 6
DD28__D1 0 14 M4MDCAP AREA = 12
DD27__D2 14 0 M4MDCAP AREA = 12
DD26__D16 0 32 M4MDCAP AREA = 12.5
DD25__D17 33 0 M4MDCAP AREA = 12.5
DD24__D23 18 43 M4MDCAP AREA = 4
DD23__D22 0 18 M4MDCAP AREA = 4
DD22__D21 9 0 M4MDCAP AREA = 4
DD21__D20 40 9 M4MDCAP AREA = 4
LL20__LOCATION 45 4 4n
LL19__LOCATION 44 8 4n
LL18__LOCATION 64 15 4n
LL17__LOCATION 15 5 71n
LL16 LOCATION 63 52 4n
LL15__LOCATION 52 1 71n
RR14__R6 23 15 156 TC = 824u 7.67u
RR13__R1 14 52 60 TC = 824u 7.67u
RR12__R12 0 54 500 TC = 824u 7.67u
EV11 0 55 0 43 1
EV10 27 0 54 0 1
EV9 25 0 26 0 1
EV8 56 0 40 0 1
EV7 47 0 10 0 650m
EV6 46 0 19 0 650m
XC5__XC4 15 0 CAP5M
.SUBCKT CAP5M 1 2
CC1 1 2 3.5e-13 TC = 0
.ENDS CAP5M
XC4__XC3 17 15 CAP6M
.SUBCKT CAP6M 1 2
CC1 1 2 9e-12 TC = 0
.ENDS CAP6M
XC3__XC2 52 0 CAP5M
XC2__XC1 53 52 CAP6M
.TEMP 50
.OP
.END
```

EL4083/EL4084
Current Mode Four Quadrant Multiplier

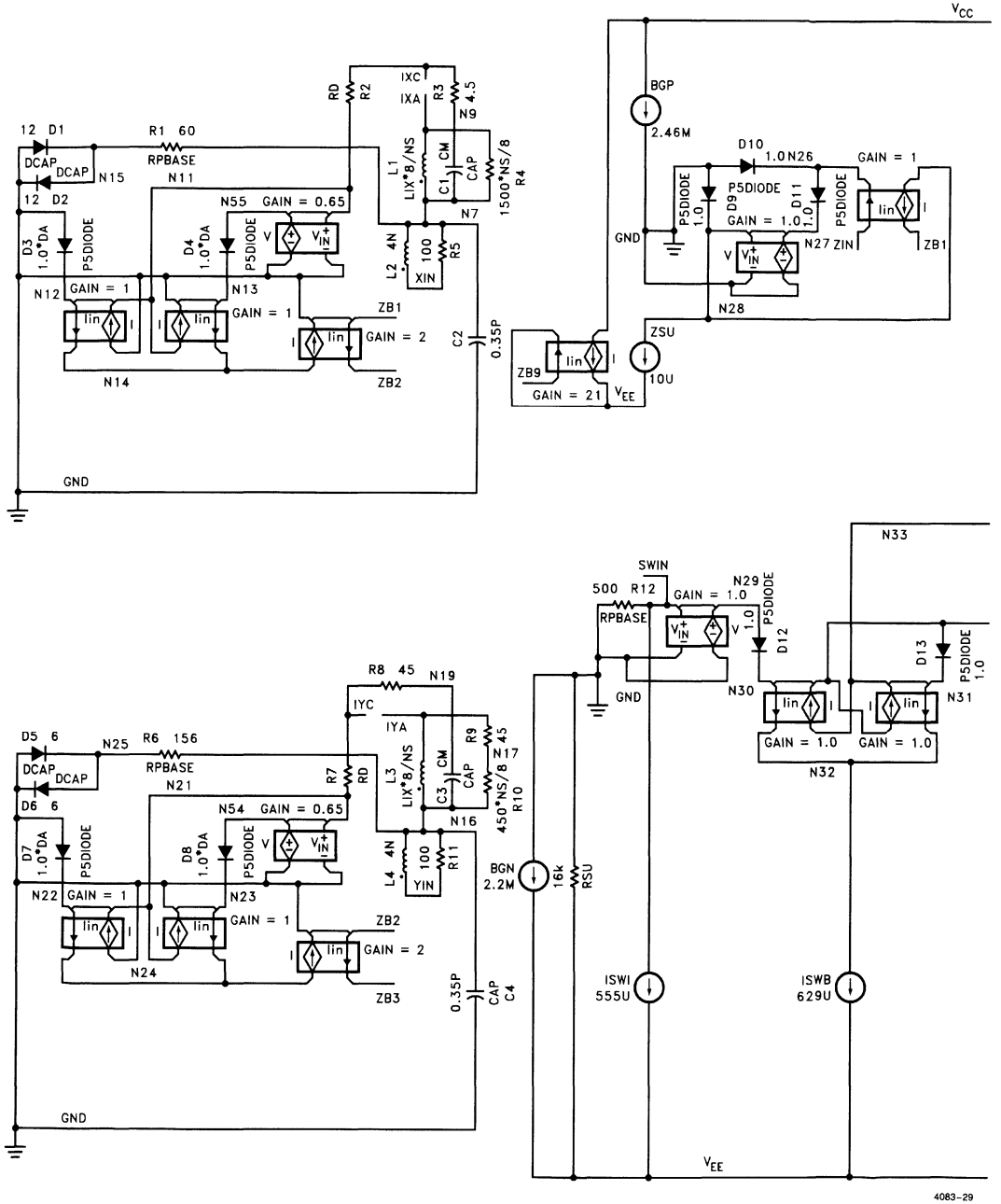
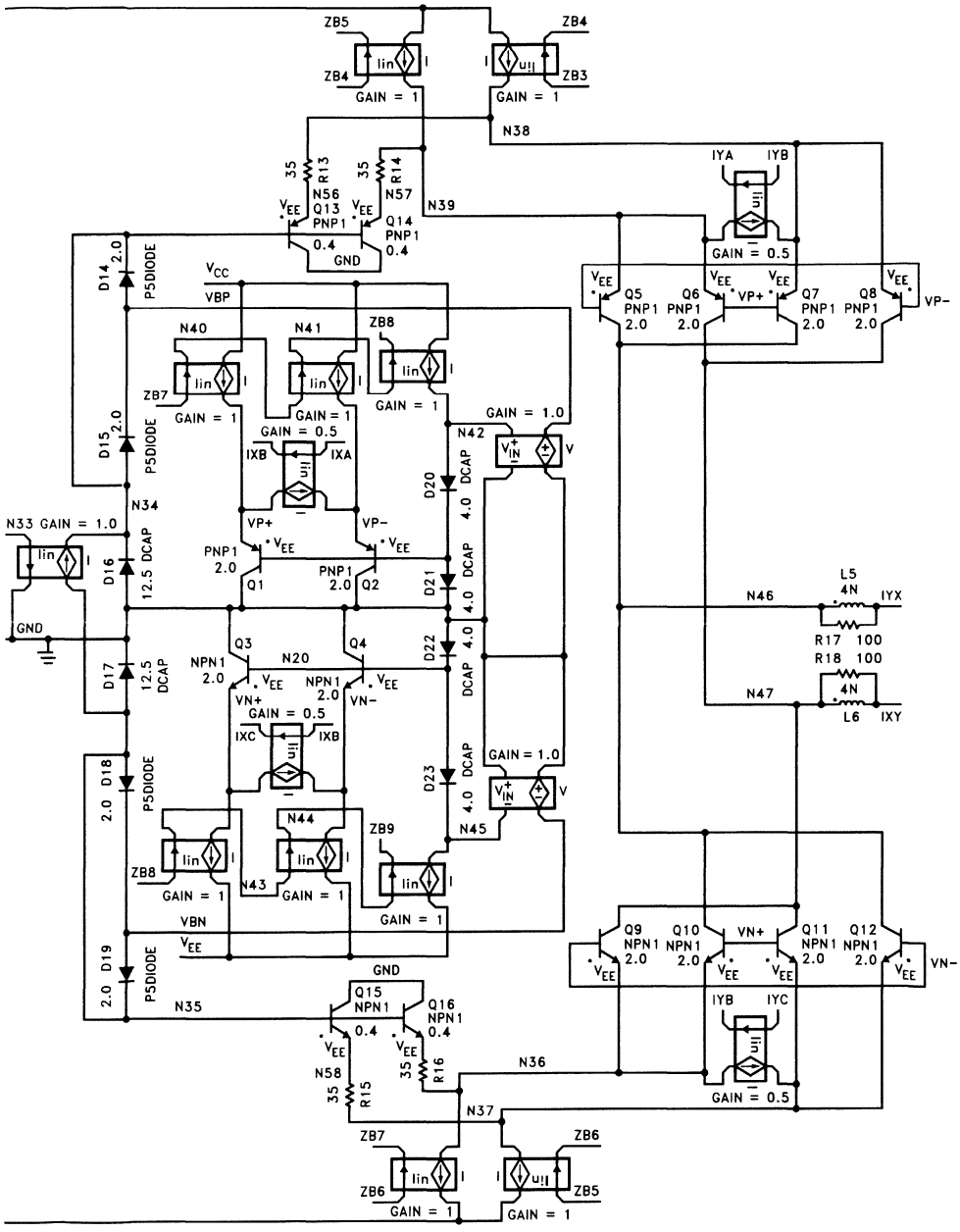


Figure 24. Macromodel



4083-30

Figure 24. Macromodel — Contd.

Introduction

Eight stand alone applications of the EL4083/EL4084 are presented in the parts' datasheet. These are four quadrant multiplication, squaring, mixing, modulating, demodulating, frequency doubling, gain control and video switching. All of these are possible with either of the two basic applications schematics (see datasheet Figures 22 and 23). Also included in the sheet is a detailed discussion of the parts' features and characteristics on a pin by pin basis in the general operating information section. This can be very useful in developing new applications or modifying the ones presented to perform a more specific task.

The applications presented in this note, except for the first divider circuit, are more elaborate designs that involve more than one multiplier or apply feedback around a multiplier. The examples chosen were either to demonstrate that the EL4083/EL4084 can perform one of the classic four quadrant multiplier applications or to show some of the design's unique capabilities. More applications are planned so contact Elantec if you want to be sure your revision of this note is the most current.

Division by Control of I_Z

In Figure 1, the I_Z pin is used as a denominator input to perform division. However, since the value of the current into the Z_{IN} pin also determines the input impedance and frequency response of all the inputs as well as the supply current of the part, this considerably restricts the computational range and accuracy of this approach. It is presented for its simplicity and can produce acceptable results for a 30 dB (~30-1) range of I_Z.

The key to this circuit is to run it from higher voltage supplies so that the input voltage ranges and the input resistors can be chosen large enough to minimize the input impedance modulation caused by a changing I_Z. The maximum value of I_Z is about 400 μA to stay within the power dissipation rating of the package. The frequency response of the denominator and the numerator inputs over a range of signal levels is shown in Figures 2 and 3 respectively. The circuit performs a multiplication as well as a division and obeys the transfer equation;

$$(Ixy - \overline{Ixy}) = Ix \times Iy/I_Z$$

See RMS #2 on page 4-67, and performance curves 10 and 11 in the datasheet for other hints on using the I_Z pin as an input signal. A second divider circuit using feedback with a 40 dB to 50 dB denominator range and differential numerator inputs is presented at the end of this note.

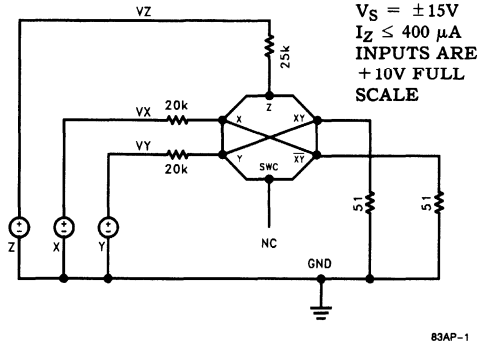


Figure 1. I_Z Divider

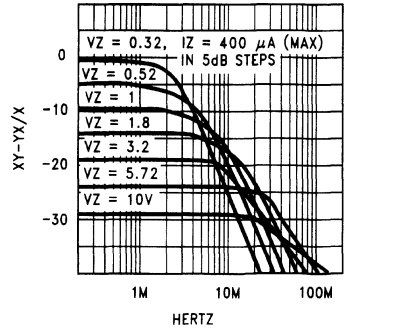


Figure 2. I_Z Divider Frequency Response of XIN for 5 dB D.C. Steps of V_Z

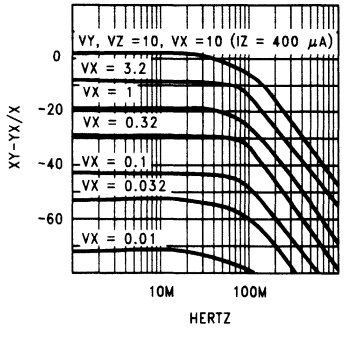


Figure 3. I_Z Divider Frequency Response of XIN for 10 dB D.C. Steps of V_X

Square Rooter

The circuit shown in Figure 4 calculates the function:

$V_{OUT} = \sqrt{(V_{IP} - V_{IN})}$, $V_{IP} - V_{IN} > 0$;
$V_{OUT} = 0$ for $V_{IP} - V_{IN} < 0$

Like the feedback divider circuit below, it has differential inputs. An unused input in either application can simply be omitted with its series resistor. The bandwidth of this circuit is proportional to the square root of the instantaneous input signal value (see Figure 5). The Ccomp capacitors are required for loop stability and their value is chosen to be appropriate to the output op amp selected. As a rule, the faster the op amp, the smaller the value that Ccomp needs to be and the wider the bandwidth of the circuit. The critical condition for stability is at the largest input signal level since this is where the loop will have its highest bandwidth.

A square root circuit can be thought of performing a signal compression function in that the output changes 1 dB in amplitude for every 2 dB amplitude change at the input. The Figure 4 circuit can process an input referred dynamic range of about 50 dB with good accuracy. This is limited mostly by the output referred offset of the multiplier. If more dynamic range or better accuracy is required, the optional trim network shown on the figure can be used.

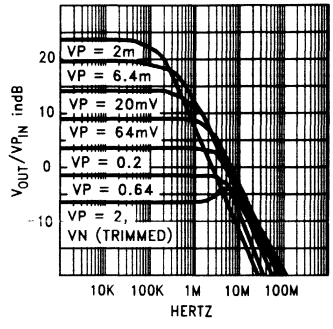


Figure 5. Gain/Frequency Response in 10 dB D.C. Steps at the Input

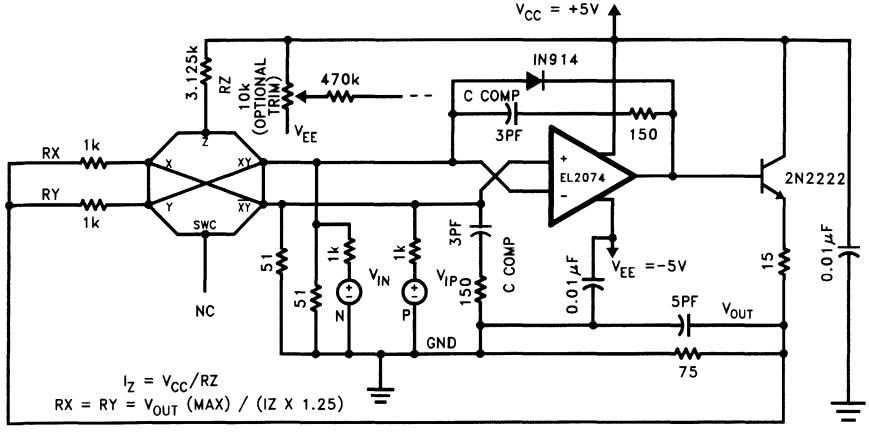


Figure 4. Fast Square Rooting Circuit (with Inverting and Non-inverting Inputs)

EL4083/EL4084
Current Mode Four Quadrant Multiplier Application Note

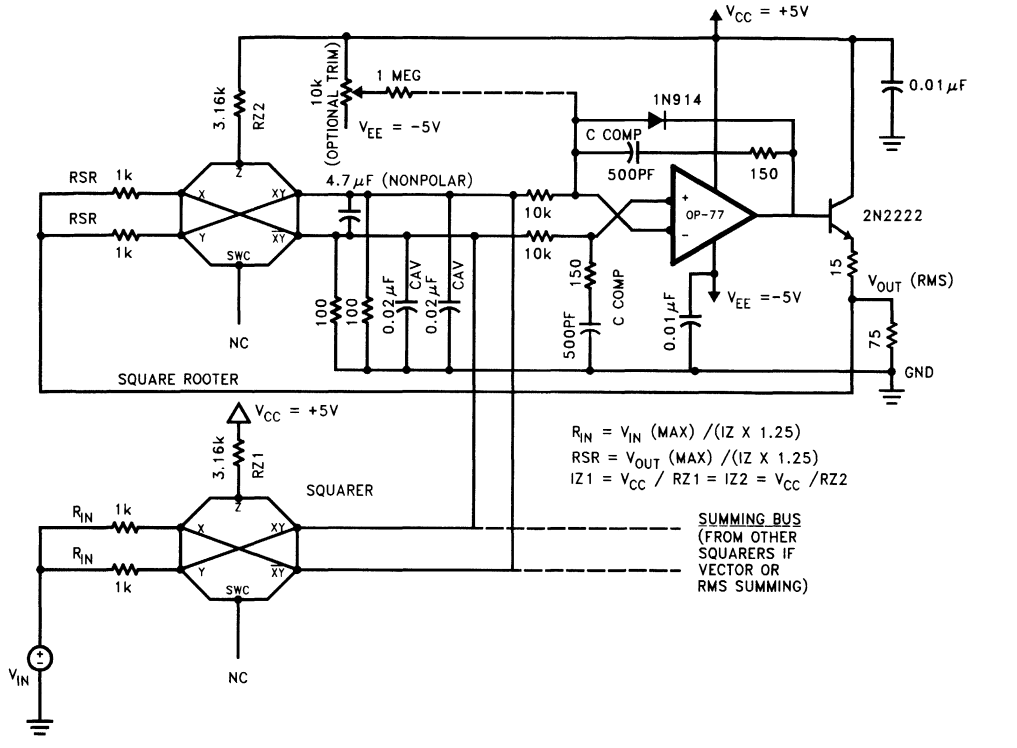


Figure 6. Wideband RMS (RMS #1) Computing Circuit

Wideband RMS Computing Circuit (RMS #1), Vector Addition-RMS Summing

Two 4083/84s can be used to calculate the root-mean-square of a wideband input signal (see Figure 6). The first multiplier calculates the mean square of the input signal by squaring and then averaging the output signal with capacitors. This signal, which is differential, is then processed by the square rooting circuit presented above. The squarer acts as a dynamic range expander in that its output changes 2 dB in level for every 1 dB change at the inputs. Its low level output referred errors limit the untrimmed system dynamic range performance to 30 dB or 40 dB. An optional trim network is shown in the applications figure.

The I_Z bias current of the squaring multiplier must be high enough so that the bandwidth of the squarer will pass the highest frequency of interest. The op amp in the square rooter need not be particularly fast since the squarer's output is immediately averaged by the capacitors. One may also need to provide D.C. blocking capacitors in front of the squarer to prevent offsets in the input signal source from causing errors. Figure 7 shows the response of the circuit to a 10 MHz signal burst. The "lazy" tail of the decay waveform is caused by the bandwidth of the square root circuit contracting with signal level. With the I_Z of the squaring multiplier at its maximum of 1.6 mA, the system is accurate for input frequencies up to 100 MHz.

The outputs of additional squaring multipliers can be summed into the averaging nodes which are inputs to the square root circuit. The value computed is;

Vvectsum =

$$\sqrt{\text{avg}\,(V_1 \times V_1) + (V_2 \times V_2) + \ldots + (V_n \times V_n)}$$

This is the RMS or vector sum of inputs V_1 to V_n.

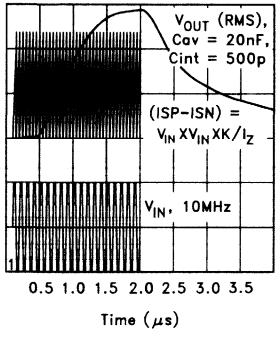


Figure 7. RMS #1 Response to a 10 MHz Signal Burst

Single Multiplier Implicit RMS Computing Loop (RMS #2)

The circuit of Figure 8 uses the I_Z pin of the EL4083/EL4084 as a divisor input to perform the implicit computation:

$$V_{RMS} = \text{avg}\,(V_{IN} \times V_{IN}) / V_{RMS}$$

Note that the averaging function is provided by a capacitor at the noninverting current output which sources positive current only since the part is performing a squaring function. This point is then connected to the I_Z input through a resistor which completes the computing loop. The inverting current output is fed to the virtual ground input of an op amp where it is averaged and converted to a buffered voltage.

The fact that one is using a current output to drive the I_Z pin overcomes the problem that the voltage on the pin is not constant at low driving currents (see datasheet Figure 10). However, other problems associated with using the I_Z pin as a signal input, notedly the bandwidth and multiplier input impedance dependence on I_Z, remain.

The IZO resistor provides a default current into the I_Z pin to prevent the bandwidth from collapsing and the input impedances from becoming too high as the signal amplitude goes to zero. The value of this current is determined by the application as a trade off between dynamic range and accuracy on the one hand and bandwidth and input impedance modulation, which also affects accuracy, on the other. Figure 9 shows the circuit's response to a signal burst. Note the effect of bandwidth modulation when the output is near zero. This circuit can be quite useful over about a 20 dB to 30 dB dynamic range given these limitations.

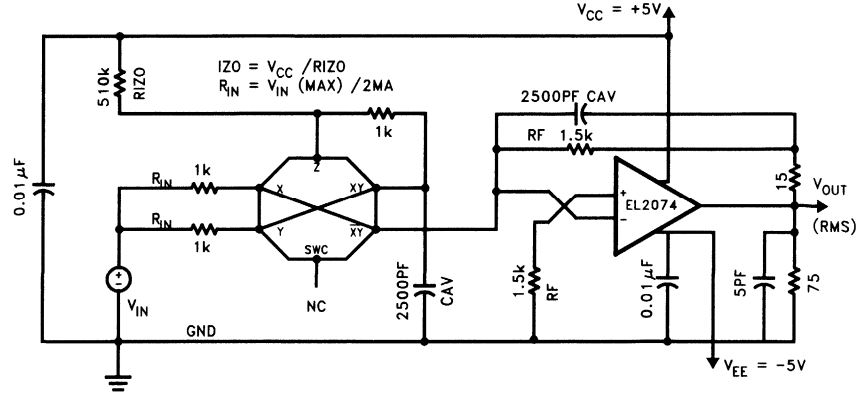


Figure 8. Single Multiplier Implicit RMS Computing Loop (RMS #2)

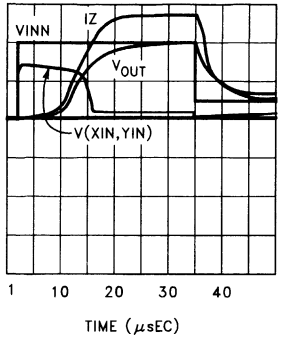


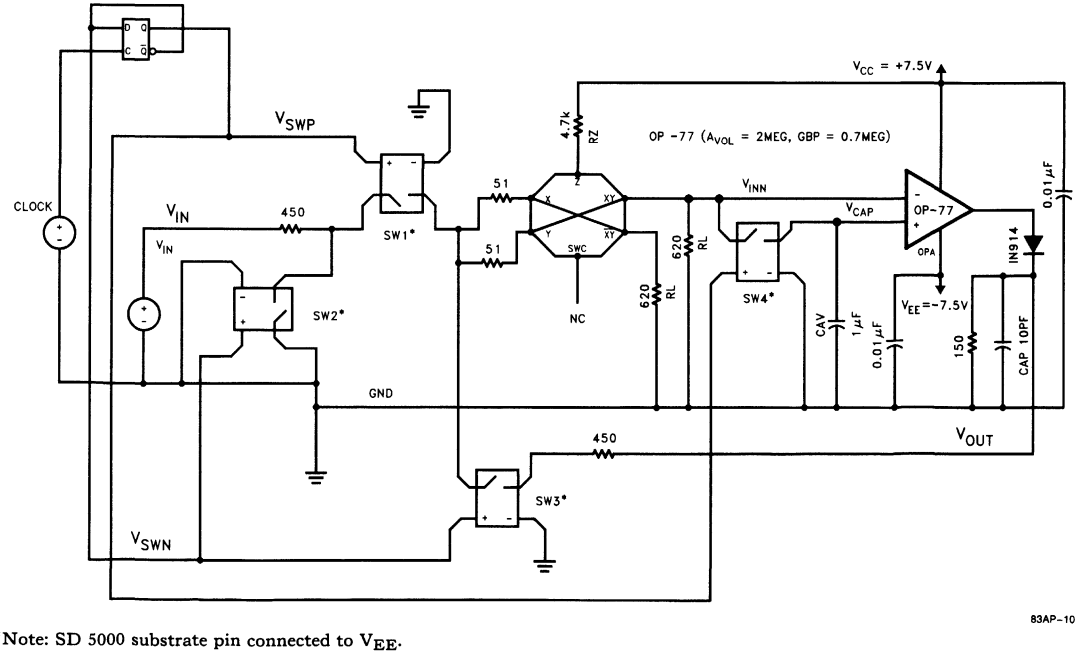
Figure 9. RMS #2 Singal Burst Response

Single Multiplier Switched RMS Circuit (RMS #3)

The circuit of Figure 10 operates by switching alternately between two modes of operation. The first computes the mean square of the input and the second computes the square root of this value. The output value is not valid until it is settled at the end of the second phase. This circuit is useful in applications which do not require continuous monitoring of an input signal as in digital metering. It would be inappropriate, for example, as the level detection portion of an AGC circuit since a sudden level change could go uncorrected for as much as a full computing cycle.

The major advantage of this circuit is the improvement in accuracy achieved by having the same inputs of the same multiplier do both the mean square and the square root computations. The gains are therefore identical and the effects of the offsets tend to cancel out. A high gain low offset op amp like the OP-77 is recommended at the output for the best results. Inexpensive switches such as the standard CMOS 4000 series can be used for input frequencies up to about 10 MHz. The Siliconix SD5000 series quad DMOS FET switches work well to over 200 MHz which is the maximum operating frequency of the EL4083/EL4084.

An Overall detection bandwidth of 100 MHz and a dynamic range of over 40 dB can be achieved with this circuit without trimming.



*Note: SD 5000 substrate pin connected to V_{EE}.

Figure 10. Single Multiplier Switched RMS Circuit
RMS #3 (SW1-4 are Siliconix SD5000 Series Quad DFETS for F_{IN} > 10 MHz)

Polynomial Functions (CRT Focus and Geometry Correction)

The current inputs and differential current outputs of EL4083/EL4084 lend these devices extremely well to the computation of high frequency polynomial functions. Two practical examples, CRT focus and geometry correction, are shown in Figures 11 and 12. The final outputs can be used single ended or recovered differentially as discussed in the Basic Product Functions section of the datasheet. Since seriesed 4083/84 multipliers are current mode devices, very little bandwidth is lost through a complex signal chain. This idea can be expanded to arbitrary weighted sums of first order terms, squares, cubes, cross products and perhaps higher order functions.

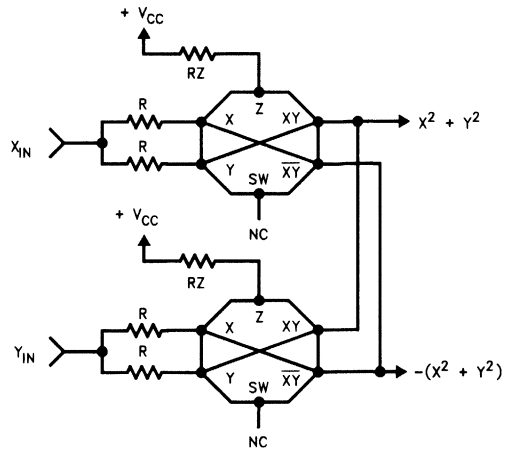


Figure 11. CRT Focus Correction

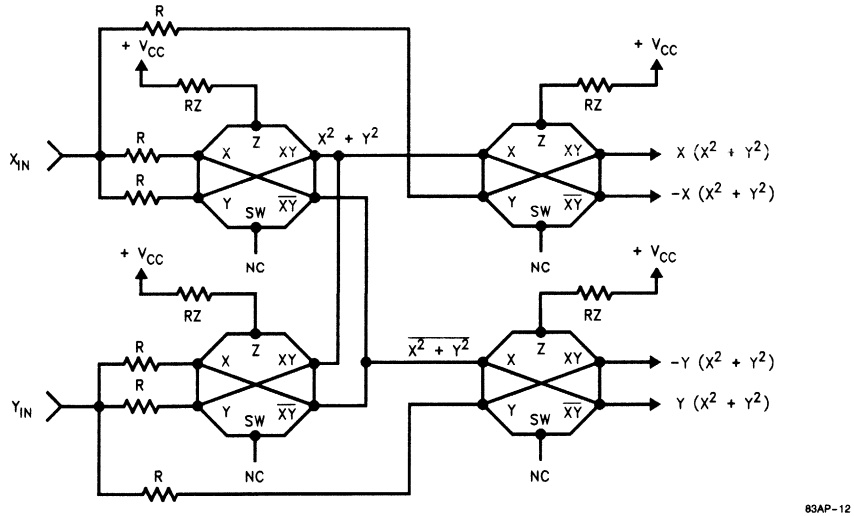


Figure 12. CRT Geometry Correction

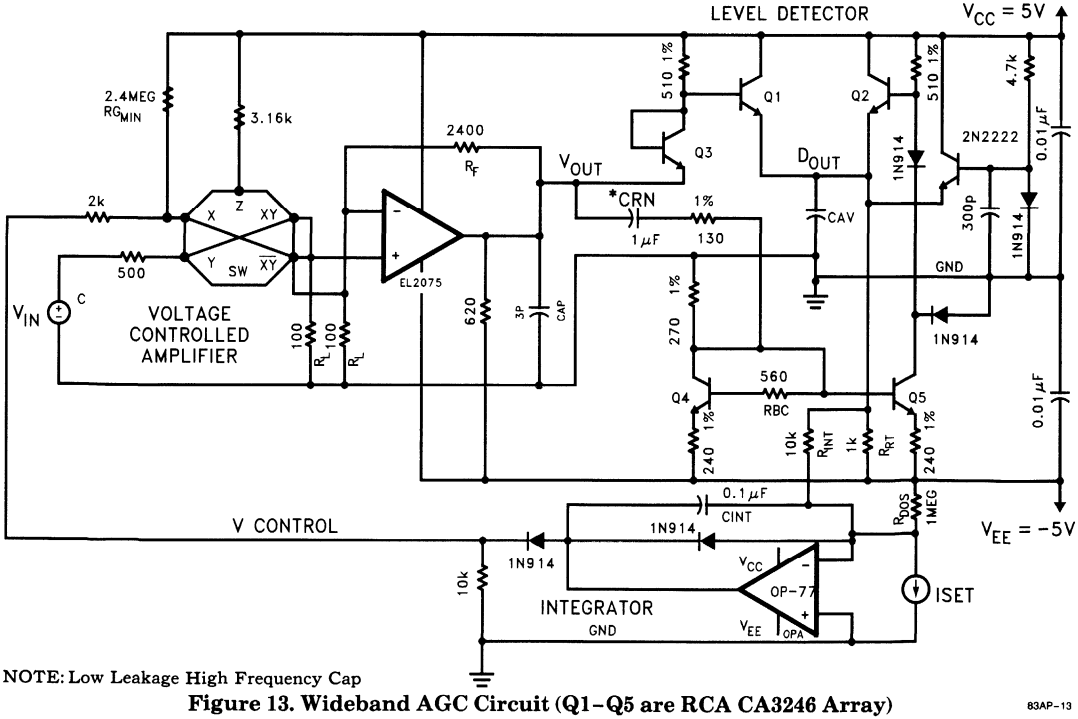
EL4083/EL4084
Current Mode Four Quadrant Multiplier Application Note

Wideband AGC Amplifier

The circuit in Figure 13 is a very wideband output regulating type AGC amplifier. It consists of a VCA (see datasheet Figure 23), a 100 MHz full wave rectifier/level detector and an op amp integrator. The level detector is built around the RCA CA3246 3 GHz Ft five transistor array. Transistors Q3 and Q1 rectify the positive portion of the output waveform while transistors Q4, Q5 and Q2 form an inverting amplifier which when connected to the output of Q1, completes the full wave rectifier. The Crn capacitor level shifts and D.C. blocks the signal into the input of the inverting amplifier. The Rbc resistor compensates for the effects of base currents. The 2N2222 acts as a negative clamp on the output of the inverting amplifier which enhances its speed. The Cav capacitor averages the rectified output and its value together with the value of the Rrt resistor determines the recovery time of the circuit to a signal level decrease. By connecting Rrt to the negative supply, bandwidth is maintained at low signal levels by keeping a D.C. standing current in Q1 and Q2. The nonzero value at D_{OUT} with zero input due to current density mismatches can be compensated at the intergator input by choosing the value of Rdos such that;

Rdos = V_{EE}*Rint/Vdos where Vdos is the zero input offset voltage.

The current source I_{SET}, which can be fixed or variable, determines the output level to which the AGC will try to regulate. The feedback is such that a level detected above this point will cause the integrator to reduce the forward gain. The diode at the integrator output insures that only positive voltages can be presented to the control input of the multiplier. This together with Rgmin, whose value determines the minimum forward gain, prevents gain foldback around a control input of zero.



*NOTE: Low Leakage High Frequency Cap

Figure 13. Wideband AGC Circuit (Q1–Q5 are RCA CA3246 Array)

83AP-13

The maximum forward gain of the signal path is 15 dB with a 3 dB bandwidth of 115 MHz. One can trade off bandwidth for more gain in the EL2075 in the usual manner by scaling the RL and RF resistor values. The 500Ω input resistor is appropriate for a full scale input voltage swing of ±1V and maximizes the the gain of the multiplier for this signal level. Figure 14 shows the regulated output vs input signal level over a range of values of I_{SET}.

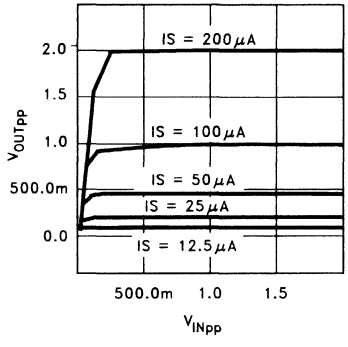


Figure 14. AGC Circuit Output Level Regulation vs Input Level at Several Values of I_{SET}

Controlled Signal Summer/Multiplexer and Video Fader/Switcher for HDTV

A circuit that can produce the controlled sum or mix of two input signals as well serve as a fast, high isolation 2-1 multiplexer is shown in Figure 15. This idea can be extended to any number of signal inputs if one keeps in mind that there will be some sacrifice of speed due to the summing of the device output capacitances. For producing either a final dual single ended or a differential recovered output, all the comments in the Basic product Functions section of the datasheet apply.

A video cross fader function can be realized by a slightly modified version of the Figure 15 circuit shown in Figure 16. Note that the control voltage is common to both multipliers and one control input is offset by the current in a resistor connected to the negative supply. A control voltage moving from ground to some positive maximum value will cause the output mix to go continuously from signal 2 only to signal 1 only. The negative D.C. offset on the control input of second multiplier would invert signal 2's polarity in the sum if it's outputs were not cross connected with the first. This circuit can also serve as a 2-1 multiplexer or a signal can be quickly and completely removed from the output mix if it's switch control is activated.

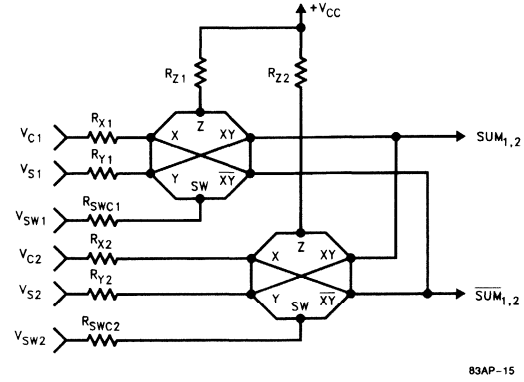


Figure 15. Controlled Signal Summer/Multiplexer

In Figure 17 a complementary current output DAC such as the DAC-08 or DAC-10 is used to provide the control currents for the cross fading function. Since the current outputs of the DAC are directly connected to the virtual ground inputs of the 4083s, the full current bandwidth of the DACs can be realized. The optional capacitor shown in the figure can be used to reduce switching transients if needed. The reference current for the DAC should be chosen to be equal to the full scale current selected for the multipliers. Note that the sense of both multiplier outputs have been flipped because of the negative only current sink outputs of the DAC.

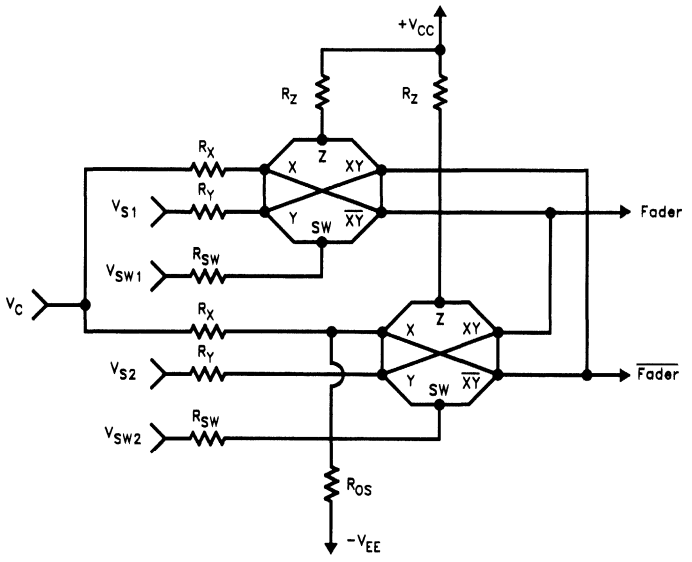
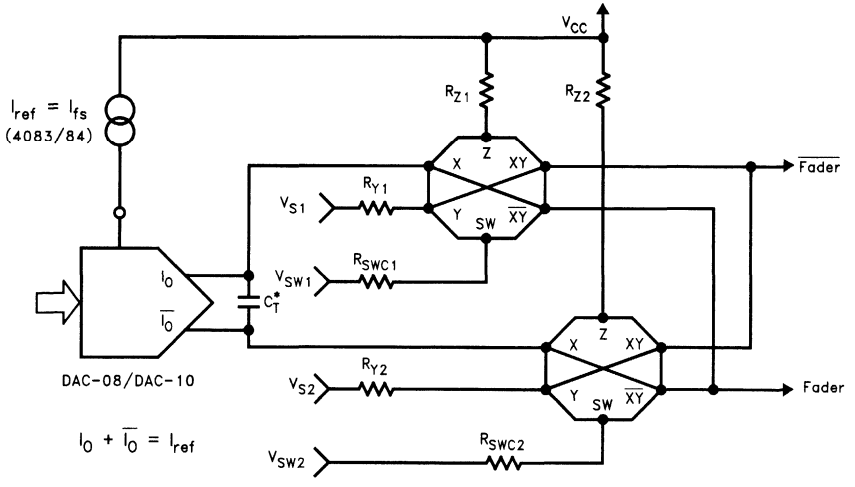


Figure 16. Fader/Switch (2-1)



*Optional Transient Filter Capacitor

Figure 17. Digitally Controlled Fader/Switch (2-1)

Feedback Divider

The circuit of Figure 18 performs the function $V_{OUT} = (Vzp - Vzn)/Vy$. This expression complies with the conventions established in the literature for such circuits and the Zs in the numerator should not be confused with the Z_{IN} pin which, in this example, is run at a constant (bias) current. This type of circuit is called a feedback divider.

Figure 19 shows the frequency response of the Z(numerator) inputs as a function of amplitude with I_Z = 1.6 mA and the Y(denominator) input at it's 2 mA maximum. The response is monotonic (no foldback) and has about a 50 dB to 60 dB range with good accuracy. The frequency response of the Y(denominator) input is shown in Figure 20. Note that the bandwidth is proportional to the value of the divider input. Since a division function has a singularity with the denominator at zero, a divider's performance will degrade as this value is approached. One can obtain about a 40 dB computational range with reasonable accuracy using an untrimmed part. If higher accuracy or greater range is required of this input, one can use the optional trim network shown in the figure.

The performance curves in Figures 19 and 20 are for I_Z = 1.6 mA. For lower values of I_Z the cutoff frequencies will be proportionally lower.

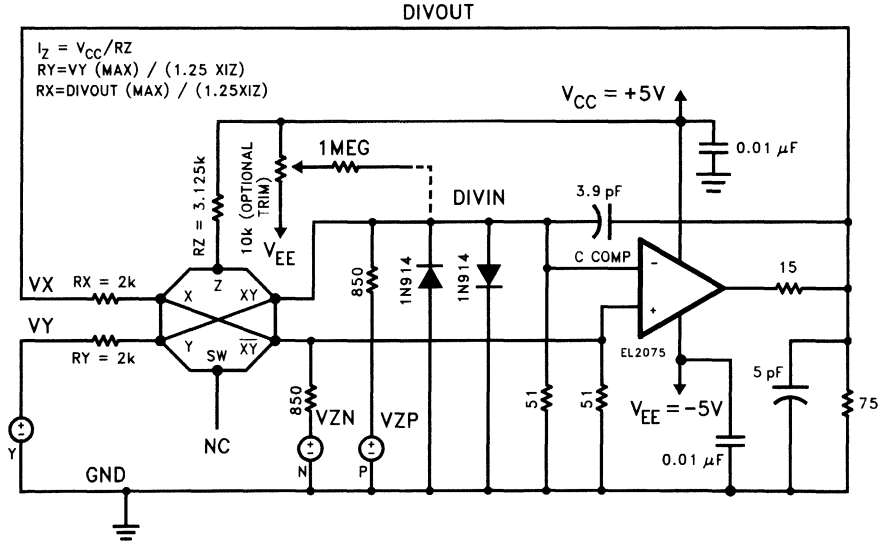


Figure 18. Fast Feedback Divider (with Inverting and Non-inverting Inputs)

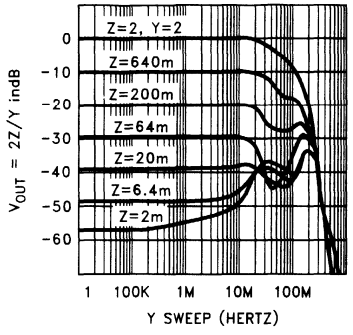


Figure 19. Divider Frequency Response (Denomination at Maximum, 10 dB Numerator Steps

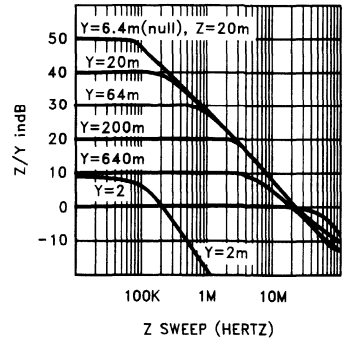


Figure 20. Divider Frequency Response (Numerator at −40 dB of Full Scale, Denominator in 10 dB Steps)

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4089C
DC Restored Video Amplifier

Features

- Complete video level restoration system
- 0.02% differential gain and 0.05° differential phase accuracy at NTSC
- 60 MHz bandwidth
- 0.1 dB flatness to 10 MHz
- V_S = ±5V to ±15V
- TTL/CMOS hold signal

Applications

- Input amplifier in video equipment
- Restoration amplifier in video mixers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4089CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL4089CS	0°C to +75°C	8-Lead SO	MDP0027

General Description

The EL4089C is an 8-pin complete DC-restored monolithic video amplifier sub-system. It contains a high quality video amplifier and a nulling, sample-and-hold amplifier specifically designed to stabilize video performance.

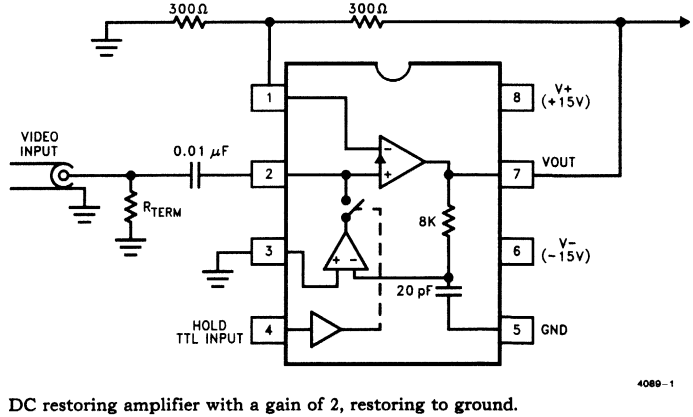
When the HOLD logic input is set to a TTL/CMOS logic 0, the sample- and-hold amplifier can be used to null the DC offset of the video amplifer.

When the HOLD input goes to a TTL/CMOS logic 1, the correcting voltage is stored on the video amplifier's input coupling capacitor. The correction voltage can be further corrected as need be, on each video line.

The video amplifier is optimized for video performance and low power. Its current feedback design allows the user to maintain essentially the same bandwidth over a gain range of nearly 10:1. The amplifier drives back-terminated 75Ω lines.

The EL4089C is fabricated in Elantec's proprietary Complementary Bipolar process which produces NPN and PNP transistors with equivalent AC and DC performance. The EL4089C is specified for operation over 0°C to +75°C temperature range.

Connection Diagram



DC restoring amplifier with a gain of 2, restoring to ground.

EL4089C
DC Restored Video Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	33V
Voltage between $V_{IN}+$, $S/H_{IN}+$, and GND pins	(V+) +0.5V to (V−) −0.5V
V_{OUT} Current	60 mA
Current into $V_{IN}-$ and HOLD Pins	5 mA
Internal Power Dissipation	See Curves
Operating Ambient Temperature Range	0°C to +75°C
Operating Junction Temperature	
Plastic DIP or SOL	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
DIP Package (Soldering, <10 Seconds)	300°C
SOL Package	
Vapor Phase (+60 Seconds)	215°C
Infrared (<15 Seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

Provisional Supplies at ±15V, Load = 1 kΩ; T_A = +25°C

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Amplifier Section (HOLD = 5V)							
V_{OS}	Input Offset Voltage	+25°C		12	25	II	mV
Ib+	IN+ Input Bias Current	+25°C		1	5	II	µA
Ib−	IN− Input Bias Current	+25°C		18	150	II	µA
R_{OL}	Transimpedance (Note 1)	+25°C	180	800		II	kΩ
$R_{IN}-$	IN− Resistance	+25°C		20		V	Ω
CMRR	Common Mode Rejection Ratio (Note 2)	+25°C	44	60		II	dB
V_O	Output Voltage Swing	+25°C	±12	±13		II	V
I_{SC}	Short Circuit Current (IN+ Only Driven to 0.5V)	+25°C	45	100		II	mA
Restore Section							
V_{OS}, Comp	Composite Input Offset Voltage (Note 3)	+25°C		3	7	II	mV
Ib+,r	Restore In+ Input Bias Current	+25°C		3	12	II	µA
I_{OUT}	Restoring Current Available	+25°C	180	300		II	µA
CMRR	Common Mode Rejection Ratio (Note 2)	+25°C	60	70		II	dB

Open Loop DC Electrical Characteristics — Contd.

Provisional Supplies at ±15V, Load = 1 kΩ; T_A = +25°C

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Restore Section —Contd.							
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C	60	90		II	dB
$V_{THRESHOLD}$	HOLD Logic Threshold	+25°C	0.8		2.0	II	V
I_{IH}, Hold	HOLD Input Current @ Logic High	+25°C		1	5	II	µA
I_{IL}, Hold	HOLD Input Current @ Logic Low	+25°C		5	15	II	µA
Supply Current							
Isy, Hold	Supply Current (HOLD = 5V)	+25°C	4.8	6.0	9.0	II	mA
Isy, Sampling	Supply Current (HOLD = 0V)	+25°C	5.0	6.5	11.0	II	mA

Closed Loop AC Electrical Characteristics

Provisional Supplies at ±15V, Load = 150Ω and 15 pF. R_f and R_g = 300Ω; A_V = 2, T_A = 25°C. (See Note 7 about Test Fixture)

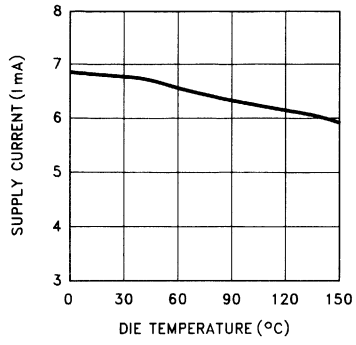
Parameter	Description		Min	Typ	Max	Test Level	Units
Amplifier Section							
SR	Slew Rate (Note 5)			500		V	V/µs
SR	Slew Rate with ±5V Supplies (Note 5)			275		V	V/µs
BW	Bandwidth	−3 dB		60		V	MHz
	±5V Supplies	−3 dB		55		V	MHz
BW	Bandwidth	±0.1 dB		25		V	MHz
	±5V Supplies	±0.1 dB		23		V	MHz
dG	Differential Gain	V_S = ±15V		0.02		V	%
	at 3.58 MHz (Note 6)	V_S = ±5V		0.03		V	%
dPh	Differential Phase	V_S = ±15V		0.05		V	°
	at 3.58 MHz (Note 6)	V_S = ±5V		0.06		V	°
Restore Section							
SR	Restore Amplifier Slew Rate (Test Circuit) 20%–80%			25		V	V/µs
T_{HE}	Time to Enable Hold			25		V	ns
T_{HD}	Time to Disable Hold			40		V	ns

Note 1: For current feedback amplifiers, $A_{VOL} = R_{OL}/R_{IN-}$.
Note 2: V_{CM} = ±10V for V_S = ±15V.
Note 3: Measured from S/H Input to amplifier output, while restoring.
Note 4: V_{OS} is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.
Note 5: SR measured at 20% to 80% of a 4V pk-pk square wave.
Note 6: DC offset from −0.714V through +0.714V, ac amplitude is 286 mVp-p, equivalent to 40 ire.
Note 7: Test fixture was designed to minimize capacitance at the IN− input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

EL4089C
DC Restored Video Amplifier

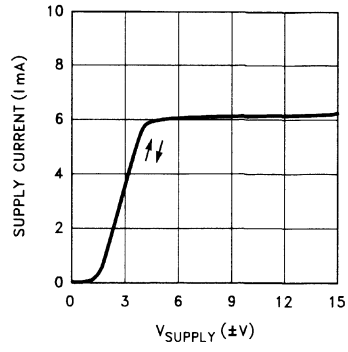
Typical Performance Curves

Supply Current vs Temperature
V_S = ±15V



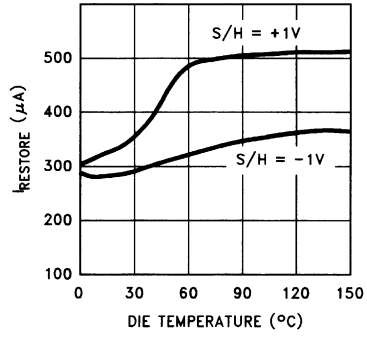
4089-2

Supply Current vs Supply Voltage



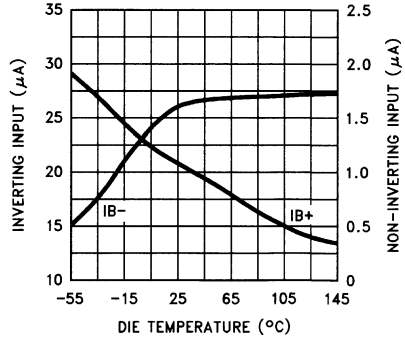
4089-3

Restoring Current vs Temperature



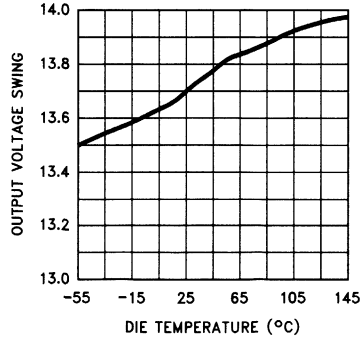
4089-4

Amplifier Input Current vs Die Temperature



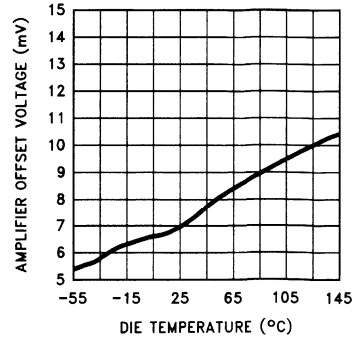
4089-5

Amplifier Output Voltage vs Die Temperature;
V_S = ±15V



4089-6

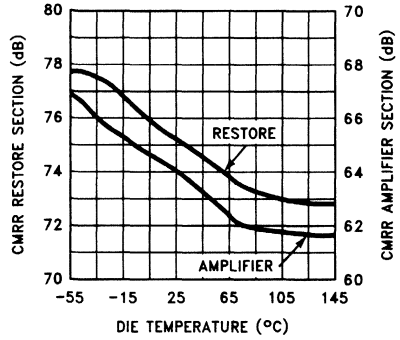
Amplifier Offset Voltage vs Die Temperature



4089-7

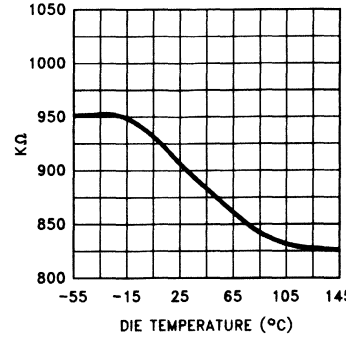
Typical Performance Curves — Contd.

CMRR for Amplifier and Restore Section vs Die Temperature



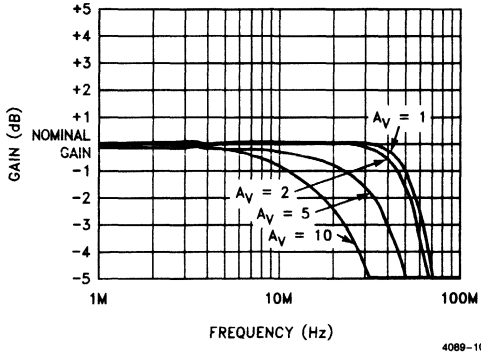
4089-8

Transimpedance (R_{OL}) vs Die Temperature



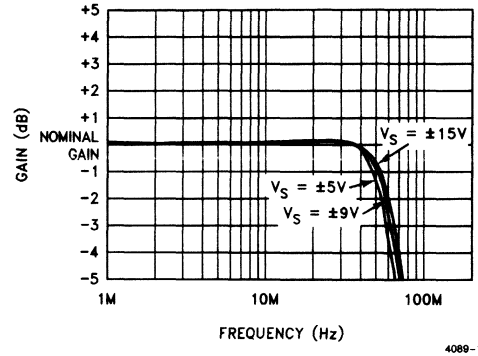
4089-9

Relative Frequency Response for Various Gains, R_F = 300Ω



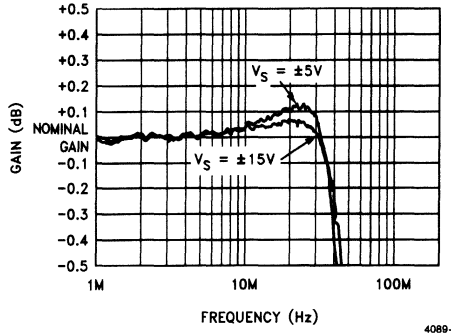
4089-10

Frequency Response vs Supply A_V = 2; R_F = 300



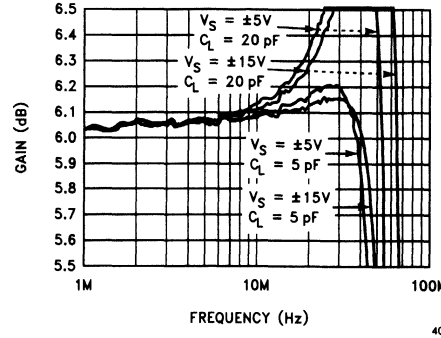
4089-11

Frequency Response Flatness vs Supply A_V = 2; R_F = 300



4089-12

Frequency Response Flatness for Various Load and Supply Conditions A_V = 2; R_F = 300

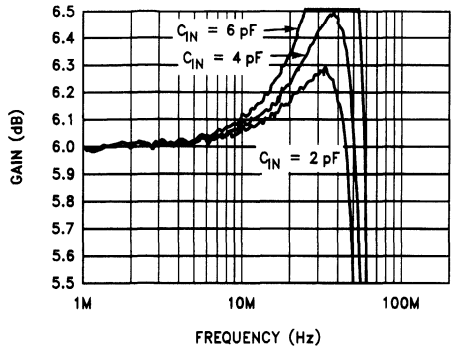


4089-13

EL4089C
DC Restored Video Amplifier

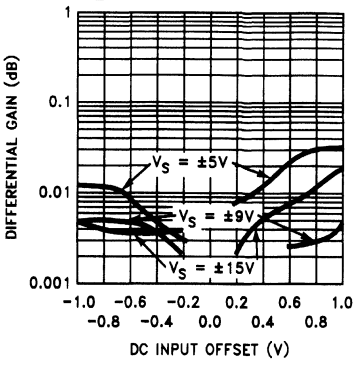
Typical Performance Curves — Contd.

Frequency Response Flatness vs C_{IN}–; A_V = 2; R_F = 300



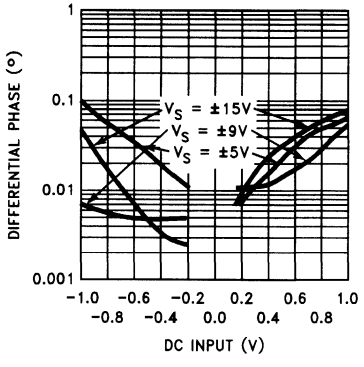
4089-14

Differential Gain vs DC Input Offset; A_V = 2, F_O = 3.58 MHz, R_L = 150Ω



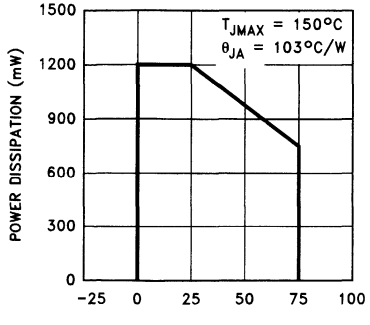
4089-15

Differential Phase vs DC Input Offset; A_V = 2; F_O = 3.58 MHz; R_L = 150Ω



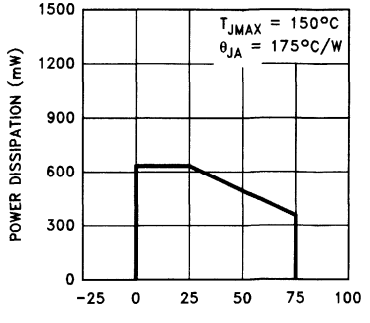
4089-16

8-Pin Plastic DIP Maximum Power Dissipation vs Ambient Temperature



4089-17

8-Lead SO Maximum Power Dissipation vs Ambient Temperature



4089-18

Typical Application

The EL4089 can be used to DC-restore a video waveform (see Fig. 1). The above circuit forces the cable driving video amplifier's output to ground when the HOLD pin is at a logic low.

The "correction voltage" is stored on capacitor CX1, an external ceramic capacitor. The capacitor value is chosen from the system requirements. The typical input bias current to the video amplifier is 1 μA, so for a 62 μs hold time, and a 0.01 μF capacitor, the output voltage drift is 6.2 mV in one line.

The S/H amplifier can provide a typical current of 300 μA to charge capacitor CX1, so with a 1.2 μs sampling time, the output can be corrected by 36 mV in each line.

Using a smaller value of CX1 increases both the voltage that can be corrected, and the drift while being held, likewise, using a larger value of CX1, reduces the voltages.

The RX1 resistor is in the circuit purely to simulate some external source impedance, and is not needed as a real component. Likewise for RX2. The 75Ω back terminating resistor RXT is recommended when driving 75Ω cables.

The board layout should have a ground plane underneath the EL4089, with the ground plane cut away from the vicinity of the V_{IN-} pin, (pin 1). This helps to minimize the stray capacitance on pin 1.

Power supply bypassing is important, and a 0.1 μF ceramic capacitor, from each power pin to ground, placed very close to the power pins, together with a 4.7 μF tantalum bead capacitor, is recommended.

When both digital and Analog grounds are on the same board, the EL4089 should be on the Analog ground. The digital ground can be connected to the Analog ground through a 100Ω–300Ω resistor, near the EL4089. This allows the digital signal a return path, while preventing the digital noise from corrupting the analog ground.

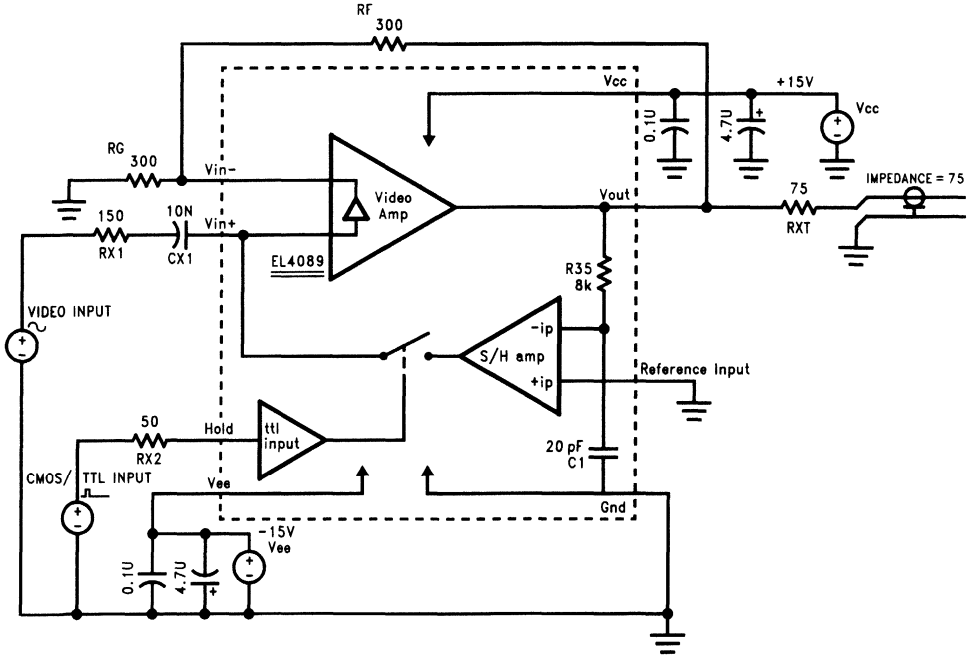


Figure 1

Table of Charge Storage Capacitor vs Droop Charging Rates

Cap Value nF	Droop in 60 μs mV	Charge in 1.2 μs mV	Charge in 4 μs mV
10	6	36	120
33	1.8	11	36
100	0.6	3.6	12

Basic formulae are:
V (droop) = Ib+ * (Line time − Sample time) / Capacitor
and V (charge) = I_{OUT} * Sample time / Capacitor

EL4094C
Video Gain Control/Fader

Features

- Complete video fader
- 0.02%/0.04° differential gain/phase @100% gain
- Output amplifier included
- Calibrated linear gain control
- ±5V to ±15V operation
- 60 MHz bandwidth
- Low thermal errors

Applications

- Video faders/wipers
- Gain control
- Video text insertion
- Level adjust
- Modulation

Ordering information

Part No.	Temp. Range	Package	Outline #
EL4094CN	−40°C to +85°C	8-Pin P-DIP	MDP0031
EL4094CS	−40°C to +85°C	8-Pin SO	MDP0027

General Description

The EL4094C is a complete two-input fader. It combines two inputs according to the equation:

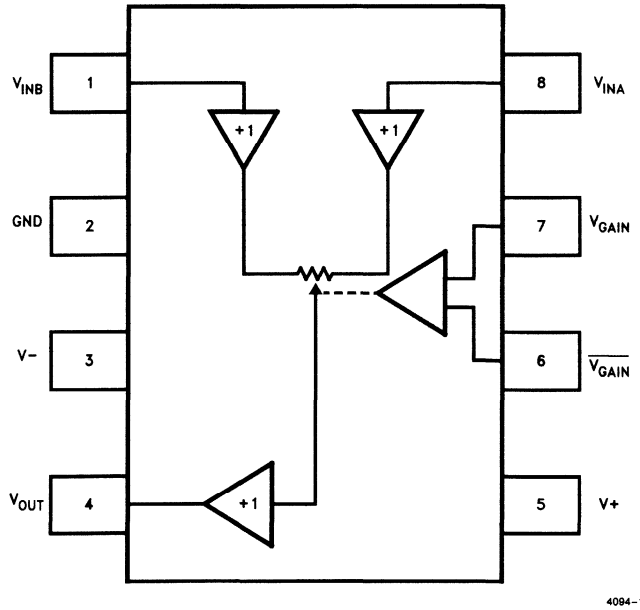
$$V_{OUT} = V_{INA}(0.5V + Vg) + V_{INB}(0.5V - Vg),$$

where V_{GAIN} is the difference between V_{GAIN} and $\overline{V_{GAIN}}$ pin voltages and ranges from −0.5V to +0.5V. It has a wide 60 MHz bandwidth at −3 dB, and is designed for excellent video distortion performance. The EL4094C is the same circuit as the EL4095, but with feedback resistors included on-chip to implement unity-gain connection. An output buffer is included in both circuits.

The gain-control input is also very fast, with a 20 MHz small-signal bandwidth and 70 ns recovery time from overdrive.

The EL4094C is compatible with power supplies from ±5V to ±15V, and is available in both the 8-pin plastic DIP and SO-8.

Connection Diagram



EL4094C
Video Gain Control/Fader

Absolute Maximum Ratings (T_A = 25°C)

V_S+	Voltage between V_S+ and GND	+18V
V_S	Voltage between V_S+ and V_S-	+33V
V_{INA}, V_{INB}	Input Voltage	(V_S-) −0.3V to (V_S+) +0.3V
V_{GAIN}	Input Voltage	$\overline{V_{GAIN}}$ ±5V
$\overline{V_{GAIN}}$	Input Voltage	V_S- to V_S+
I_{OUT}	Output Current	±35 mA

	Internal Power Dissipation	See Curves
T_A	Operating Ambient Temp. Range	−40°C to +85°C
T_J	Operating Junction Temperature	150°C
T_{ST}	Storage Temperature Range	−65°C to +150°C
T_{LD}	Lead Temperature (Soldering <10 sec.)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, T_A = 25°C, V_{GAIN} = +0.6V to measure channel A, V_{GAIN} = −0.6V to measure channel B, $\overline{V_{GAIN}}$ = 0V, unless otherwise specified

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
V_{OS}	Input Offset Voltage		4	20	I	mV
I_{B+}	V_{IN} Input Bias Current		2	10	I	µA
PSRR	Power Supply Rejection Ratio	65	80		I	dB
EG	Gain Error, 100% Setting		−0.5	−0.8	I	%
V_{IN}	V_{IN} Range	(V−) +2.5		(V+) −2.5	I	V
V_O	Output Voltage Swing	(V−) +2.5		(V+) −2.5	I	V
I_{SC}	Output Short-Circuit Current	50	95	150	I	mA
V_{GAIN}, 100%	Minimum Voltage at V_{GAIN} for 100% Gain	0.465	0.5	0.535	I	V
V_{GAIN}, 0%	Maximum Voltage at V_{GAIN} for 0% Gain	−0.535	−0.5	−0.465	I	V
NL, Gain	Gain Control Non-linearity, V_{IN} = ±0.5V		1.5	4	I	%
NL, A_V = 1	Signal Non-linearity, V_{IN} = 0 to ±1V, V_{GAIN} = 0.55V		0.01		V	%
A_V = 0.5	Signal Non-linearity, V_{IN} = 0 to ±1V, V_{GAIN} = 0V		0.05		V	%
A_V = 0.25	Signal Non-linearity, V_{IN} = 0 to ±1V, V_{GAIN} = −0.25V		0.2	0.5	I	%
R_{GAIN}	Resistance between V_{GAIN} and $\overline{V_{GAIN}}$	4.6	5.5	6.6	I	kΩ
I_S	Supply Current	12	14.5	17	I	mA
F_T	Off-Channel Feedthrough		−75	−50	I	dB

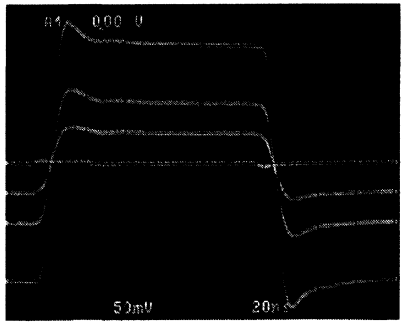
Closed Loop AC Electrical Characteristics

V_S = ±15V, C_L = 15 pF, T_A = 25°C, A_V = 100% unless otherwise noted

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
SR	Slew Rate; V_{OUT} from −3V to +3V measured at −2V and +2V	370	500		V	V/µs
BW	Bandwidth, −3 dB	45	60		III	MHz
	−1 dB		35		V	MHz
	−0.1 dB		6		V	MHz
dG	Differential Gain, AC amplitude of 286 mV_{p-p}					
	at 3.58 MHz on DC offset of −0.7, 0, and +0.7V A_V = 100%		0.02		V	%
	A_V = 50%		0.20		V	%
	A_V = 25%		0.40		V	%
dθ	Differential Phase, AC ampitude of 286 mV_{p-p}					
	at 3.58 MHz on DC offset of −0.7, 0, and +0.7V A_V = 100%		0.04		V	(°)
	A_V = 50%		0.20		V	(°)
	A_V = 25%		0.20		V	(°)
BW, GAIN	−3 dB Gain Control Bandwidth, V_{GAIN} Amplitude 0.5 V_{p-p}		20		V	MHz
T_{REC}, GAIN	Gain Control Recovery from Overload; V_{GAIN} from −0.6V to 0V		70		V	ns

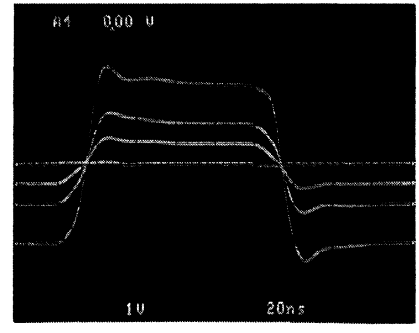
Typical Performance Curves

Small-Signal Step Response for Gain = 100%, 50%, 25%, and 0%. V_S ±5V



4094-2

Large-Signal Step Response for Gain = 100%, 50%, 25%, and 0%. V_S ±12V

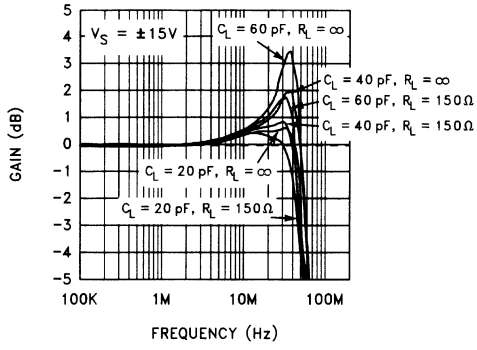


4094-3

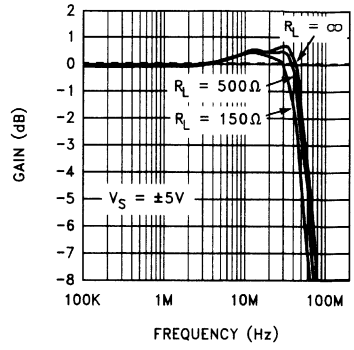
EL4094C
Video Gain Control/Fader

Typical Performance Curves — Contd.

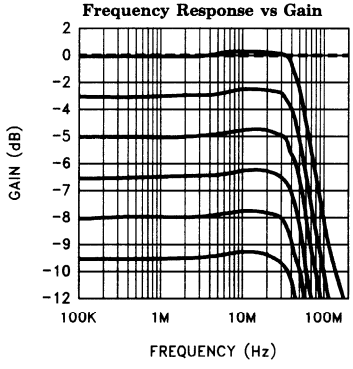
Frequency Response vs Capacitive Loading



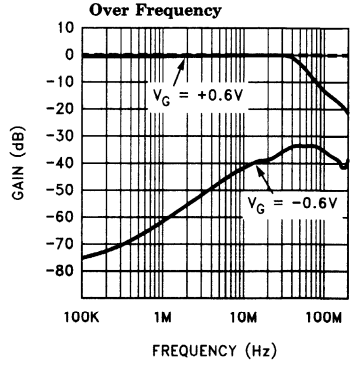
Frequency Response vs Resistive Loading



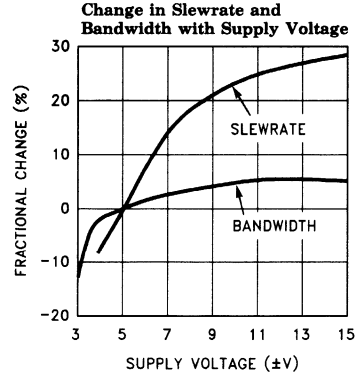
Frequency Response vs Gain



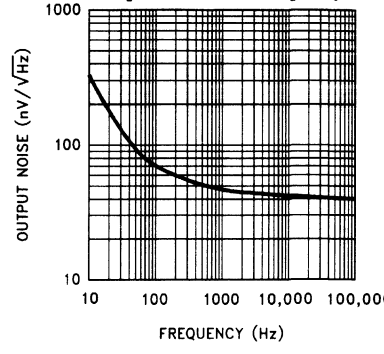
Off-Channel Isolation Over Frequency



Change in Slewrate and Bandwidth with Supply Voltage



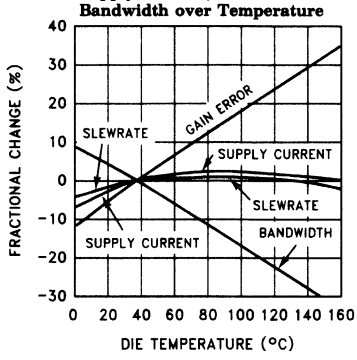
Output Noise Over Frequency



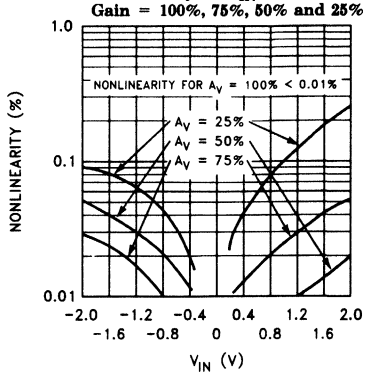
4094-4

Typical Performance Curves — Contd.

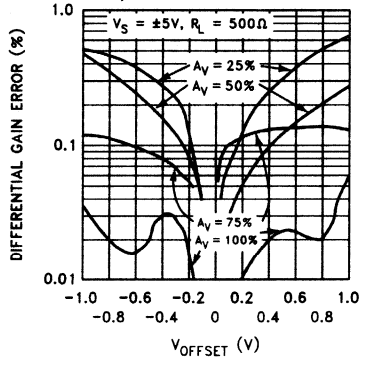
Change in 100% Gain Error, Supply Current, Slewrate and Bandwidth over Temperature



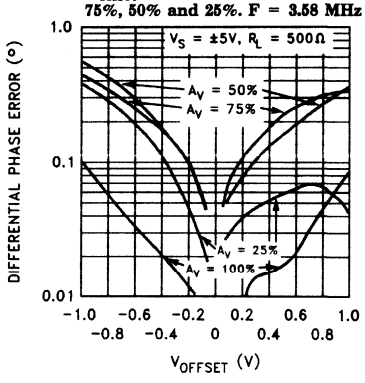
Nonlinearity vs V_{IN} for Gain = 100%, 75%, 50% and 25%



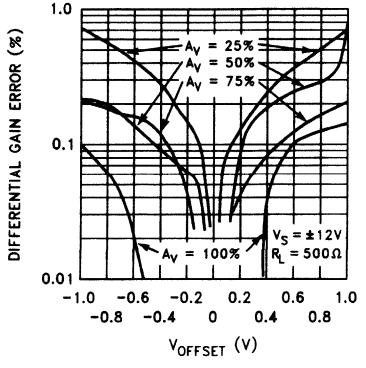
Differential Gain Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz



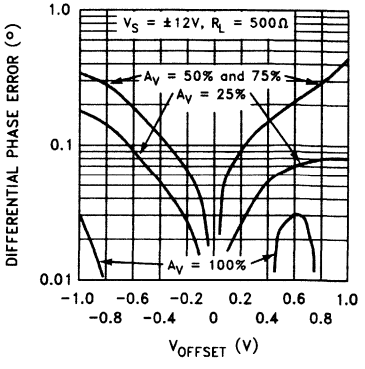
Differential Phase Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz



Differential Gain Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz



Differential Phase Error vs V_{offset} for Gain = 100%, 75%, 50% and 25%. F = 3.58 MHz

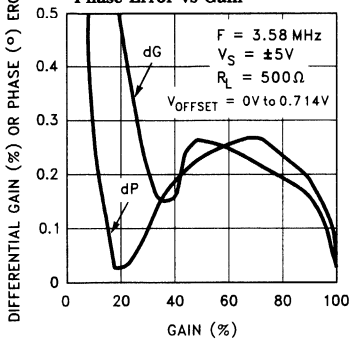


4094-5

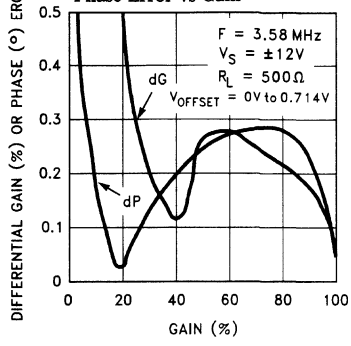
EL4094C
Video Gain Control/Fader

Typical Performance Curves — Contd.

Differential Gain and Phase Error vs Gain

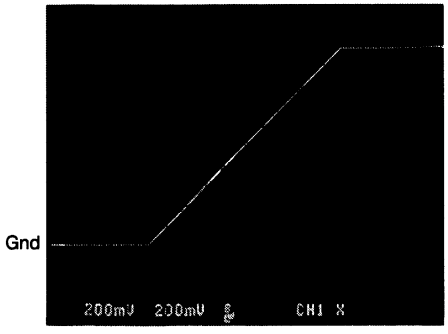


Differential Gain and Phase Error vs Gain



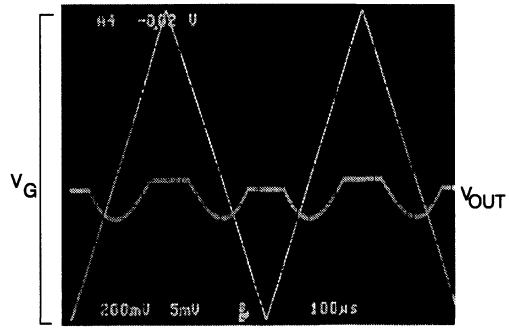
4094-6

Gain vs V_G. $1V_{DC}$ at V_{INA}



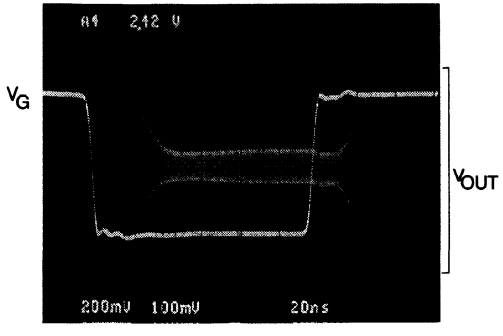
4094-7

Cross-Fade Balance. V_{INA} = V_{INB} = 0V



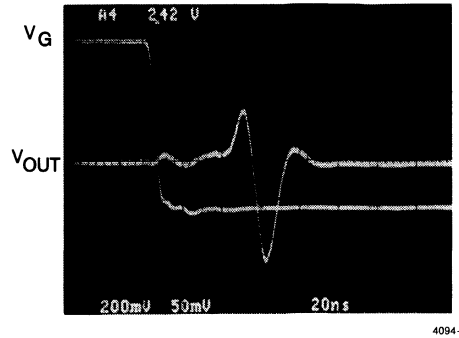
4094-8

Gain Control Response to a Non-Overloading Step, Constant Sinewave at V_{INA}



4094-9

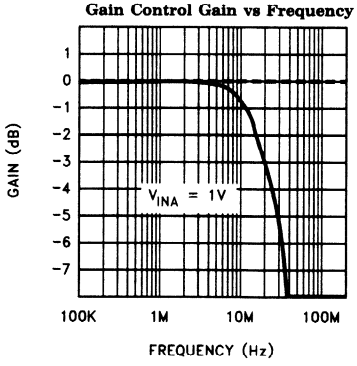
V_{GAIN} Overload Recovery Response



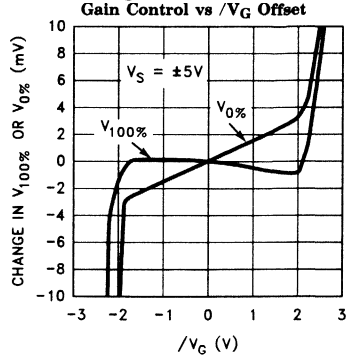
4094-10

Typical Performance Curves — Contd.

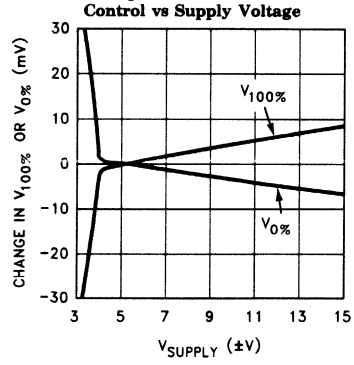
Gain Control Gain vs Frequency



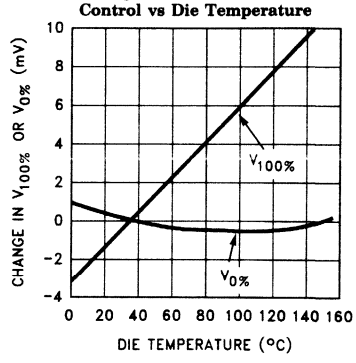
Change in V(100%) and V(0%) of Gain Control vs /V_G Offset



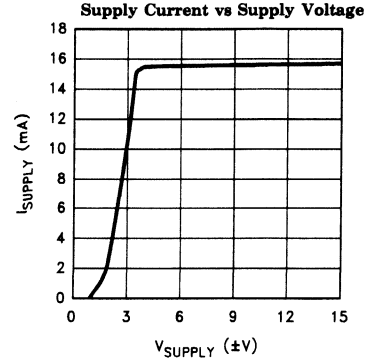
Change in V(100%) and V(0%) of Gain Control vs Supply Voltage



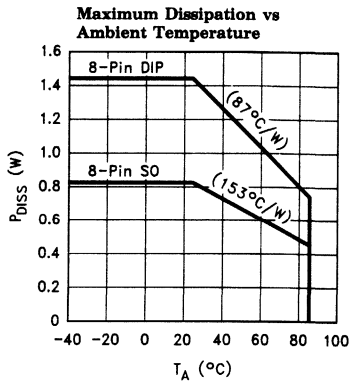
Change in V(100%) and V(0%) of Gain Control vs Die Temperature



Supply Current vs Supply Voltage



Maximum Dissipation vs Ambient Temperature



4094-11

EL4094C
Video Gain Control/Fader

Applications Information

The EL4094 is a self-contained and calibrated fader subsystem. When a given channel has 100% gain the circuit behaves as a current-feedback amplifier in unity-gain connection. As such, video and transfer distortions are very low. As the gain of the input is reduced, a 2-quadrant multiplier is gradually introduced into the signal path and distortions increase with reducing gain.

The input impedance also changes with gain setting, from about 1 MΩ at 100% gain down to 16 kΩ at zero gain. To maximize gain accuracy and linearity, the inputs should be driven from source impedances of 500Ω or less.

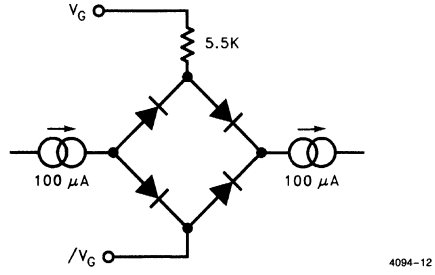
Linearity

The EL4094 is designed to work linearly with ±2V inputs, but lowest distortion occurs at ±1V levels and below. Errors are closer to those of a good current-feedback amplifier above 90% gain.

Low-frequency linearity is 0.1% or better for gains 25% to 100% and inputs up to 1V. NTSC differential gain and phase errors are better than 0.3% and 0.3° for the 25% to 100% gain range. These distortions are not strongly affected by supply voltage nor output loading, at least down to 150Ω. For settling to 0.1%, however, it is best to not load the output heavily and to run the EL4094 on the lowest practical supply voltages, so that thermal effects are minimized.

Gain Control Inputs

The gain control inputs are differential and may be biased at any voltage as long as $/V_{GAIN}$ is less than 2.5V below V+ and 3V above V−. The differential input impedance is 5.5 kΩ, and the common-mode impedance is more than 500 kΩ. With zero differential voltage on the gain inputs, both signal inputs have a 50% gain factor. Nominal calibration sets the 100% gain of V_{INA} input at +0.5V of gain control voltage, and 0% at −0.5V of gain control. V_{INB}'s gain is complementary to that of V_{INA}; +0.5V of gain control sets 0% gain at V_{INB} and −0.5V gain control sets 100% V_{INB} gain. The gain control does not have a completely abrupt transition at the 0% and 100% points. There is about 10 mV of "soft" transfer at the gain endpoints. To obtain the most accurate 100% gain factor or best attenuation at 0% gain, it is necessary to overdrive the gain control input by 30 mV or more. This would set the gain control voltage range as −0.565V to +0.565V, or 30 mV beyond the maximum guaranteed 0% to 100% range. In fact, the gain control inputs are very complex. Here is a representation of the terminals:



Representation of Gain Control Inputs V_G and $/V_G$

For gain control inputs between ±0.5V (±90 μA), the diode bridge is a low impedance and all of the current into Vg flows back out through/V_g. When gain control inputs exceed this amount, the bridge becomes a high impedance as some of the diodes shut off, and the V_g impedance rises sharply from the nominal 5.5KΩ to about 500KΩ. This is the condition of gain control overdrive. The actual circuit produces a much sharper overdrive characteristic than does the simple diode bridge of this representation.

The gain input has a 20 MHz −3 dB bandwidth and 17 ns risetime for inputs to ±0.45V. When the gain control voltage exceeds the 0% or 100% values, a 70 ns overdrive recovery transient will occur when it is brought back to linear range. If quicker gain overdrive response is required, the Force control inputs of the EL4095 can be used.

Output Loading

The EL4094 does not work well with heavy capacitive loads. Like all amplifier outputs, the output impedance becomes inductive over frequency resonating with a capacitive load. The effective output inductance of the EL4094 is about 350 nH. More than 50 pF will cause excessive frequency response peaking and transient ringing. The problem can be solved by inserting a low-value resistor in series with the load, 22Ω or more. If a series resistance cannot be used, then adding a 300Ω or less load resistor to ground or a "snubber" network may help. A snubber is a re-

Applications Information — Contd.

sistor in series with a capacitor, 150Ω and 100 pF being typical values. The advantage of a snubber is that it does not draw DC load current.

Unterminated coaxial line loads can also cause resonances, and they should be terminated either at the far end or a series back-match resistor installed between the EL4094 and the cable.

The output stage can deliver up to 140 mA into a short-circuit load, but it is only rated for a continuous 35 mA. More continuous current can cause reliability problems with the on-chip metal interconnect. Video levels and loads cause no problems at all.

Noise

The EL4094 has a very simple noise characteristic: the output noise is constant (40 nV/√Hz wideband) for all gain settings. The input-referred noise is then the output noise divided by the gain. For instance, at a gain of 50% the input noise is 40 nV/√Hz/0.5, or 80 nV/√Hz.

Bypassing

The EL4094 is fairly tolerant of power-supply bypassing, but best multiplier performance is obtained with closely connected 0.1 μF ceramic capacitors. The leaded chip capacitors are good, but neither additional tantalums nor chip components are necessary. The signal inputs can oscillate locally when connected to long lines or unterminated cables.

Power Dissipation

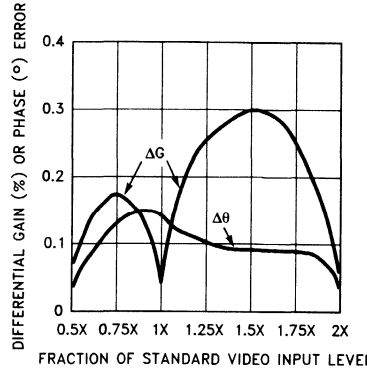
Peak die temperature must not exceed 150°C. At this temperature, the epoxy begins to soften and becomes unstable, chemically and mechanically. This allows 75°C internal temperature rise for a 75°C ambient. The EL4094 in the 8-pin PDIP package has a thermal resistance of 87°/W, and can thus dissipate 862 mW at a 75°C ambient temperature. The device draws 17 mA maximum supply current, only 510 mW at ±15V supplies, and the circuit has no dissipation problems in this package.

The SO-8 surface-mount package has a 153°/W thermal resistance with the EL4094, and only 490 mW can be dissipated at 75°C ambient temperature. The EL4094 thus cannot be operated with ±15V supplies at 75°C in the surface-mount package; the supplies should be reduced to ±5V to ±12V levels, especially if extra dissipation occurs when driving a load.

The EL4094 as a Level Adjust

A common use for gain controls is as an input signal leveller—a circuit that scales too-large or too-small signals to a standard amplitude. A typical situation would be to scale a variable video input by +6 dB to −6 dB to obtain a standard amplitude. The EL4094 cannot provide more than 0 dB gain, but it can span the range of 0 dB to −12 dB with another amplifier gaining the output up by 6 dB. The simplest way to obtain the range is to simply ground the B input and vary the gain of the signal applied to the A input. The disadvantage of this approach is that linearity degrades at low gains. By connecting the signal to the A input of the EL4094 and the signal attenuated by 12 dB to the B input, the gain control offers the highest linearity possible at 0 dB and −12 dB extremes, and good performance between. The circuit is shown on the following page.

The EL4095 can be used to provide the required gains without the extra amplifier. In practice, the gain control is adjusted to set a standard video level regardless of the input level. The EL4583 sync-separator has a recovered amplitude output that can be used to servo the gain control voltage. Here is the curve of differential gain and phase distortion for varying inputs, with the output set to standard video level:



Differential Gain and Phase of Linearized Level Control

EL4094C
Video Gain Control/Fader

Applications Information — Contd.

The differential gain error is kept to 0.3% and the differential phase to 0.15° or better over the entire input range.

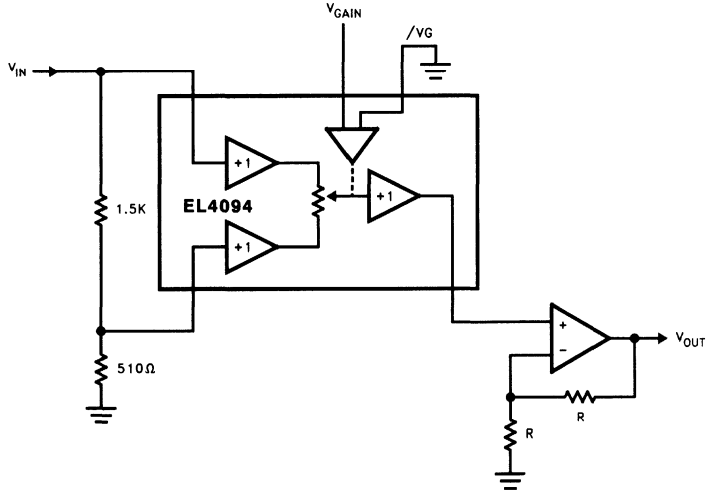
The EL4094 as an Adjustable Filter

Equalizers are used to adjust the delay or frequency response of systems. A typical use is to compensate for the high-frequency loss of a cable system ahead of the cable so as to create a flat response at the far end. A generalized scheme with the EL4094 is shown below.

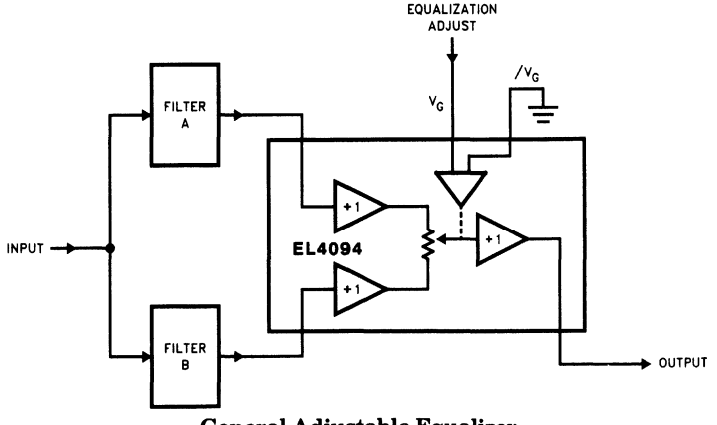
For an adjustable preemphasis filter, for instance, filter A might be an all-pass filter to compensate for the delay of filter B, a peaking filter. Fading the gain from A to B provides a variable amount of peaking, but constant delay.

The EL4094 as a Phase Modulator

To make a phase modulator, filter A might be a leading-phase network, and filter B a lagging network. The wide bandwidth of the gain-control input allows wideband phase modulation of the carrier applied to the main input. Of course, the carrier and gain inputs must not be digital but be reasonably clean sinewaves for the modulation to be accurate.



+6 dB to −6 dB Linearized Level Control



General Adjustable Equalizer

EL4094 Macromodel

This macromodel is offered to allow simulation of general EL4094 behavior. We have included these characteristics:

Small-signal frequency response
Output loading effects
Input impedance
Off-channel feedthrough
Output impedance over frequency

Signal path DC distortions
V_{GAIN} I-V characteristics
V_{GAIN} overdrive recovery delay
100% gain error

These will give a good range of results for various operating conditions, but the macromodel does not behave identically as the circuit in these areas:

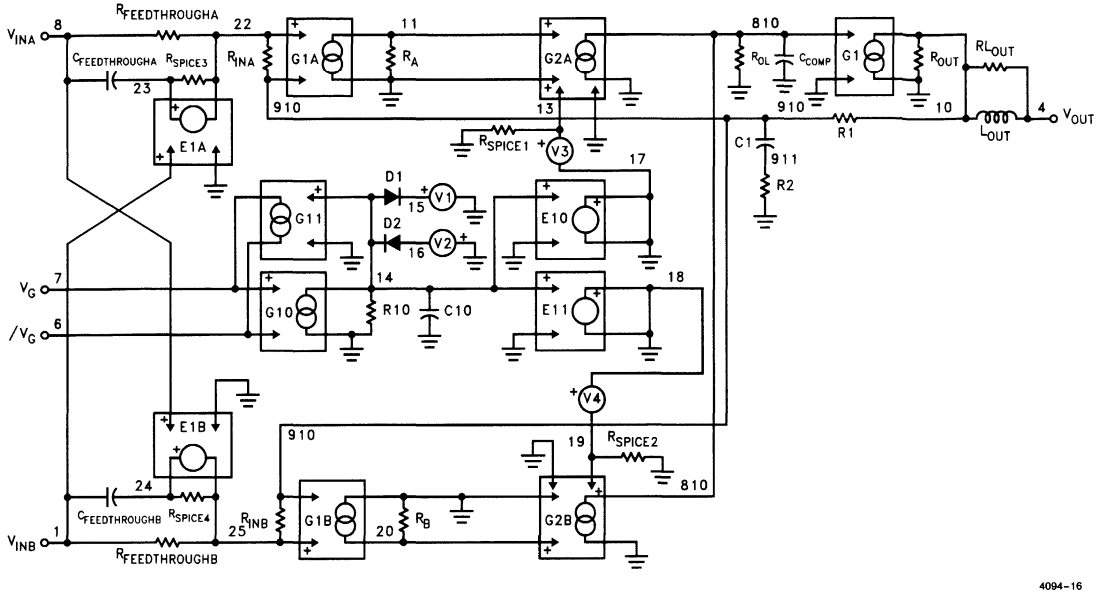
Temperature effects
Signal overload effects
Signal and $/V_G$ operating range
Current-limit
Video and high-frequency distortions
Supply voltage effects
Slewrate limitations
Noise
Power supply interactions

The macromodel's netlist is based on the Pspice simulator (copywritten by the Microsim Company). Other simulators may not support the POLY function, which is used to implement multiplication as well as square-low nonlinearities.

```
******
******
*                    VINB
*                    |    VOUT
*                    |    |    /VG
*                    |    |    |    VG
*                    |    |    |    |    VINA
*                    |    |    |    |    |
.subckt EL4094subckt (1    4    6    7    8)
***
ROL 810 0 290k
Ccomp 810 0 3.5p
G1 10 0 810 0 -10
ROUT 10 0 0.1
LOUT 10 4 350.200n
RLOUT 10 4 80
r1 10 910 10
c1 910 911 300p
r2 911 0 90
***
*** Input channel A
***
RINA 22 10 16k
ra 11 0 1k
Cfeedthrougha 23 8 130p
Rfeedthrougha 8 22 1.0
Ela 23 22 1 0 1.0
Rspice3 23 22 1E12
G1a 11 0 POLY(1) (22,910) 0.0 0.001 -3E-6
G2a 810 0 POLY(2) (11,0) (13,0) 0.0 0.0 0.0 0.0 0.001
***
***Input channel B
***
RINB 25 10 16k
rb 20 0 1k
Cfeedthroughb 24 1 130p
Rfeedthroughb 1 25 1.0
E1b 24 25 8 0 1.0
Rspice4 24 25 1E12
G1b 20 0 POLY(1) (25,910) 0.0 0.001 -3E-6
G2b 810 0 POLY(2) (20,0) (19,0) 0.0 0.0 0.0 0.0 0.001
***
***Gain control
***
Rspice1 13 0 1E12
Rspice2 18 0 1E12
R10 14 0 1E7
C10 14 0 8E-16
D1 14 15 Dclamp
D2 16 14 Dclamp
.model Dclamp D (TT=200n)
V1 15 0 4999.3
V2 0 16 4999.3
V3 13 17 0.5
V4 19 18 0.5
G10 14 0 7 6 -0.001
G11 7 6 14 0 -2E-8
E10 17 0 14 0 1E-4
E11 18 0 14 0 -1E-4
***
.ends
******
```

EL4094C
Video Gain Control/Fader

Applications Information — Contd.



EL4094 Macromodel Schematic

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4095C
Video Gain Control/Fader/Multiplexer

Features
- Full function video fader
- 0.02%/0.02° differential gain/phase @ 100% gain
- 25 ns multiplexer included
- Output amplifier included
- Calibrated linear gain control
- ±5V to ±15V operation
- 60 MHz bandwidth
- Low thermal errors

Applications
- Video faders/wipers
- Gain control
- Graphics overlay
- Video text insertion
- Level adjust
- Modulation

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4095CN	−40°C to +85°C	14 Pin P-DIP	MDP0031
EL4095CS	−40°C to +85°C	SO-14	MDP0027

General Description
The EL4095C is a versatile variable-gain building block. At its core is a fader which can variably blend two inputs together and an output amplifier that can drive heavy loads. Each input appears as the input of a current-feedback amplifier and with external resistors can separately provide any gain desired. The output is defined as:

$$V_{OUT} = A^*V_{INA}\,(0.5V + V_{GAIN}) + B^*V_{INB}\,(0.5V - V_{GAIN}),$$

where A and B are the fed-back gains of each channel.

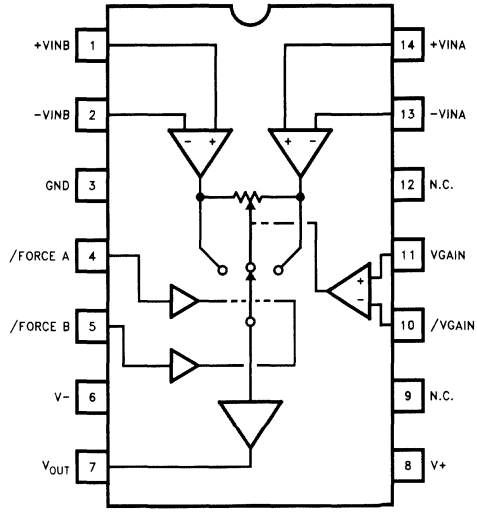
Additionally, two logic inputs are provided which each override the analog V_{GAIN} control and force 100% gain for one input and 0% for the other. The logic inputs switch in only 25 ns and provide high attenuation to the off channel, while generating very small glitches.

Signal bandwidth is 60 MHz, and gain-control bandwidth 20 MHz. The gain control recovers from overdrive in only 70 ns.

The EL4095C operates from ±5V to ±15V power supplies, and is available in both 14-pin DIP and narrow surface mount packages.

Connection Diagram

14-Pin DIP, SO



4095-1

Top View

Absolute Maximum Ratings (T_A = 25°C)

V_S+	Supply Voltage	+18V
V_S	Voltage between V_S^+ and V_S^-	+33V
$+V_{INA}$, $+V_{INB}$	Input Voltage	(V_S-) −0.3V to (V_S+) +0.3V
I_{IN}	Current Into $-V_{INA}$, $-V_{INB}$	5 mA
V_{GAIN}	Input Voltage	$V_{\overline{GAIN}}$ ±5V
$V_{\overline{GAIN}}$	Input Voltage	V_S- to V_S+

V_{FORCE}	Input Voltage	−1V to +6V
I_{OUT}	Output Current	±35 mA
T_A	Operating Temperature Range	−40°C to +85°C
T_J	Operating Junction Temperature	0°C to +150°C
T_{ST}	Storage Temperature Range	−65°C to +150°C
T_{LD}	Lead Solder Temperature (<10 seconds)	300°C
Internal Power Dissipation		See Curves

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±15V, T_A = 25°C, $V_{\overline{GAIN}}$ ground unless otherwise specified

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
V_{OS}	Input Offset Voltage		1.5	5	I	mV
I_{B+}	$+V_{IN}$ Input Bias Current		5	10	I	µA
I_{B-}	$-V_{IN}$ Input Bias Current		10	30	I	µA
CMRR	Common Mode Rejection	70	80		I	dB
−CMRR	$-V_{IN}$ Input Bias Current Common Mode Rejection		0.5	1.5	I	µA/V
PSRR	Power Supply Rejection Ratio	75	95		I	dB
−IPSR	$-V_{IN}$ Input Current Power Supply Rejection Ratio		0.2	2	I	µA/V
R_{OL}	Transimpedance	0.2	0.4		I	MΩ
R_{IN-}	$-V_{IN}$ Input Resistance		80		V	Ω
V_{IN}	$+V_{IN}$ Range	(V−) + 3.5		(V+) −3.5	I	V
V_O	Output Voltage Swing	(V−) +2		(V+) −2	I	V
I_{SC}	Output Short-Circuit Current	80	125	160	I	mA
V_{IH}	Input High Threshold at Force A or Force B Inputs			2.0	I	V
V_{IL}	Input Low Threshold at Force A or Force B Inputs	0.8			I	V
I_{FORCE}, High	Input Current of Force A or Force B, V_{FORCE} = 5V			−50	I	µA
I_{FORCE}, Low	Input Current of Force A or Force B, V_{FORCE} = 0V		−440	−650	I	µA

EL4095C
Video Gain Control/Fader/Multiplexer

Open Loop DC Electrical Characteristics — Contd.

$V_S = \pm 15V$, $T_A = 25°C$, unless otherwise specified

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
Feedthrough, Forced	Feedthrough of Deselected Input to Output, Deselected Input at 100% Gain Control	60	75		I	dB
V_{GAIN}, 100%	Minimum Voltage at V_{GAIN} for 100% Gain	0.465	0.5	0.535	I	V
V_{GAIN}, 0%	Maximum Voltage at V_{GAIN} for 0% Gain	−0.535	−0.5	−0.465	I	V
NL, Gain	Gain Control Non-linearity, $V_{IN} = \pm 0.5V$		2	4	I	%
R_{IN}, VG	Impedance between V_{GAIN} and $\overline{V_{GAIN}}$	4.5	5.5	6.5	I	kΩ
NL, $A_V = 1$	Signal Non-linearity, $V_{IN} = \pm 1V$, $V_{GAIN} = 0.55V$		<0.01		V	%
$A_V = 0.5$	Signal Non-linearity, $V_{IN} = \pm 1V$, $V_{GAIN} = 0V$		0.03		V	%
$A_V = 0.25$	Signal Non-linearity, $V_{IN} = \pm 1V$, $V_{GAIN} = -0.25V$		0.07	0.4	I	%
I_S	Supply Current		17	20	I	mA

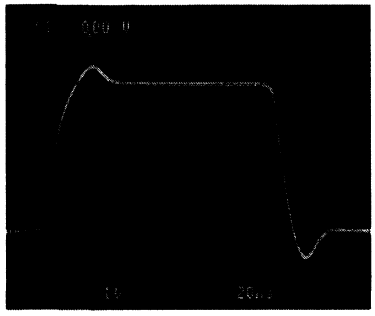
Closed Loop AC Electrical Characteristics

$V_S = \pm 15V$, $A_V = +1$, $R_F = R_{IN} = 1\ k\Omega$, $R_L = 500\Omega$, $C_L = 15\ pF$, $C_{IN} - = 2\ pF$, $T_A = 25°C$, $A_V = 100\%$ unless otherwise noted

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
SR	Slew Rate; V_{OUT} from −3V to +3V Measured at −2V and +2V		330		V	V/μs
BW	Bandwidth −3 dB		60			MHz
	−1 dB		30		V	MHz
	−0.1 dB		6			MHz
dG	Differential Gain; AC Amplitude of 286 mV_{p-p} at 3.58 MHz on DC Offset of −0.7V, 0V and +0.7V					
	$A_V = 100\%$		0.02		V	%
	$A_V = 50\%$		0.07			%
	$A_V = 25\%$		0.07			%
dθ	Differential Phase; AC Amplitude of 286 mV_{p-p} at 3.58 MHz on DC Offset of −0.7V, 0V and +0.7V					
	$A_V = 100\%$		0.02		V	°
	$A_V = 50\%$		0.05			°
	$A_V = 25\%$		0.15			°
T_S	Settling Time to 0.2%; V_{OUT} from −2V to +2V					
	$A_V = 100\%$		100		V	ns
	$A_V = 25\%$		100			ns
T_{FORCE}	Propagation Delay from V_{FORCE} = 1.4V to 50% Output Signal Enabled or Disabled Amplitude		25		V	ns
BW, Gain	−3 dB Gain Control Bandwidth, V_{GAIN} Amplitude 0.5 V_{P-P}		20		V	MHz
T_{REC}, Gain	Gain Control Recovery from Overload; V_{GAIN} from −0.7V to 0V		70		V	ns

Typical Performance Curves

Large-Signal Pulse Response Gain = +1



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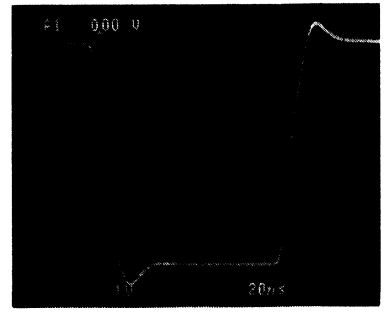
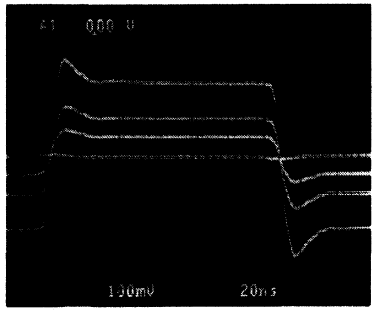
Large-Signal Pulse Response Gain = −1



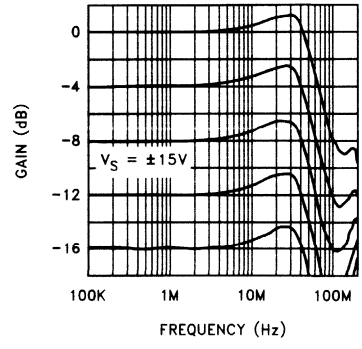
4095-7

Small-Signal Pulse Response for Various Gains



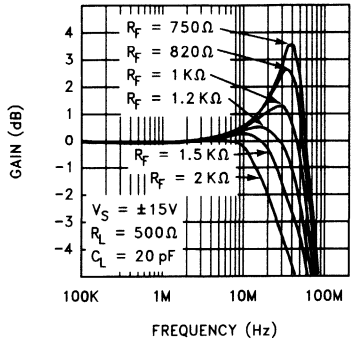
4095-8

Frequency Response for Different Gains-A_V = +1



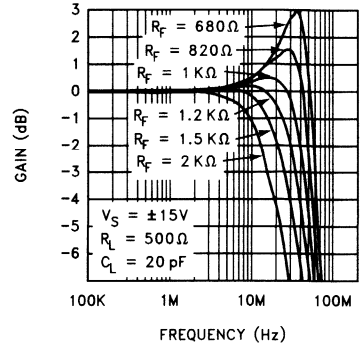
4095-9

Frequency Response with Different Values of R_F − Gain = +1



4095-10

Frequency Response with Different Values of R_F − Gain = −1



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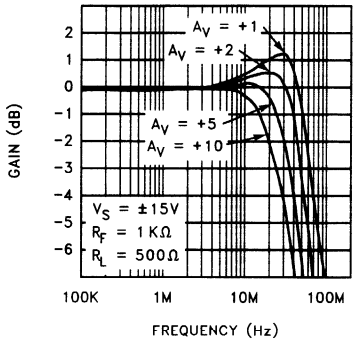
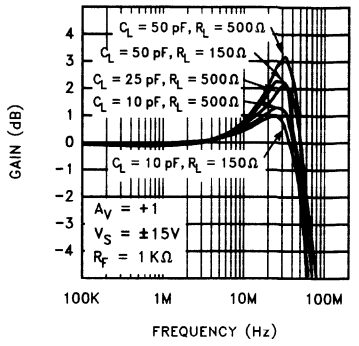
EL4095C
Video Gain Control/Fader/Multiplexer

Typical Performance Curves — Contd.

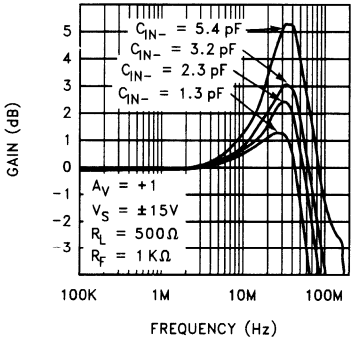
Frequency Response with Different Gains



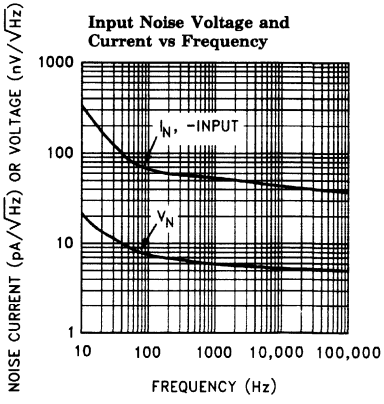
Frequency Response with Various Load Capacitances and Resistances



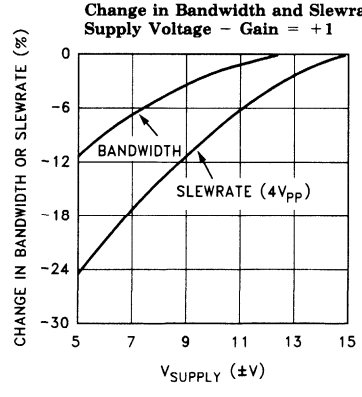
Frequency Response with Various Values of Parasitic C_{IN-}



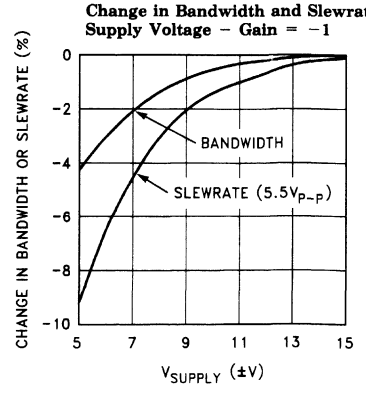
Input Noise Voltage and Current vs Frequency



Change in Bandwidth and Slewrate with Supply Voltage – Gain = +1



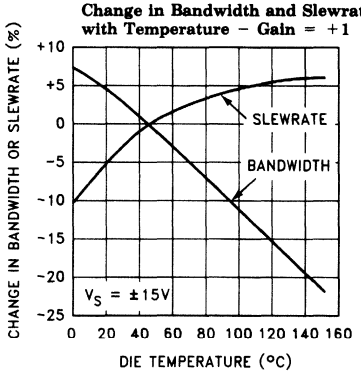
Change in Bandwidth and Slewrate with Supply Voltage – Gain = −1



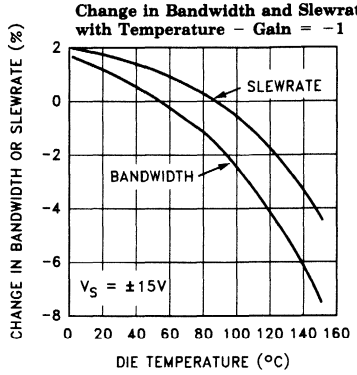
4095-12

Typical Performance Curves — Contd.

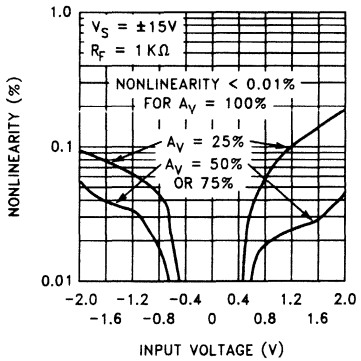
Change in Bandwidth and Slewrate with Temperature – Gain = +1



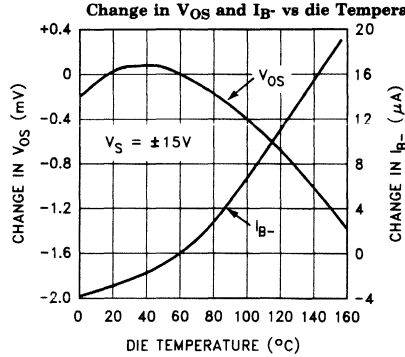
Change in Bandwidth and Slewrate with Temperature – Gain = –1



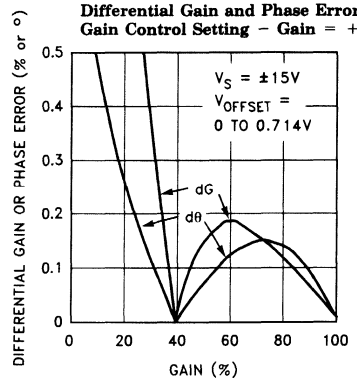
DC Nonlinearity vs Input Voltage – Gain = +1



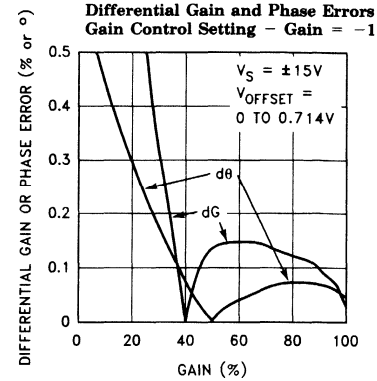
Change in V_{OS} and I_{B-} vs die Temperature



Differential Gain and Phase Errors vs Gain Control Setting – Gain = +1



Differential Gain and Phase Errors vs Gain Control Setting – Gain = –1



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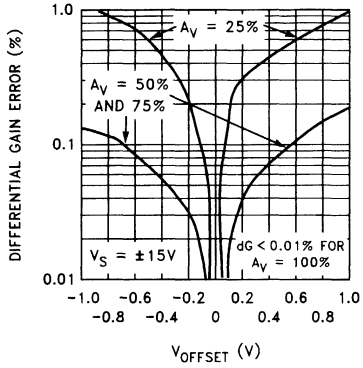
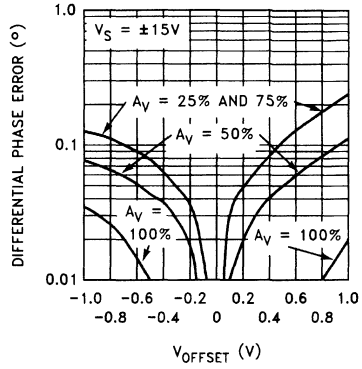
EL4095C
Video Gain Control/Fader/Multiplexer

Typical Performance Curves — Contd.

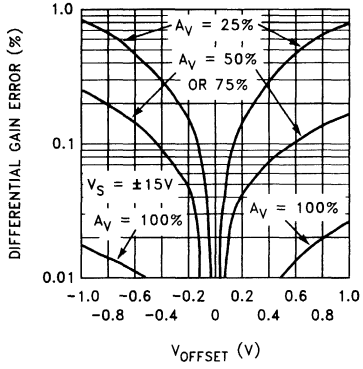
Differential Phase Error vs DC Offset – Gain = +1



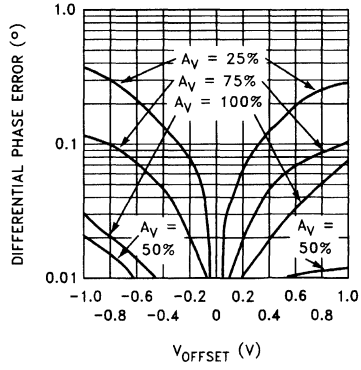
Differential Phase Error vs DC Offset – Gain = +1



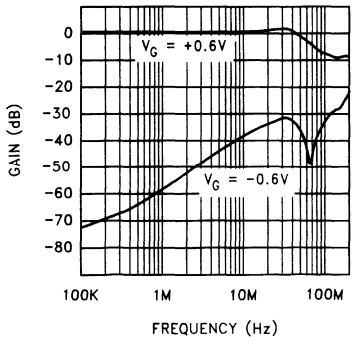
Differential Phase Error vs DC Offset – Gain = −1



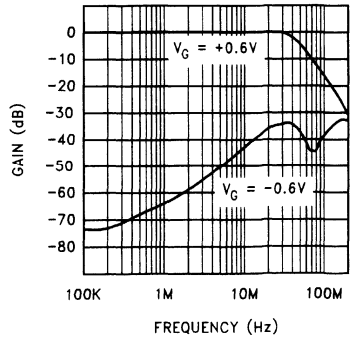
Differential Phase Error vs DC Offset – Gain = −1



Attenuation over Frequency – Gain = +1



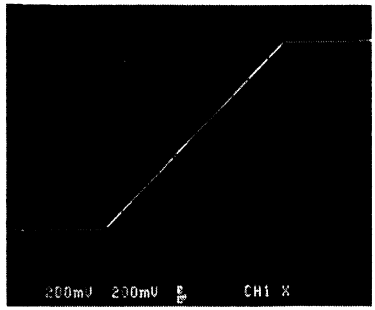
Attenuation over Frequency – Gain = −1



4095-14

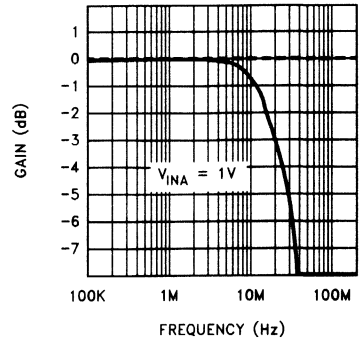
Typical Performance Curves — Contd.

Gain vs V_G (1 V_{DC} at V_{INA})



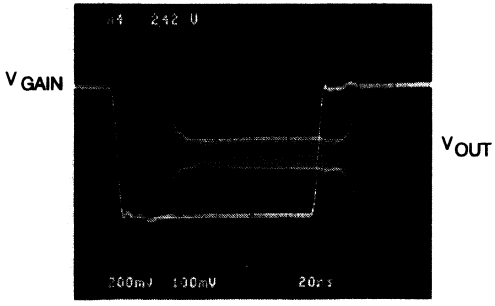
4095-15

Gain Control Gain vs Frequency



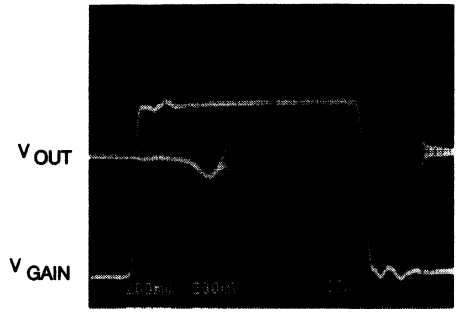
4095-16

Gain Control Response to a Non-Overloading Step, Constant Sinewave at V_{INA}



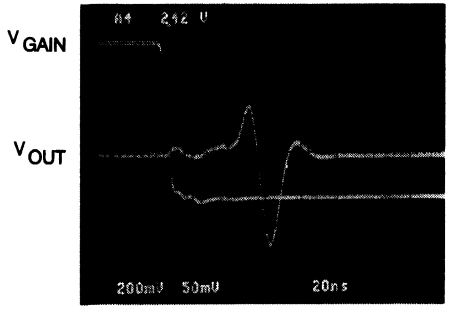
4095-17

V_{GAIN} Overload Recovery Delay



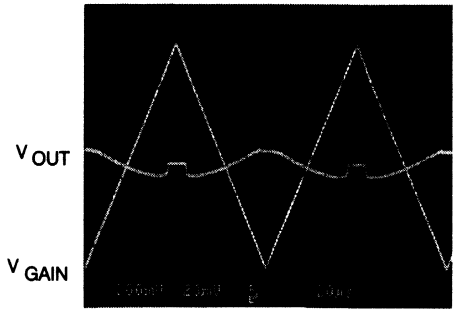
4095-18

V_{GAIN} Overload Recovery Response—No AC Input



4095-19

Cross-Fade Balance −0V on A_{IN} and B_{IN}; Gain = +1

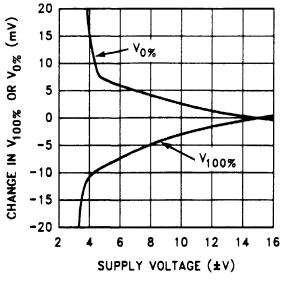


4095-20

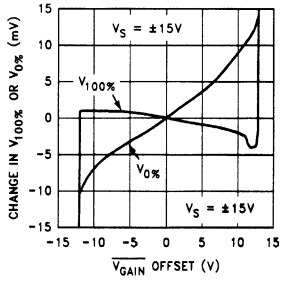
EL4095C
Video Gain Control/Fader/Multiplexer

Typical Performance Curves — Contd.

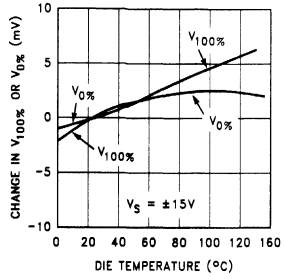
Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs Supply Voltage



Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs $\overline{V_{GAIN}}$ Offset

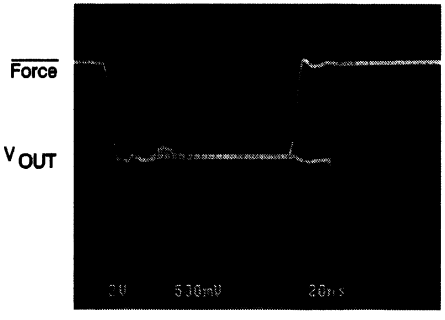


Change in $V_{100\%}$ and $V_{0\%}$ of Gain Control vs Die Temperature



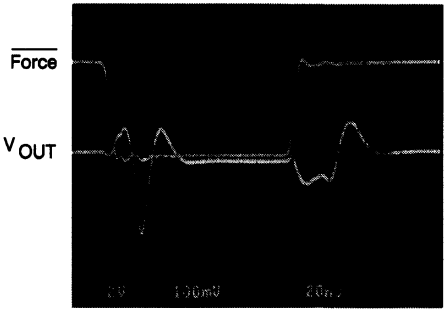
4095-21

$\overline{Force}$ Response



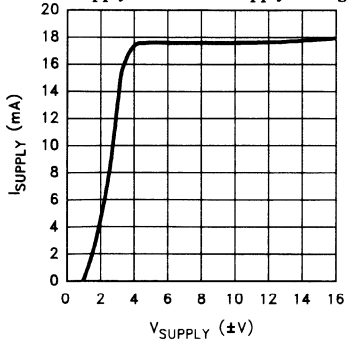
4095-22

$\overline{Force}$-Induced Output Transient



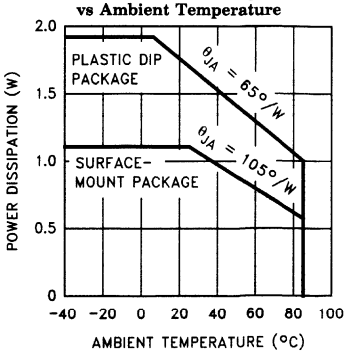
4095-23

Supply Current vs Supply Voltage



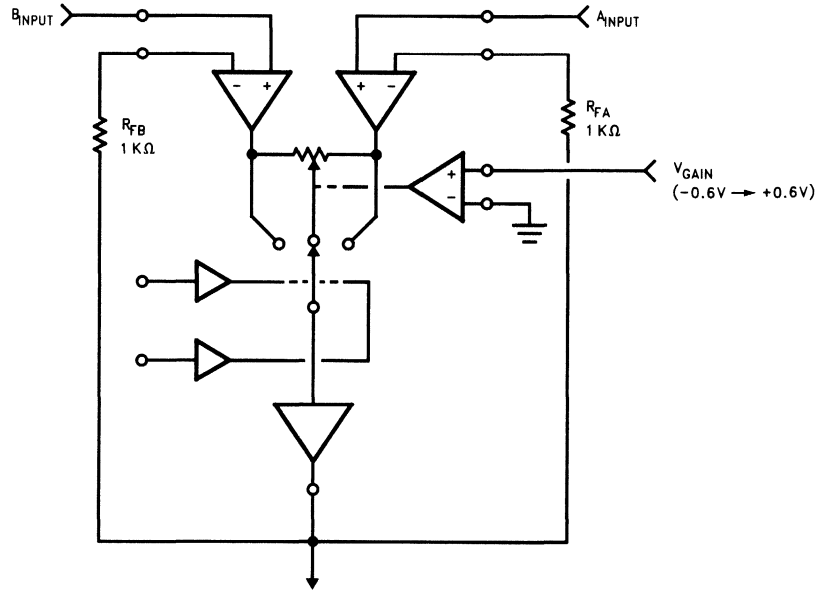
4095-24

Package Power Dissipation vs Ambient Temperature



4095-25

Test Circuit, $A_V = +1$



4095-26

EL4095C
Video Gain Control/Fader/Multiplexer

Applications Information

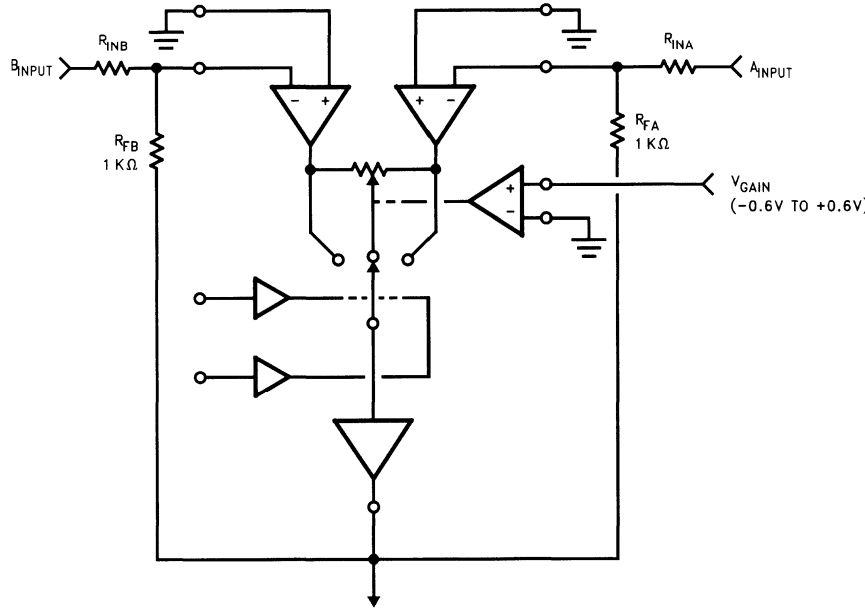
The EL4095 is a general-purpose two-channel fader whose input channels each act as a current-feedback amplifier (CFA) input. Each input can have its own gain factor as established by external resistors. For instance, the Test Circuit shows two channels each arranged as +1 gain, with the traditional single feedback resistor R_F connected from V_{OUT} to the $-V_{IN}$ of each channel.

The EL4095 can be connected as an inverting amplifier in the same manner as any CFA:

Frequency Response

Like other CFA's, there is a recommended feedback resistor, which for this circuit is 1 KΩ. The value of RF sets the closed-loop −3 dB bandwidth, and has only a small range of practical variation. The user should consult the typical performance curves to find the optional value of R_F for a given circuit gain. In general, the bandwidth will decrease slightly as closed-loop gain is increased; R_F can be reduced to make up for bandwidth loss. Too small a value of R_F will cause frequency response peaking and ringing during transients. On the other hand, increasing R_F will reduce bandwidth but improve stability.

EL4095C In Inverting Connection



$$\text{OUTPUT} = -A_{IN}\left(\frac{R_{FA}}{R_{INA}}\right)(0.5 + V_{GAIN}) - B_{IN}\left(\frac{R_{FB}}{R_{INB}}\right)(0.5 - V_{GAIN})$$

FOR $-0.5V \le V_{GAIN} \le +0.5V$

4095-27

Applications Information — Contd.

Stray capacitance at each $-V_{IN}$ terminal should absolutely be minimized, especially in a positive-gain mode, or peaking will occur. Similarly, the load capacitance should be minimized. If more than 25 pF of load capacitance must be driven, a load resistor from 100Ω to 400Ω can be added in parallel with the output to reduce peaking, but some bandwidth degradation may occur. A "snubber" load can alternatively be used. This is a resistor in series with a capacitor to ground, 150Ω and 100 pF being typical values. The advantage of a snubber is that it does not draw DC load current. A small series resistor, low tens of ohms, can also be used to isolate reactive loads.

Distortion

The signal voltage range of the $+V_{IN}$ terminals is within 3.5V of either supply rail.

One must also consider the range of error currents that will be handled by the $-V_{IN}$ terminals. Since the $-V_{IN}$ of a CFA is the output of a buffer which replicates the voltage at $+V_{IN}$, error currents will flow into the $-V_{IN}$ terminal. When an input channel has 100% gain assigned to it, only a small error current flows into its negative input; when low gain is assigned to the channel the output does not respond to the channel's signal and large error currents flow.

Here are a few idealized examples, based on a gain of +1 for channels A and B and $R_F = 1\ k\Omega$ for different gain settings:

Gain	V_{INA}	V_{INB}	$I(-V_{INA})$	$I(-V_{INB})$	V_{OUT}
100%	1V	0	0	1 mA	1V
75%	1V	0	−250 μA	750 μA	0.75V
50%	1V	0	−500 μA	500 μA	0.5V
25%	1V	0	−750 μA	250 μA	0.25V
0%	1V	0	−1 mA	0	0V

Thus, either $-V_{IN}$ can receive up to 1 mA error current for 1V of input signal and 1 kΩ feedback resistors. The maximum error current is 3 mA for the EL4095, but 2 mA is more realistic. The major contributor of distortion is the magnitude of error currents, even more important than loading effects. The performance curves show distortion versus input amplitude for different gains.

If maximum bandwidth is not required, distortion can be reduced greatly (and signal voltage range enlarged) by increasing the value of R_F and any associated gain-setting resistor.

100% Accuracies

When a channel gain is set to 100%, static and gain errors are similar to those of a simple CFA. The DC output error is expressed by

$$V_{OUT}, \text{Offset} = V_{OS}{}^* A_V + (I_B-)^*R_F.$$

The input offset voltage scales with fed-back gain, but the bias current into the negative input, I_B-, adds an error not dependent on gain. Generally, I_B- dominates up to gains of about seven.

The fractional gain error is given by

$$E_{GAIN} = (R_F + A_V{}^*R_{IN} -) R_F + A_V R_{IN})/R_{OL}$$

The gain error is about 0.3% for a gain of one, and increases only slowly for increasing gain. $R_{IN}-$ is the input impedance of the input stage buffer, and R_{OL} is the transimpedance of the amplifier, 80 kΩ and 350 kΩ respectively.

Gain Control Inputs

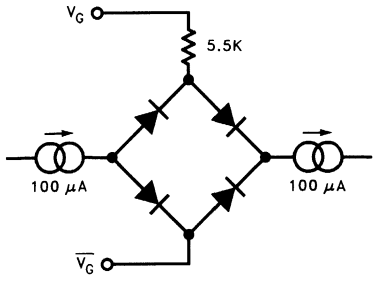
The gain control inputs are differential and may be biased at any voltage as long as $\overline{V_{GAIN}}$ is less than 2.5V below V+ and 3V above V−. The differential input impedance is 5.5 kΩ, and a common-mode impedance is more than 500 kΩ. With zero differential voltage on the gain inputs, both signal inputs have a 50% gain factor. Nominal calibration sets the 100% gain of V_{INA} input at +0.5V of gain control voltage, and 0% at −0.5V of gain control. V_{INB}'s gain is complementary to that of V_{INA}; +0.5V of gain control sets 0% gain at V_{INB} and −0.5V gain control sets 100% V_{INB} gain. The gain control does not have a completely abrupt transition at the 0% and 100% points. There is about 10 mV of "soft" transfer at the gain endpoints. To obtain the most accurate 100% gain factor or best attenuation of 0% gain, it is necessary to overdrive the gain control input by about 30 mV. This would set the gain control voltage range as −0.565 mV to +0.565V, or 30 mV beyond the maximum guaranteed 0% to 100% range.

EL4095C
Video Gain Control/Fader/Multiplexer

Applications Information — Contd.

In fact, the gain control internal circuitry is very complex. Here is a representation of the terminals:

Representation of Gain Control Inputs V_G and $\overline{V_G}$



4095-28

For gain control inputs between ±0.5V (±90 μA), the diode bridge is a low impedance and all of the current into V_G flows back out through $\overline{V_G}$. When gain control inputs exceed this amount, the bridge becomes a high impedance as some of the diodes shut off, and the V_G impedance rises sharply from the nominal 5.5 KΩ to over 500 KΩ. This is the condition of gain control overdrive. The actual circuit produces a much sharper overdrive characteristics than does the simple diode bridge of this representation.

The gain input has a 20 MHz −3 dB bandwidth and 17 ns risetime for inputs to ±0.45V. When the gain control voltage exceeds the 0% or 100% values, a 70 ns overdrive recovery transient will occur when it is brought back to linear range. If quicker gain overdrive response is required, the Force control inputs of the EL4095 can be used.

Force Inputs

The Force inputs completely override the V_{GAIN} setting and establish maximum attainable 0% and 100% gains for the two input channels. They are activated by a TTL logic low on either of the $\overline{FORCE}$ pins, and perform the analog switching very quickly and cleanly. $\overline{FORCEA}$ causes 100% gain on the A channel and 0% on the B channel. $\overline{FORCEB}$ does the reverse, but there is no defined output state when $\overline{FORCEA}$ and $\overline{FORCEB}$ are simultaneously asserted.

The Force inputs do not incur recovery time penalties, and make ideal multiplexing controls. A typical use would be text overlay, where the A channel is a video input and the B channel is digitally created text data. The $\overline{FORCEA}$ input is set low normally to pass the video signal, but released to display overlay data. The gain control can be used to set the intensity of the digital overlay.

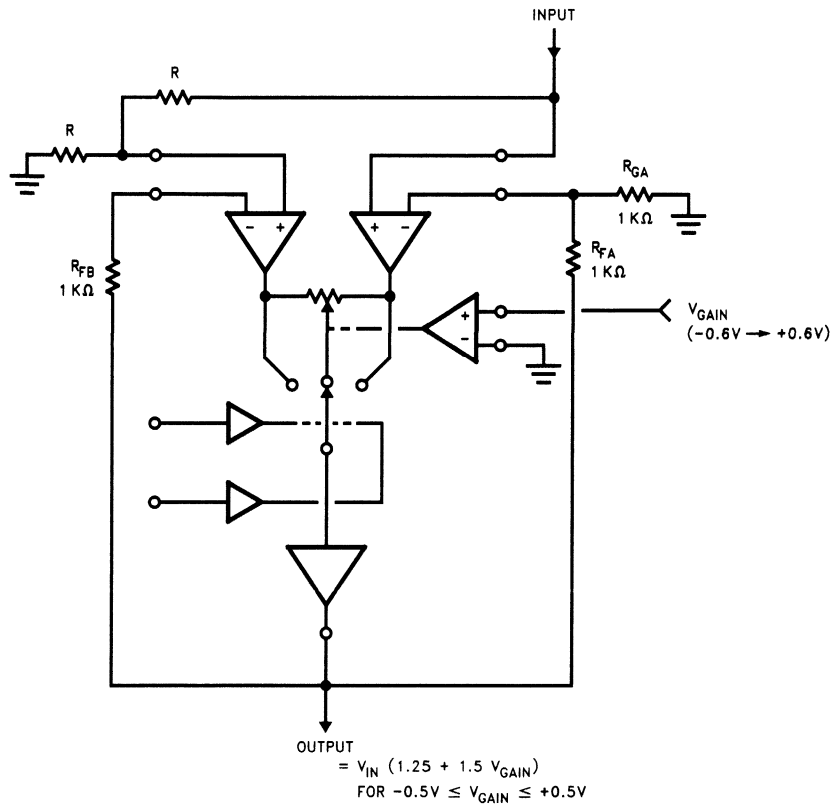
Other Applications Circuits

The EL4095 can also be used as a variable-gain single input amplifier. If a 0% lower gain extreme is required, one channel's input should simply be grounded. Feedback resistors must be connected to both $-V_{IN}$ terminals; the EL4095 will not give the expected gain range when a channel is left unconnected.

This circuit gives +0.5 to +2.0 gain range, and is useful as a signal leveller, where a constant output level is regulated from a range of input amplitudes:

Application Information — Contd.

Leveling Circuit with $0.5 \leq A_V \leq 2$



Here the A input channel is configured for a gain of +2 and the B channel for a gain of +1 with its input attenuated by ½. The connection is virtuous because the distortions do not increase monotonically with reducing gain as would the simple single-input connecton.

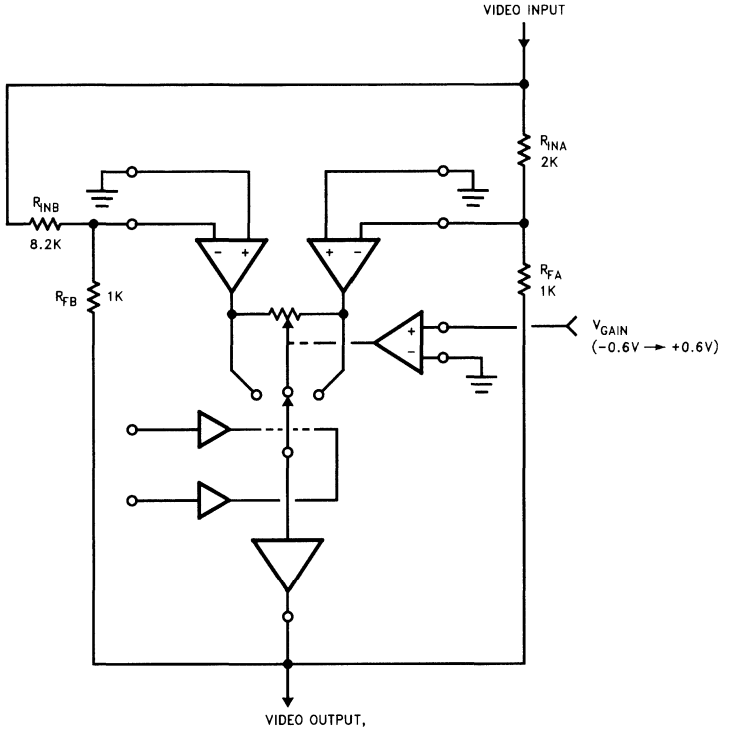
For video levels, however, these constants can give fairly high differential gain error. The problem occurs for large inputs. Assume that a "twice-size" video input occurs. The A-side stage sees the full amplitude, but the gain would be set to 100% B-input gain to yield an overall gain of

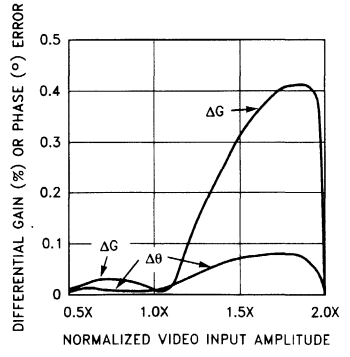
EL4095C
Video Gain Control/Fader/Multiplexer

Application Information — Contd.

½ to produce a standard video output. The $-V_{IN}$ of the A side is a buffer output that reproduces the input signal, and drives R_{GA} and R_{FA}. Into the two resistors 2.1 mA of error current flows for a typical 1.4V of input DC offset, creating distortion in a A-side input stage. R_{GA} and R_{FA} could be increased together in value to reduce the error current and distortions, but increasing R_{FA} would lower bandwidth. A solution would be to simply attenuate the input signal magnitude and restore the EL4095 output level to standard level with another amplifier so:

Reduced-Gain Leveler for Video Inputs and Differential Gain and Phase Performance (see text)





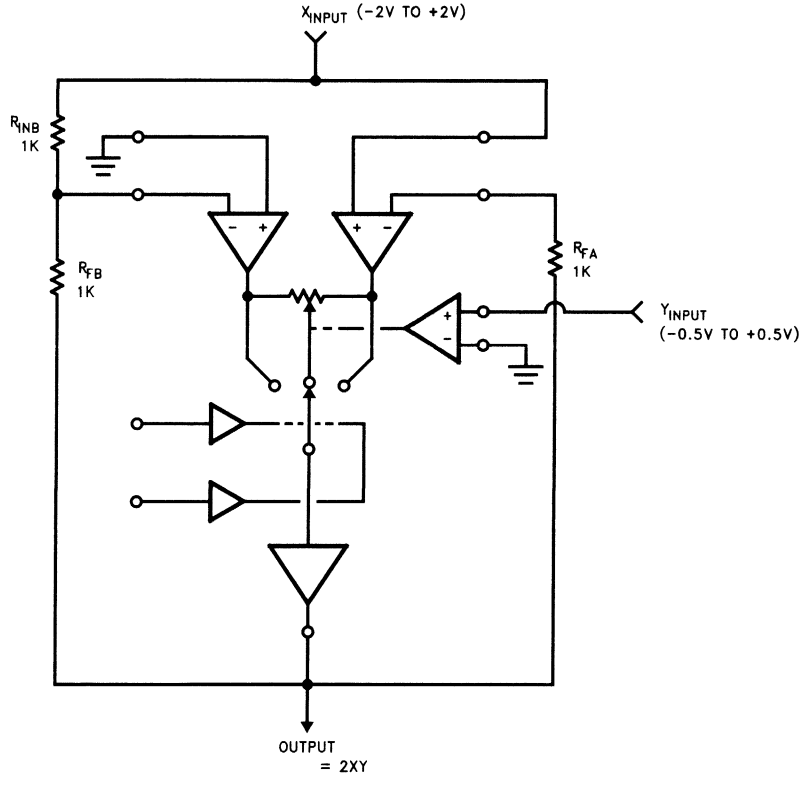
Application Information — Contd.

Although another amplifier is needed to gain the output back to standard level, the reduced error currents bring the differential phase error to less than 0.1′ over the entire input range.

A useful technique to reduce video distortion is to DC-restore the video level going into the EL4095, and offsetting black level to −0.35V so that the entire video span encompasses ±0.35V rather than the unrestored possible span of ±0.7V (for standard-sized signals). For the preceding leveler circuit, the black level should be set more toward −0.7V to accommodate the largest input, or made to vary with the gain control itself (large gain, small offset; small gain, larger offset).

The EL4095 can even be wired as a four quadrant multiplier:

EL4095 Connected as a Four-Quadrant Multiplier



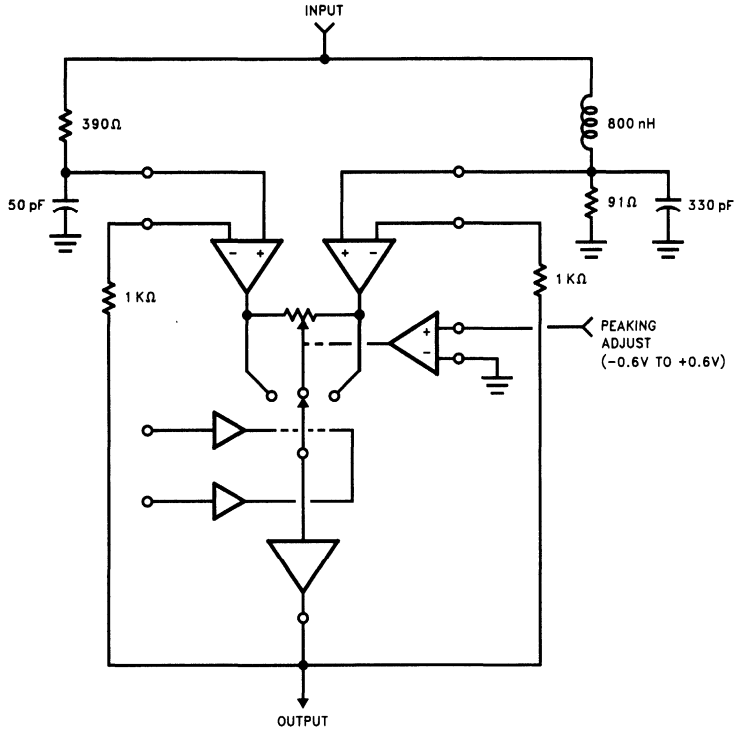
4095-32

Application Information — Contd.

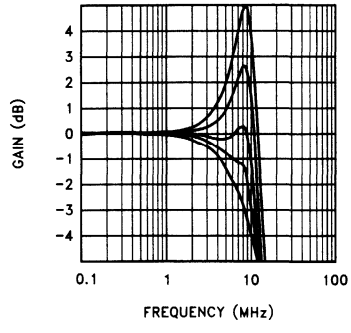
The A channel gains the input by +1 and the B channel by −1. Feedthrough suppression of the Y input can be optimized by introducing an offset between channel A and B. This is easily done by injecting an adjustable current into the summing junction ($-V_{IN}$ terminal) of the B input channel.

The two input channels can be connected to a common input through two dissimilar filters to create a DC-controlled variable filter. This circuit provides a controlled range of peaking through rolloff characteristics:

Variable Peaking Filter



4095-33



4095-34

Applications Information — Contd.

The EL4095 is connected as a unity-gain fader, with an LRC peaking network connected to the A-input and an RC rolloff network connected to the B-input. The plot shows the range of parking controlled by the V_{GAIN} input. This circuit would be useful for flattening the frequency response of a system, or for providing equalization ahead of a lossy transmission line.

Noise

The electrical noise of the EL4095 has two components: the voltage noise in series with $+V_{IN}$ is 5 nV $\sqrt{Hz}$ wideband, and there is a current noise injected into $-V_{IN}$ of 35 pA$\sqrt{Hz}$. The output noise will be

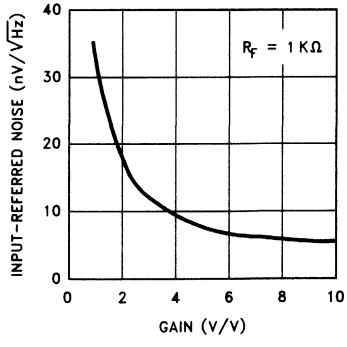
$$\overline{V_{n,\,out}} = \sqrt{(A_V \bullet \overline{V_{n,\,input}})^2 + (\overline{I_{n,\,input}} \bullet R_F)^2},$$

and the input-referred noise is

$$\overline{V_{n,\,input\text{-}referred}} = \sqrt{(\overline{V_{n,\,input}})^2 + (\overline{I_{n,\,input}} \bullet R_F/A_V)^2}$$

where A_V is the fed-back gain of the EL4095. Here is a plot of input-referred noise vs A_V:

Input-Referred Noise vs Closed-Loop Gain



4095-35

Thus, for a gain of three or more the fader has a noise as good as an op-amp. The only trade-off is that the dynamic range of the input is reduced by the gain due to the nonlinearity caused by gained-up output signals.

Power Dissipation

Peak die temperature must not exceed 150°C. This allows 75°C internal temperature rise for a 75°C ambient. The EL4095 in the 14-pin PDIP package has a thermal resistance of 65°C/W, and can thus dissipate 1.15W at a 75°C ambient temperature. The device draws 20 mA maximum supply current, only 600 mW at ±15V supplies, and the circuit has no dissipation problems in this package.

The SO-14 surface-mount package has a 105°C/W thermal resistance with the EL4095, and only 714 mW can be dissipated at 75°C ambient temperature. The EL4095 thus can be operated with ±15V supplies at 75°C, but additional dissipation caused by heavy loads must be considered. If this is a problem, the supplies should be reduced to ±5V to ±12V levels.

The output will survive momentary short-circuits to ground, but the large available current will overheat the die and also potentially destroy the circuit's metal traces. The EL4095 is reliable within its maximum average output currents and operating temperatures.

The EL4095 Macromodel

This macromodel is offered to allow simulation of general EL4095 behavior. We have included these characteristics:

- Small-signal frequency response
- Output loading effects
- Input impedance
- Off-channel feedthrough
- Output impedance over frequency
- $-V_{IN}$ characteristics and sensitivity to parasitic capacitance
- Signal path DC distoritons
- V_{GAIN} I-V characteristics
- V_{GAIN} overdrive recovery delay
- 100% gain error
- $\overline{FORCE}$ operation

These will give a good range of results of various operating conditions, but the macromodel does not behave identically as the circuit in these areas:

- Temperature effects
- Signal overload effects
- Signal and $\overline{V_G}$ operating range
- Current-limit
- Video and high-frequency distortions
- Glitch and delay from $\overline{FORCE}$ inputs
- Manufacturing tolerances
- Supply voltage effects
- Slewrate limitations
- Noise
- Power supply interactions

Applications Information — Contd.

```
*** EL4095 macromodel ***
******
******
*                        +VinB
*                          |   -VinB
*                          |    |   /ForceA
*                          |    |    |    /ForceB
*                          |    |    |    |     Vout
*                          |    |    |    |     |   /Vgain
*                          |    |    |    |     |    |    Vgain
*                          |    |    |    |     |    |    |    -VinA
*                          |    |    |    |     |    |    |    |   +VinA
*                          |    |    |    |     |    |    |    |   |
.SUBCKT 4095macromodel ( 1    2    4    5    7    10   11   13   14 )
***
Rol 810 0 290k
Ccomp 810 0 4.3p
G1 110 0 810 0 -10
Rout 110 0 0.1
Lout 110 7 350n
RLout 110 7 80
***
Rina+ 14 0 5E6
Rinb+ 1 0 5E6
Rvg 11 0 2E6
Rvgg 10 0 2E6
Rforcea 4 0 1E9
Rforceb 5 0 1E9
******
*** Input channel A
***
Rina 22 313 79
Ra 111 0 1k
Rfeedthrougha 13 313 1.0
Cfeedthrougha 23 13 2500p
Ccompa 111 0 2p
E1a 23 313 302 25 -1
E2a 22 0 14 0 0.9999
Rspice3 23 313 1E12
G1a 111 0 POLY(1) (22,313) 0.0 0.0125 -150E-6
G2a 810 0 POLY(2) (111,0) (113,0) 0.0 0.0 0.0 0.0 0.001
***
***Input channel B
***
Rinb 25 302 79
Rb 120 0 1k
Rfeedthroughb 2 302 1.0
Cfeedthroughb 24 2 2500p
Ccompb 120 0 2p
E1b 24 302 22 313 -1
E2b 25 0 1 0 0.9999
Rspice4 24 302 1E12
G1b 120 0 POLY(1) (25,302) 0.0 0.0125 -150E-6
G2b 810 0 POLY(2) (120,0) (119,0) 0.0 0.0 0.0 0.0 0.001
***
***Gain control
***
Rspice1 113 0 1E12
Rspice2 119 0 1E12
R10 114 0 1E7
R11 204 206 2.5E6
R12 205 206 2.5E6
C10 201 0 9.5E-16
D1 114 115 Dclamp
D2 116 114 Dclamp
D3 204 4 Dclamp
```

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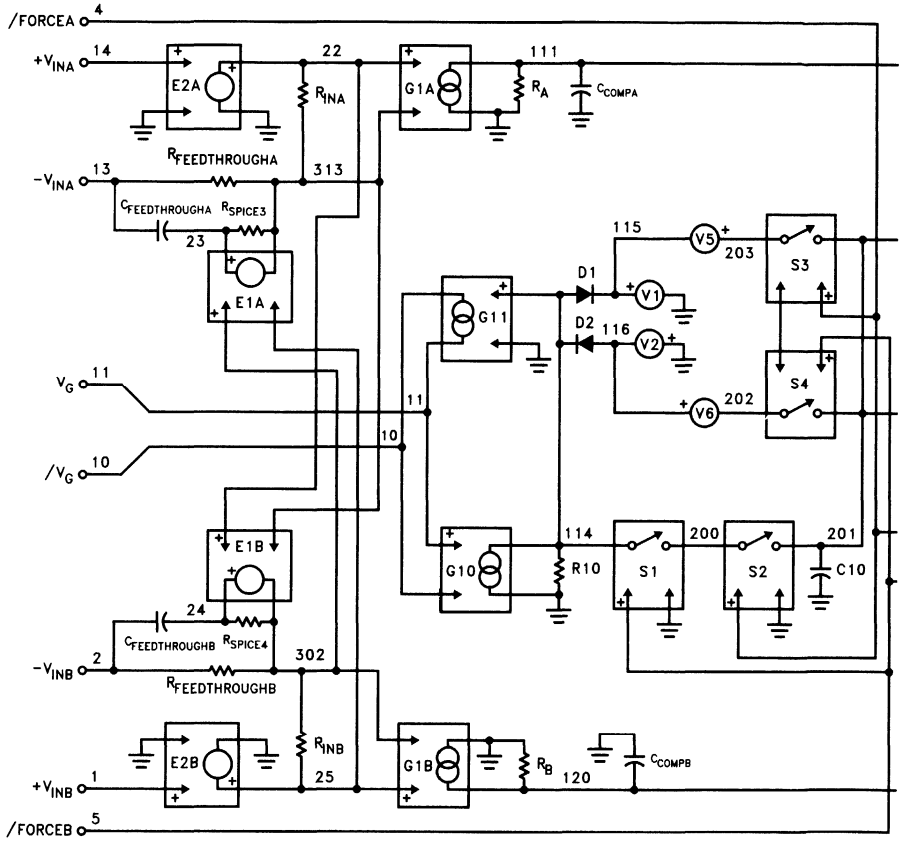
Applications Information — Contd.

```
D4 205 5 Dclamp
.model Dclamp D(TT=200n)
Vtt1 206 0 2.4
V1 115 0 4999.3
V2 0 116 4999.3
V3 113 117 0.5
V4 119 118 0.5
V5 203 115 0.7
V6 116 202 0.7
G10 114 0 11 10 -0.001
G11 11 10 114 0 -2E-8
E10 117 0 201 0 1E-4
E11 118 0 201 0 -1E-4
S1 114 200 5 0 Nopen
S2 200 201 4 0 Nopen
S3 203 201 4 0 Nclosed
S4 202 201 5 0 Nclosed
.model Nopen VSWITCH(Ron=100 Roff=1E12 Von=1.6 Voff=1.2)
.model Nclosed VSWITCH( Ron=100 Roff=1E12 Von=1.2 Voff=1.6)
***
.ENDS
******
```

4095-37

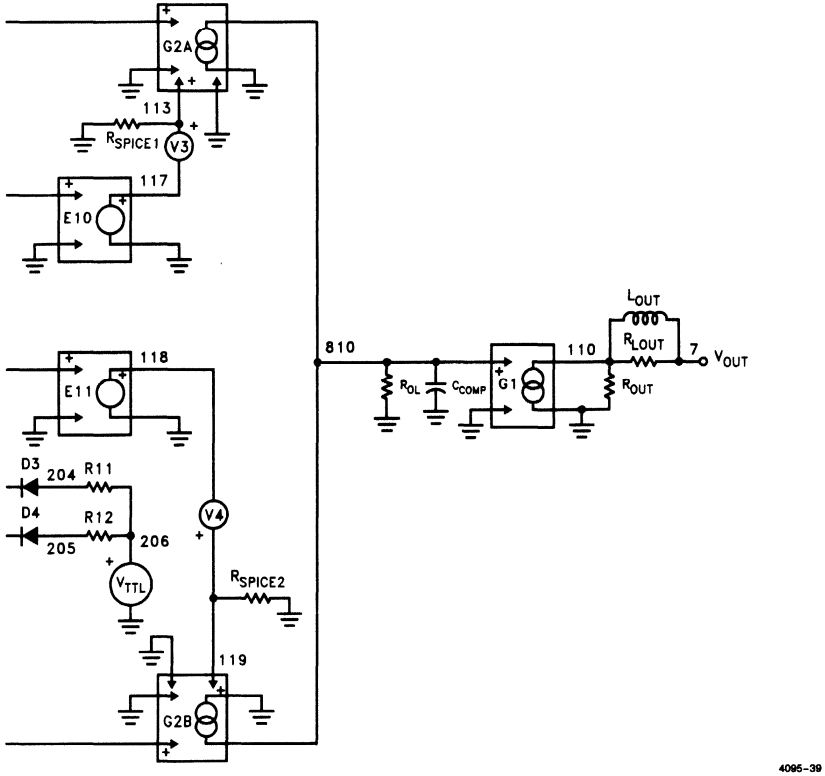
Applications Information — Contd.

The EL4095 Macromodel Schematic



4095-38

Applications Information — Contd.



4095-39

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4390C

Triple 60 MHz Video Amplifier w/DC Restore

Features

- 60 MHz −3 dB bandwidth for gains of 1 to 10
- 600 V/μs slew rate
- 10 MHz bandwidth flat to 0.1 dB
- Excellent differential gain and phase
- TTL/CMOS compatible DC restore function
- Available in SOL-16

Applications

- RGB drivers requiring DC restoration
- RGB multiplexers requiring DC restoration
- RGB gain blocks
- Video gain blocks requiring AC restoration
- Sync and color burst processing

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4390CN	40°C to +85°C	16-Lead P-DIP	MDP0031
EL4390CM	40°C to +85°C	16-Lead SOL	MDP0027

General Description

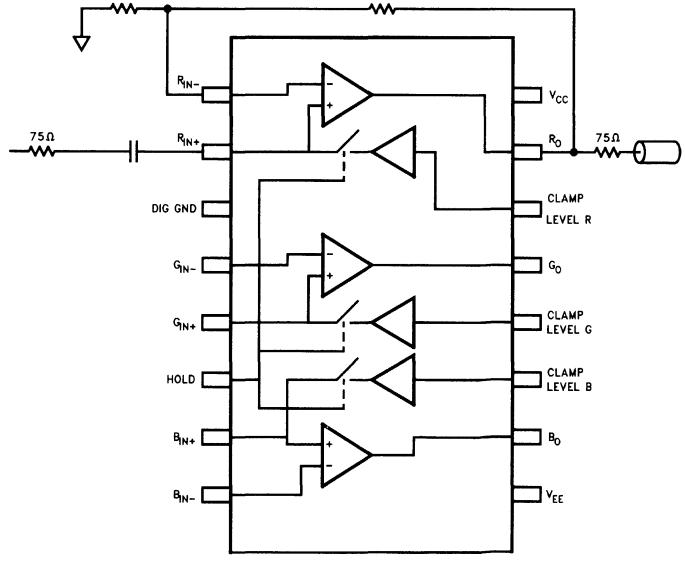
The EL4390C is three wideband current-feedback amplifiers optimized for video performance, each with a DC restore amplifier. The DC restore function is activated by a common TTL/CMOS compatible control signal, while each channel has a separate restore reference.

Each amplifier can drive a load of 150Ω at video signal levels. The EL4390C operates on supplies as low as ±4V up to ±15V.

Being a current-feedback design, the bandwidth stays relatively constant at approximately 60 MHz over the ±1 to ±10 gain range. The EL4390C has been optimized for use with 1500Ω feedback resistors.

Elantec products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1: *Elantec's Processing, Integrated Circuits.*

Connection Diagram



Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S^+ and V_S^-	+33V	Internal Power Dissipation	See Curves
Voltage at V_S^+	+18V	Operating Ambient Temp Range	−40°C to +85°C
Voltage at V_S^-	−18V	Operating Junction Temperature	150°C
Voltage between V_{IN}^+ and V_{IN}^-	±6V	Storage Temperature Range	−65°C to +150°C
Current into V_{IN}^+ or V_{IN}^-	5 mA	Lead Temperature (Soldering <10 seconds)	300°C

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterisation Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 150Ω

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Amplifier Section (not restored)							
V_{OS}	Input Offset Voltage	+25°C		2	15	II	mV
I_B^+	I_{IN}^+ Input Bias Current	+25°C		0.2	5	II	µA
I_B^-	I_{IN}^- Input Bias Current	+25°C		10	65	II	µA
R_{OL}	Transimpedance (Note 1)	+25°C	100	220		II	kΩ
R_{IN}^-	I_N^- Resistance	+25°C		50		V	Ω
CMRR	Common-Mode Rejection Ratio (Note 2)	+25°C	50	56		II	dB
V_O	Output Voltage Swing; R_L = 1 kΩ	+25°C	±12	±13		II	V
I_{SC}	Short-Circuit Current	+25°C	45	70		II	mA
I_{SY}	Supply Current (Quiescent)	+25°C		20	27	II	mA
Restoring Section							
$V_{OS, COMP}$	Composite Input Offset Voltage (Note 3)	+25°C		8	35	II	mV
I_B^+,R	Restore I_N^+ Input Bias Current	+25°C		0.2	5	II	µA
I_{OUT}	Restoring Current Available	+25°C	2	4		II	mA

EL4390C
Triple 60 MHz Video Amplifier w/DC Restore

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 150Ω — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Restoring Section — Contd.							
CMRR	Common-Mode Rejection Ratio (Note 2)	+25°C	45	52		II	dB
PSRR	Power Supply Rejection Ratio (Note 4)	+25°C		50		II	dB
R_{OL}	Transimpedance	+25°C		120		II	kΩ
$I_{SY, RES}$	Supply Current, Restoring (one channel only restoring)	+25°C		23	30	II	mA
$V_{IL, RES}$	RES Logic Low Threshold	+25°C		1.0	1.4	II	V
$V_{IH, RES}$	RES Logic High Threshold	+25°C	1.4	1.8		II	V
$I_{IL, RES}$	RES Input Current, Logic Low	+25°C		2	10	II	μA
$I_{IH, RES}$	RES Input Current, Logic High	+25°C		0.5	3	II	μA

Note 1: For current feedback amplifiers, $A_{VOL} = R_{OL}/R_{IN}^-$.
Note 2: $V_{CM} = \pm 10V$ for $V_S = \pm 15V$.
Note 3: Measured from V_{CL} to amplifier output, while restoring.
Note 4: V_{OS} is measured at $V_S = \pm 4.5V$ and $V_S = \pm 16V$, both supplies are changed simultaneously.

Closed Loop AC Electrical Characteristics Supplies at ±15V, Load = 150Ω and 15 pF. R_F and R_G = 1500Ω; A_V = 2, T_A = 25°C (See note 7 re: test fixture)

Parameter	Description	Min	Typ	Max	Test Level	Units
Amplifier Section						
SR	Slew Rate (Note 5)	320	400		V	V/μs
SR	Slew Rate w/ ±5V Supplies (Note 5)	220	300		II	V/μs
BW	Bandwidth, −3 dB	60	70		III	MHz
	±5V Supplies, −3 dB	55	60		III	MHz
BW	Bandwidth, −0.1 dB	12	18		III	MHz
	±5V Supplies, −0.1 dB	12	21		III	MHz
dG	Differential Gain at 3.58 MHz		0.06		V	%
	at ±5V Supplies (Note 6)		0.30		V	%
dθ	Differential Phase at 3.58 MHz		0.10		V	(°)
	at ±5V Supplies (Note 6)		0.13		V	(°)
Restoring Section						
BW	Restore Loop Bandwidth, −3 dB	1	4		III	MHz
T_{RE}	Time to Enable Restore		25	35	III	ns
T_{RD}	Time to Disable Restore		15	25	III	ns

Note 5: SR is measured at 20% to 80% of 4V pk-pk square wave.
Note 6: DC offset from −0.714V to +0.714V, AC amplitude is 286m Vp-p, equivalent to 40 ire.
Note 7: Test fixture was designed to minimize capacitance at the I_N^- input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

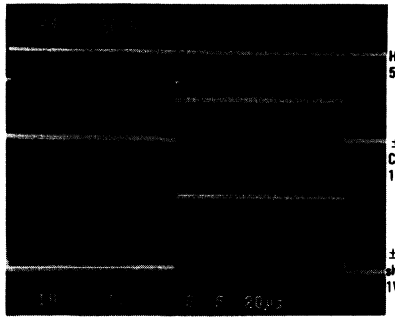
Typical Application for EL4390

The figure shows one channel of the EL4390 configured as a non-inverting DC-restoring amplifier, with a gain of 2, driving a 75Ω, back terminated cable.

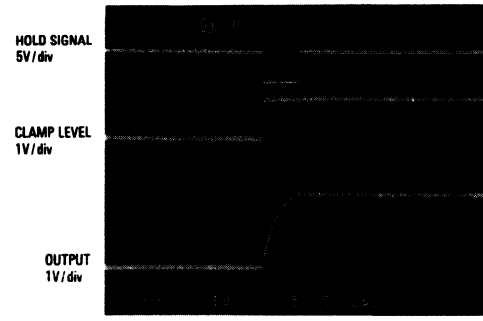
In this example, the clamp level voltage is a square wave, of 1V pk-pk amplitude. When "HOLD" is driven low with a TTL compatible signal, the internal transconductance amplifier supplies current to the V_{IN}^+ side of the input/hold capacitor, to restore any residual DC level that has accumulated on C_{IN}, due to, for example, a non symmetrical video waveform.

When "HOLD" returns to a TTL high, the internal transconductance amplifier goes into a high output impedance mode, and the DC level on the V_{IN}^+ pin is held steady.

The schematic does not show things like power supply decoupling, or pcb layout, grounding and signal returns, but these will all affect the overall performance of the circuit, and care should be taken with these aspects.

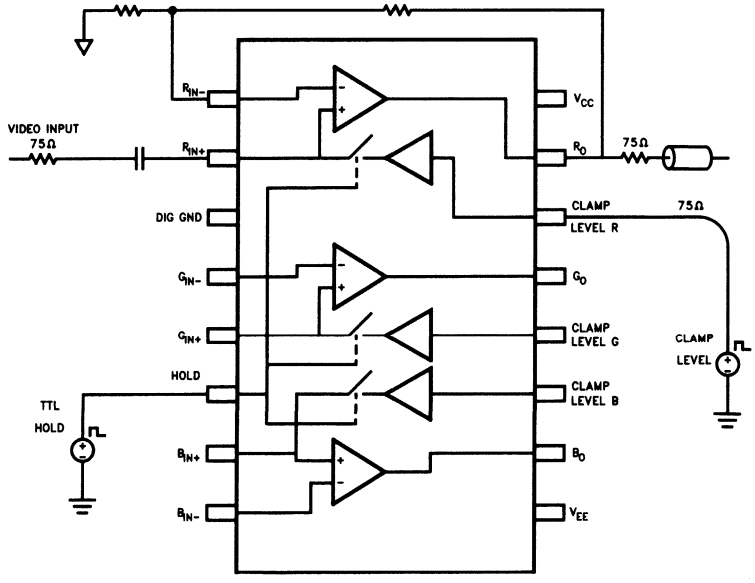


4390-2



4390-3

Typical configuration for a DC-restoring Video Amplifier. Only one channel shown connected for clarity.



4390-4

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4393C

Triple 80 MHz Video Amplifier w/Disable

Features

- 80 MHz −3 dB bandwidth for gains of 1 to 10
- 900 V/μs slew rate
- 10 MHz bandwidth flat to 0.1 dB
- Excellent differential gain and phase
- TTL/CMOS compatible
- Available in SOL-16

Applications

- RGB drivers
- RGB multiplexers
- RGB gain blocks
- Video gain blocks
- Coax cable driver
- ADC drivers/input multiplexer

Ordering Information

Part No.	Temp. Range	Package	Outline#
EL4393CN	−40°C to +85°C	16-Lead P-DIP	MDP0031
EL4393CM	−40°C to +85°C	16-Lead SOL	MDP0027

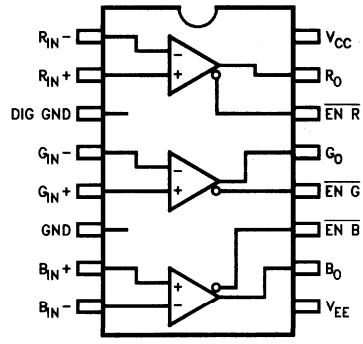
General Description

The EL4393C is three wideband current-feedback amplifiers optimized for video performance. Each amplifier can drive a load of 150Ω at video levels. Each amplifier has a disable capability, which is controlled by a TTL/CMOS compatible logic signal. The EL4393C operates on supplies as low as ±4V up to ±15V.

Being a current-feedback design, the bandwidth stays relatively constant at approximately 80 MHz over the ±1 to ±10 gain range. The EL4393C has been optimized for use with 1300Ω feedback resistors at a gain of 2.

When the outputs are disabled, the supply current consumption drops, by about 4 mA per channel that is disabled. This feature can be used to reduce power dissipation.

Connection Diagram



4393-1

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V_S^+ and V_S^-	+33V	Operating Ambient Temperature Range	−40°C to +85°C
Voltage at V_S^+	+18V	Operating Junction Temperature	150°C
Voltage at V_S^-	−18V	Storage Temperature Range	−65°C to +150°C
Voltage between V_{IN}^+ and V_{IN}^-	±6V	Lead Temperature (Soldering <10 seconds)	300°C
Current into V_{IN}^+ or V_{IN}^-	5 mA		
Internal Power Dissipation	See Curves		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1 KΩ

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	+25°C		2	12	I	mV
TCV_{OS}	Temperature Coefficient of V_{OS}	Full		50		V	µV/°C
I_B^+	I_{IN}^+ Input Bias Current	+25°C		0.2	5	I	µA
I_B^-	I_{IN}^- Input Bias Current	+25°C		10	65	I	µA
TCI_B^-	Temperature Coefficient of I_B^-	Full		25		V	nA/°C
CMRR	Common-Mode Rejection Ratio (Note 1)	+25°C	50	58		I	dB
−ICMR	I_{IN}^- Input Common-Mode Current (Note 1)	+25°C		3	8	I	µA/V
PSRR	Power Supply Rejection Ratio (Note 2)	+25°C	50	58		I	dB
−IPSR	I_{IN}^- Current Supply Rejection (Note 2)	+25°C		2	5	I	µA/V
R_{OL}	Transimpedance	+25°C	100	217		I	kΩ
R_{IN}	IN^+ Input Impedance	+25°C		2		I	MΩ
V_{IN}	IN^+ Input Range	+25°C	±13	±13.5		I	V
V_O	Output Voltage Swing; R_L = 1 kΩ	+25°C	±12	±13		I	V

EL4393C
Triple 80 MHz Video Amplifier w/Disable

Open Loop DC Electrical Characteristics Supplies at ±15V, Load = 1KΩ — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_{SC}	Short-Circuit Current (Note 3)	+25°C	40	70		I	mA
$I_{O, DIS}$	Output Current when Disabled	+25°C		5	150	I	μA
DIS V_{IL}	Disable Voltage for Logic Low	+25°C			0.8	I	V
DIS V_{IH}	Disable Voltage for Logic High	+25°C	2.2			I	V
DIS I_{IL}	Disable Logic Low Input Current	+25°C		3	25	I	μA
DIS I_{IH}	Disable Logic High Input Current	+25°C		0	5	I	μA
$I_{CC (en)}$	Positive Supply Current all Channels Enabled	+25°C	15	20	27	I	mA
$I_{CC (dis)}$	Positive Supply Current all Channels Disabled	+25°C	6	11	16	I	mA
$I_{EE (en)}$	Negative Supply Current all Channels Enabled	+25°C	13	18	25	I	mA
$I_{EE (dis)}$	Negative Supply Current all Channels Disabled	+25°C	4	9	14	I	mA

Note 1: V_{CM} = ±10V for V_S = ±15V.
Note 2: V_{OS} is measured at V_S = ±4.5V and V_S = ±16V, both supplies are changed simultaneously.
Note 3: Only one output short circuited. Pulse test or use heatsink.

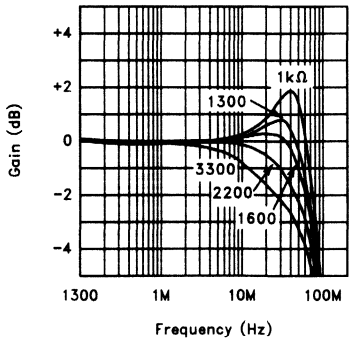
Closed Loop AC Electrical Characteristics Supplies at ±15V, Load = 150Ω and 15 pF, except where noted. Rf1 and Rf2 = 1500Ω; A_V = 2, T_A = 25°C. (See note 8 re: test fixture)

Parameter	Description	Min	Typ	Max	Test Level	Units
SR	Slew Rate (Note 4)		960		V	V/μs
SR	Slew Rate w/ ±5V Supplies (Note 5)		470		IV	V/μs
t_s	Settling Time to 1% $5V_{p-p}$ 5V Step (Note 6)		32		V	ns
BW	Bandwidth, −3 dB ±5V Supplies, −3 dB		80 60		IV IV	MHz MHz
BW	Bandwidth, −0.1 dB ±5V Supplies, −0.1 dB		16 21		IV IV	MHz MHz
Peaking	−3 dB BW Tests		0.6		IV	dB
dG	Differential Gain at 3.58 MHz at ±5V Supplies (Note 7)		0.03 0.30		V V	% %
dθ	Differential Phase at 3.58 MHz at ±5V Supplies (Note 7)		0.088 0.096		V V	(°) (°)

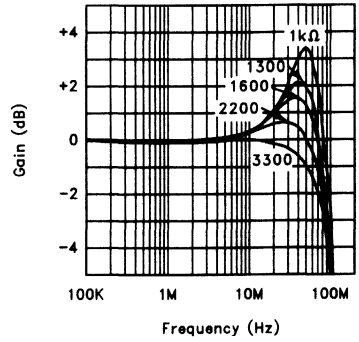
Note 4: R_L = 300Ω, −5V to +5V swing, SR measured at 20% to 80%.
Note 5: −2V to +2V swing, SR measured at 20% to 80%.
Note 6: R_L = 300Ω.
Note 7: DC offset from −0.7V through +0.7V AC amplitude is 286 mV_{P-P}, equivalent to 40 ire.
Note 8: Test fixture was designed to minimize capacitance at the I_N^+ input. A "good" fixture should have less than 2 pF of stray capacitance to ground at this very sensitive pin. See application notes for further details.

Typical Performance Curves

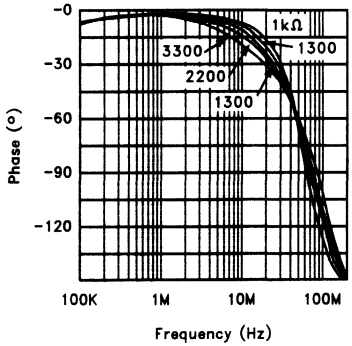
Gain Flatness vs Rf at ± 5V



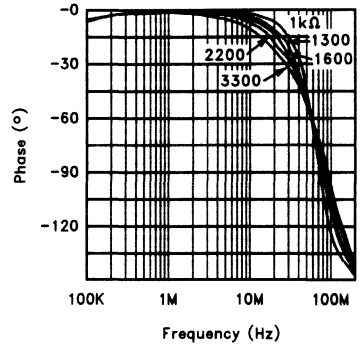
Gain Flatness vs Rf at ± 15V



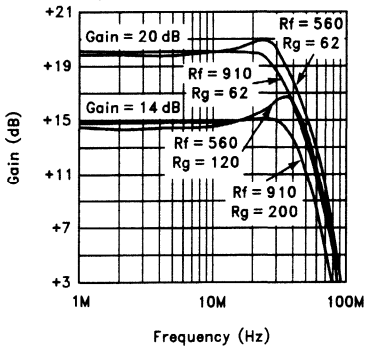
Phase vs Rf at ± 5V



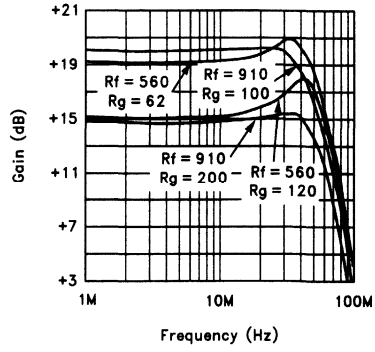
Phase vs Rf at ±15V



Gain of 5, 10 vs Various Rf, Rg at ±5V



Gain of 5, 10 vs Rf, Rg at ± 15V

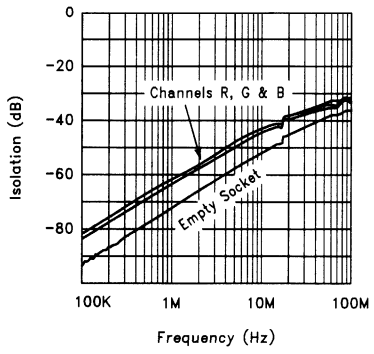


4393-3

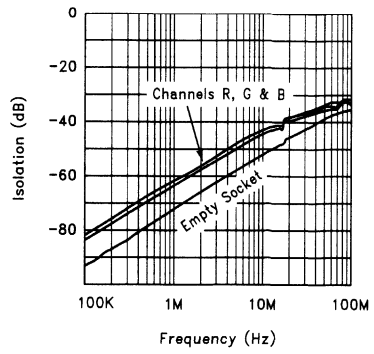
EL4393C
Triple 80 MHz Video Amplifier w/Disable

Typical Performance Curves — Contd.

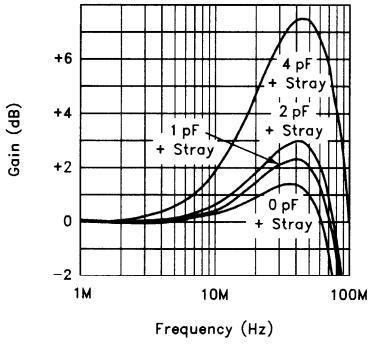
Disabled
Isolation Test at ±5V



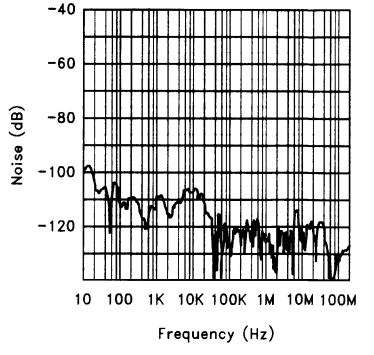
Disabled
Isolation Test at ± 15V



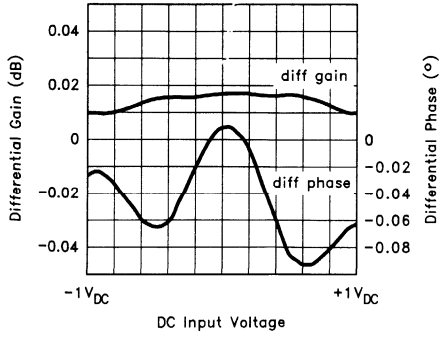
Cin—vs Peaking



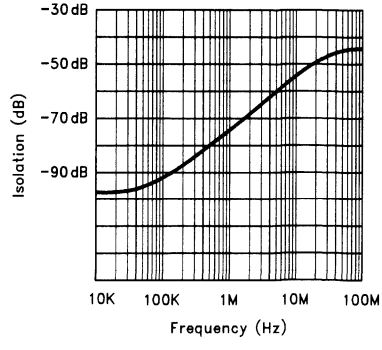
Voltage Noise



Differential Gain & Phase
at 3.58 MHz



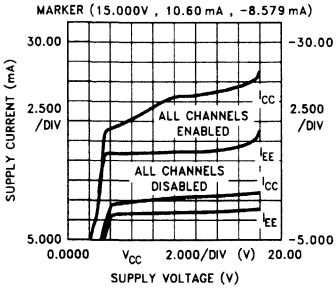
EL4393 MUX Channel
Channel Isolation



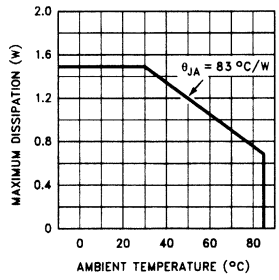
4393-11

Typical Performance Curves — Contd.

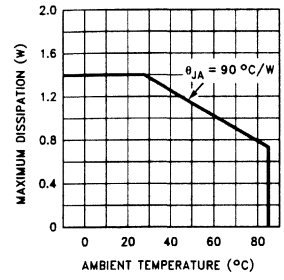
Supply Current vs Supply Voltage



Maximum Power Dissipation vs Ambient Temperature— 16-Pin PDIP

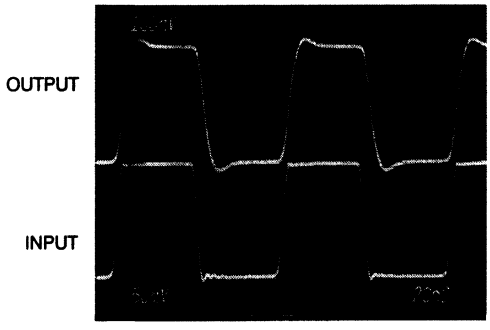


Maximum Power Dissipation vs Ambient Temperature— 16-Pin SOL



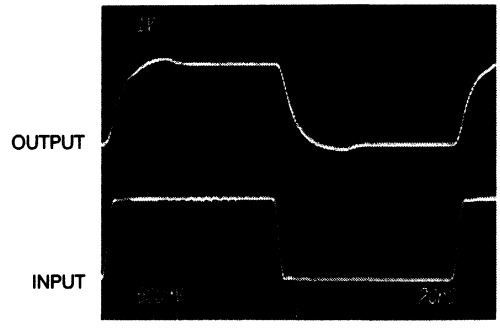
4393-4

Small Signal Pulse Response



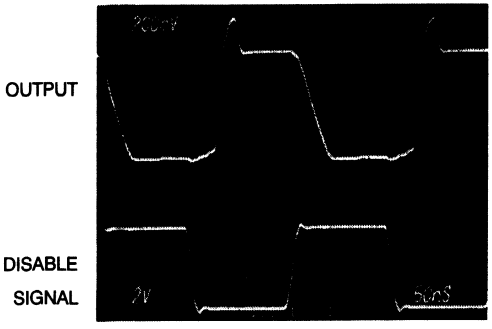
4393-5

Large Signal Pulse Response



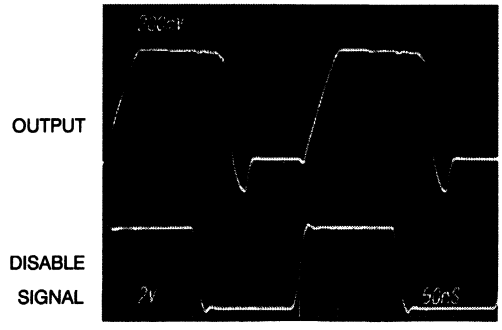
4393-6

Enable/Disable with +VE Voltage Output



4393-7

Enable/Disable with −VE Voltage Output



4393-8

EL4393C
Triple 80 MHz Video Amplifier w/Disable

Typical Application for EL4393, and General Rules for PCB Layout

The figure shows two EL4393's configured as a 2:1 RGB multiplexer, and cable driver, driving 75Ω, back terminated cables. Each channel of the EL4393 is configured to give a gain of two, to make up for the losses of the back terminating resistor.

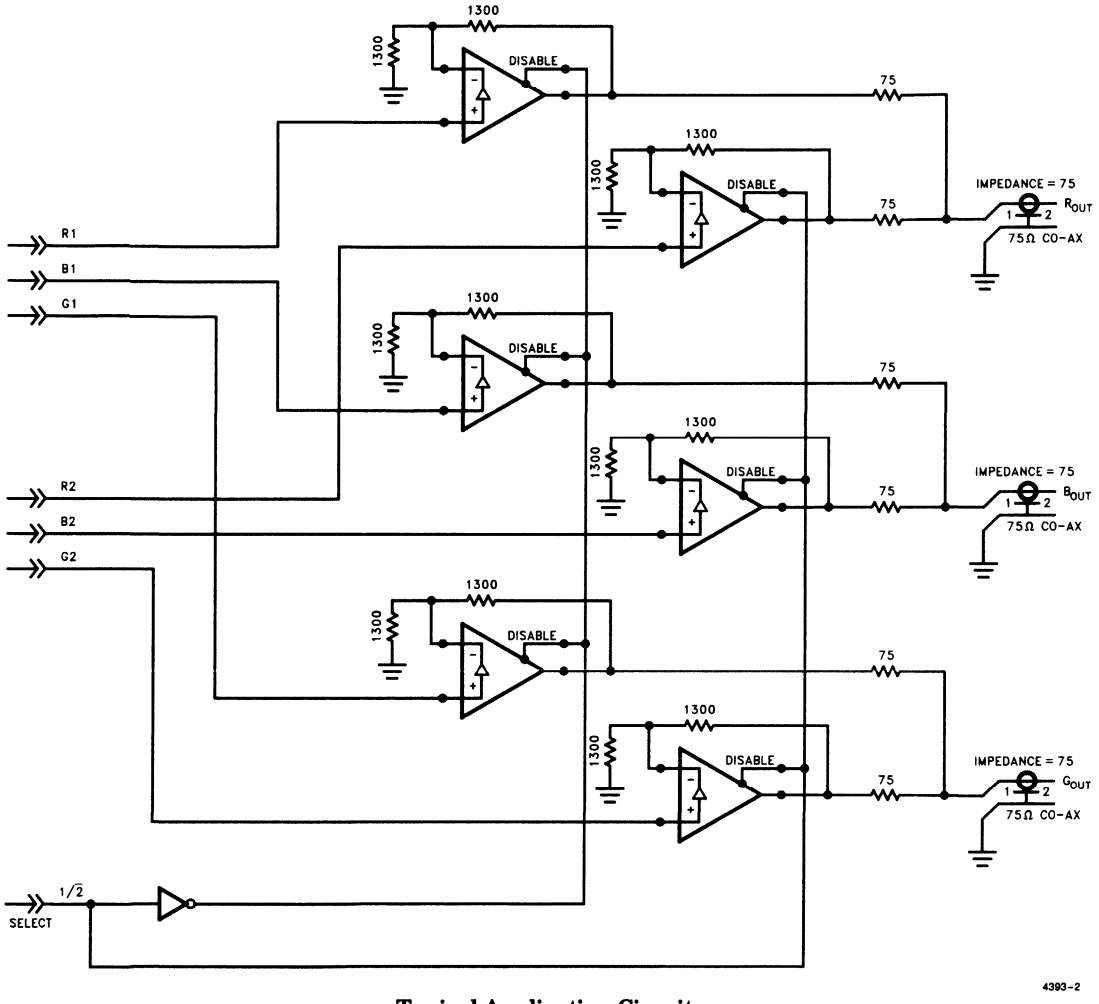
In this example, the Disable pins of each RGB section are driven by a complementary TTL "select" signal. Larger multiplexers can be assembled, with a 1-of-n TTL decoder selecting each RGB triplet.

The circuit gives channel isolations of typically better than −50 dB at 10 MHz, and with a 20 dB/decade slope, extending down to better than −90 dB at frequencies below 100 kHz.

The schematic does not show things like power supply decoupling, or pcb layout, grounding and signal returns, but these will all affect the overall performance of the circuit, and care should be taken with these aspects.

It is recommended that the V_{CC} and V_{EE} pins each be decoupled by a 0.1 μF NPO or X7R dielectric ceramic capacitors to ground within 0.1 inch of the part, and in parallel with the 0.1 μF, A 47 μF tantalum capacitor, also to ground. The 47 μF capacitors should be within 0.25 inch of their power pins. The ground plane should be underneath the package, but cut away from the In− inputs. Care should be taken with the center channel feedback—it must be kept away from any of the in+ or in− pins, if it has to go under the package. Route the G-out line between the pin 3 ground and the pin 4 In− if going under the package is essential. Otherwise, loop the G-out trace around all the other circuitry, to its Rf resistor. The Rf and if used, Rg resistors should be on the input side of the package, to minimize trace length on the In− pins.

The digital input disables are on the output side of the package, so that a good ground plane down the center of the board underneath the package will isolate any fast edges from the sensitive inputs.



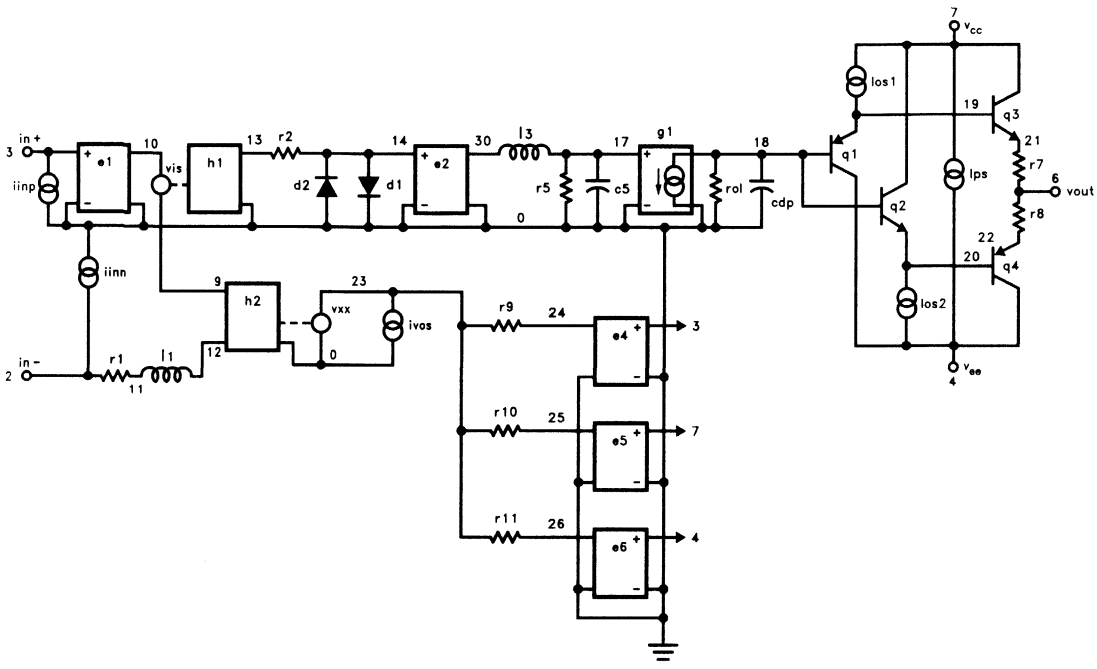
Typical Application Circuit

EL4393C
Triple 80 MHz Video Amplifier w/Disable

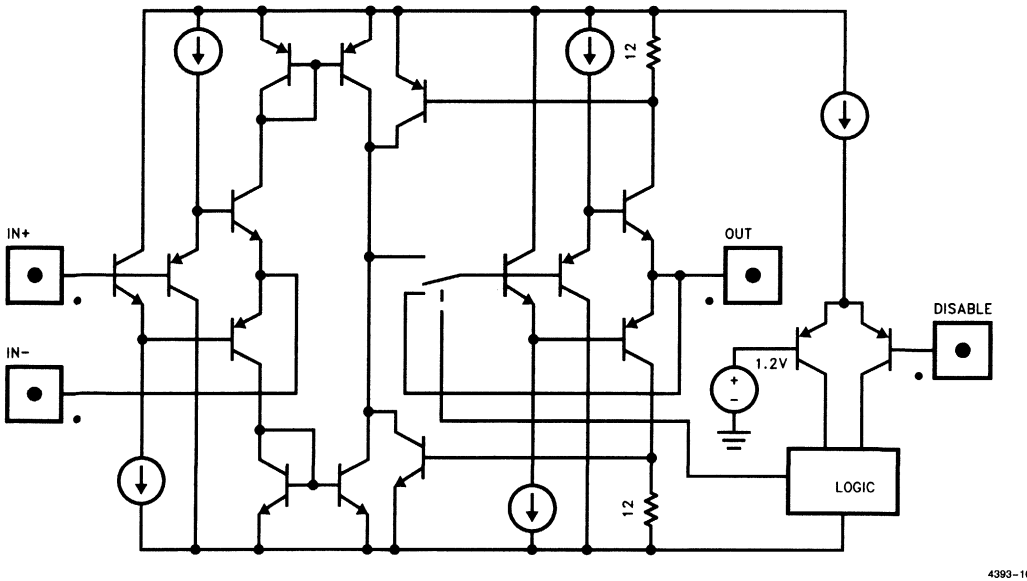
EL4393C Macromodel

```
* Revision A, July 1993
* Enhancements include PSRR, CMRR, and Slew Rate Limiting
* Connections:          +input
*                       |    -Input
*                       |    |    +Vsupply
*                       |    |    |    -Vsupply
*                       |    |    |    |    Putput
*                       |    |    |    |    |
* subckt EL4393/EL       3    2    7    4    6
*
* Input Stage
*
e1 10 0 3 0 1.0
vis 10 9 0V
h2 9 12 vxx 1.0
r1 2 11 50
l 1 11 12 29 nH
iinp 3 0 0.2 µA
iinm 2 0 10 µA
*
* Slew Rate Limiting
*
h1 13 0 vis 600
r2 13 14 1K
d1 14 0 dclamp
d2 0 14 dclamp
*
* High Frequency Pole
*
e2 30 0 14 0 0.00166666666
l5 30 17 1.2 µH
c5 17 0 1 pF
r5 17 0 500
*
* Transimpedance Stage
*
g1 0 18 17 0 1.0
rol 18 0 250k
cdp 18 0 2.2 pF
*
* Output Stage
*
q1 4 18 19 qp
q2 7 18 20 qn
q3 7 19 21 qn
q4 4 20 22 qp
r7 21 6 4
r8 22 6 4
ios1 7 19 2.5 mA
ios2 20 4 2.5 mA
*
* Error Terms
*
ivos 0 23 2 mA
vxx 23 0 0V
e4 24 0 3 0 1.0
e5 25 0 7 0 1.0
e6 26 0 4 0 1.0
r9 24 23 1K
r10 25 23 1K
r11 26 33 1K
*
* Models
*
.model qn npn (is = 5e-15 bf = 100 tf = 0.2nS)
.model qp pnp (is = 5e-15 bf = 100 tf = 0.2nS)
.model dclamp d (is = 1e-30 ibv = 0.266 bv = 1.5 n = 4)
.ends
```

EL4393C Macromodel — Contd.



4393-9



4393-10

Simplified Schematic of One Channel of EL4393

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4421C/22C/41C/42C/43C/44C
Multiplexed-Input Video Amplifiers

Features

- Unity or + 2-gain bandwidth of 80 MHz
- 70 dB off-channel isolation at 4 MHz
- Directly drives high-impedance or 75Ω loads
- <0.05% and 0.05° differential gain and phase errors
- 8 ns switching time
- <150 mV switching glitch
- 0.2% loaded gain error
- Compatible with ±5V to ±15V supplies
- 160 mW maximum dissipation at ±5V supplies

Ordering Information

Part No.	Temp. Range	Package	Outline
EL4421CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL4421CS	−40°C to +85°C	8-Pin SO	MDP0027
EL4422CN	−40°C to +85°C	8-Pin PDIP	MDP0031
EL4422CS	−40°C to +85°C	8-Pin SO	MDP0027
EL4441CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4441CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4442CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4442CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4443CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4443CS	−40°C to +85°C	14-Pin SO	MDP0027
EL4444CN	−40°C to +85°C	14-Pin PDIP	MDP0031
EL4444CS	−40°C to +85°C	14-Pin SO	MDP0027

General Description

The EL44XX family of video multiplexed-amplifiers offers a very quick 12 ns switching time and low glitch along with very low video distortion. The amplifiers have good gain accuracy even when driving low-impedance loads. To save power, the amplifiers do not require heavy loading to remain stable.

The EL4421 and EL4422 are two-input multiplexed amplifiers. The -inputs of the input stages are wired together and the device can be used as a pin-compatible upgrade from the MAX453.

The EL4441 and EL4442 have four inputs, also with common feedback. These may be used as upgrades of the MAX454.

The EL4443 and EL4444 are also 4-input multiplexed amplifiers, but both positive and negative inputs are wired separately. A wide variety of gain- and phase-switching circuits can be built using independednt feedback paths for each channel.

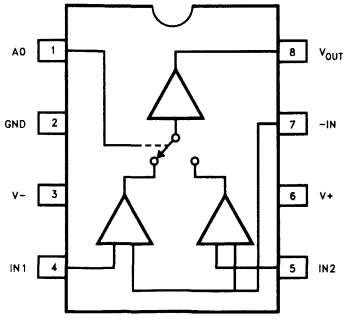
The EL4421, EL4441, and EL4443 are internally compensated for unity-gain operation. The EL4422, EL4442, and EL4444 are compensated for gains of +2 or more, especially useful for driving back-matched cables.

The amplifiers have an operational temperature of −40°C to +85°C and are packaged in plastic 8- and 14-pin DIP and 8- and 14-pin SO.

The EL44XX multiplexed-amplifier family is fabricated with Elantec's proprietary complementary bipolar process which gives excellent signal symmetry and is very rugged.

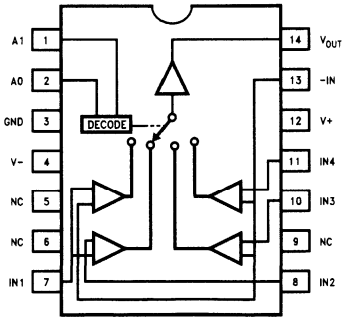
Connection Diagrams

EL4421/EL4422



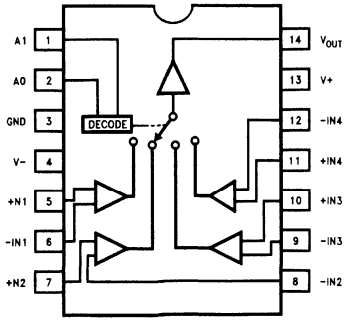
4421-1

EL4441/EL4442



4421-2

EL4443/EL4444



4421-3

Absolute Maximum Ratings

V+	Positive Supply Voltage	18V	V_{LOGIC}	Voltage at A0 or A1	−1V to 6V
V_S	V+ to V− Supply Voltage	33V	I_{IN}	Current into any Input,	4 mA
V_{IN}	Voltage at any Input or Feedback	V+ to V−		Feedback, or Logic Pin	
ΔV_{IN}	Difference between Pairs of		I_{OUT}	Output Current	30 mA
	Inputs or Feedback	6V	P_D	Maximum Power Dissipation	See Curves

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open-Loop DC Electrical Characteristics

Power supplies at ±5V, T_A = 25°C unless otherwise specified

Parameter	Description		Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	'21, '41, and '43	−8	±3	8	I	mV
		'22, '42, and '44	−6	±2	6	I	
I_B	Input Bias Current, Positive Inputs Only of the '21, '22, '41, '42, and All Inputs of the '43 and '44		−10	−5	0	I	µA
I_{FB}	Input Bias Currents of Common Feedback						
		−'21 and '22	−20	−10	0	I	µA
		−'41 and '42	−40	−20	0	I	µA
I_{OS}	Input Offset Currents of the '43 and '44			100	350	I	nA
E_G	Gain Error of the '21, '22, '41 and '42 (Note 1)			0.2	0.4	I	%
A_{VOL}	Open-Loop Gain (Note 1)	EL4443	350	750		I	V/V
		EL4444	600	900		I	V/V
V_{IN}	Input Signal Range EL4421 and EL4441 (Note 2)		±2.8	±3		I	V
CMRR	Common-Mode Rejection Ratio EL4443 and EL4444		70	90		I	dB

Open-Loop DC Electrical Characteristics — Contd.

Power supplies at ±5V, T_A = 25°C unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
CMIR	Common-Mode Input Range (Note 3) EL4443 and EL4444	±2.5	±3		I	V
V_{OUT}	Output Swing	±2.8	±3		I	V
I_{SC}	Output Short-Circuit Current	±80	±120		I	mA
F_T	Unselected Channel Feedthrough Attenuation (Note 1)	70	80		I	dB
I_{LOGIC}	Input Current at A0 and A1 with Input = 0V and 5V		−8	±50	I	µA
V_{LOGIC}	Logic Valid High and Low Input Levels	0.8		2	I	V
I_S	Supply Current EL4421 and EL4422 EL4441, EL4442, EL4443, and EL4444		11 13	14 16	I I	mA

Note 1: The '21, '41, and '43 devices are connected for unity-gain operation with 75Ω load and an input span of ±1V. The '22, '42, and '44 devices are connected for a gain of +2 with a 150Ω load and a ±1V input span.

Note 2: The '21 and '41 devices are connected for unity gain with a ±3V input span while the output swing is measured.

Note 3: CMIR is assured by passing the CMRR test at input voltage extremes.

Closed-Loop AC Electrical Characteristics

Power supplies at ±5V. T_A = 25°C, for EL4421, EL4441, and EL4443 A_V = +1 and R_L = 500Ω, for EL4422, EL4442, and EL4444 A_V = +2 and R_L = 150Ω with R_F = R_G = 270Ω and C_F = 3 pF; for all C_L = 15 pF

Parameter	Description	Min	Typ	Max	Test Level	Units
BW − 3 dB	−3 dB Small-Signal Bandwidth		80		V	MHz
BW ± 0.1 dB	0.1 dB Flatness Bandwidth		10		V	MHz
Peaking	Frequency Response Peaking		0.7		V	dB
SR	Slewrate, V_{OUT} between −2.5V and +2.5V					
	EL4421, EL4441, EL4443	130	200		I	V/µsec
	EL4422, EL4442, EL4444	160	230		I	V
V_n	Input-Referred Noise Voltage Density					
	EL4421, EL4441, EL4443		15		V	nV/rt-hz
	EL4422, EL4442, EL4444		10		V	nV/rt-hz
d_G	Differential Gain Error, V_{OFFSET} between −0.7V and +0.7V					
	EL4421, EL4441, EL4443 (V_S = ±12V)		0.02		V	%
	EL4421, EL4441, EL4443		0.10		V	%
	EL4422, EL4442, EL4444 (V_S = ±12V)		0.02		V	%
	EL4422, EL4442, EL4444		0.10		V	%

Closed-Loop AC Electrical Characteristics

Power supplies at ±5V. T_A = 25°C, for EL4421, EL4441, and EL4443 A_V = +1 and R_L = 500Ω, for EL4422, EL4442, and EL4444 A_V = +2 and R_L = 150Ω with R_F = R_G = 270Ω and C_F = 3 pF; for all C_L = 15 pF — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
d∅	Differential Phase Error, V_{OFFSET} between −0.7V and +0.7V					
	EL4421, EL4441, EL4443 (V_S = ±12V)		0.02		V	°
	EL4421, EL4441, EL4443		0.06		V	°
	EL4422, EL4442, EL4444 (V_S = ±12V)		0.02		V	°
	EL4422, EL4442, EL4444		0.06		V	°
T_{MUX}	Multiplex Delay Time, Logic Threshold to 50% Signal Change		12		V	ns
V_{GLITCH}	Peak Multiplex Glitch		120		V	mV
ISO	Channel Off Isolation at 3.58 MHz (See Text)					
	EL4421, EL4441, EL4443		72		V	dB
	EL4422, EL4442, EL4444		61		V	dB

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4581C
Video Sync Separator

Features

- NTSC, PAL and SECAM sync separation
- Single supply, +5V
- Precision 50% slicing, internal caps
- Built-in color burst filter
- Decodes non-standard verticals
- Pin compatible with LM1881
- Low power
- Typically 1.5 mA supply current
- Resistor programmable scan rate
- Few external components
- Available in 8-pin DIP and SO-8 pkg.

Applications

- Video special effects
- Video test equipment
- Video distribution
- Displays
- Imaging
- Video data capture
- Video triggers

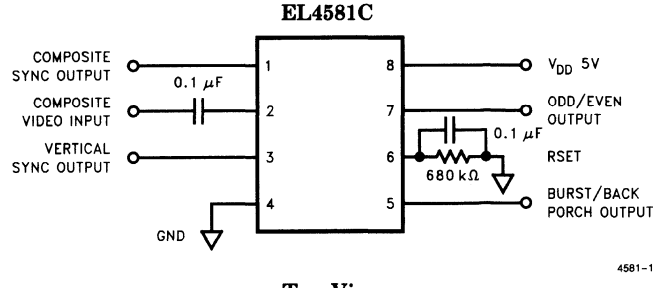
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4581CN	0°C to +75°C	8-Pin DIP	MDP0031
EL4581CS	0°C to +75°C	8-Lead SO	MDO0027

General Description

The EL4581C video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts timing information including composite sync, vertical sync, burst/back porch timing and odd/even field information from standard negative going sync NTSC, PAL®, and SECAM video signals. The EL4581C will detect video signals from 0.5 to $2V_{P-P}$. The 50% slicing feature provides precise sync edge detection even in the presence of noise and variable signal amplitudes. A built in linear phase, third order, color burst filter minimizes spurious timing information and reduces external components. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals by changing an external horizontal scan rate setting resistor. The vertical output is produced on the rising edge of the first serration in the vertical sync period. A default vertical output is produced after an internally generated time delay in the event of missing serration pulses, for example, in the case of a non-standard video signal. All outputs are active low.

Connection Diagram



Top View

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Pin Voltages	−0.5V to V_{CC} +0.5V
Storage Temperature	−65°C to +150°C	Operating Temperature Range	0°C to 75°C
Lead Temperature	260°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics Unless otherwise state V_{DD} = 5V, T_A = 25°C, R_{set} = 680 kΩ.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C	0.75	1.7	3	I	mA
Clamp Voltage	Pin 2, Unloaded	25°C	1.3	1.5	1.9	I	V
Discharge Current	Pin 2 = 2V	25°C	6	10	20	I	µA
Clamp Charge Current	Pin 2, V_{IN} = 1V	25°C	2	3		I	mA
Ref Voltage	Pin 6, V_{DD} = 5V (Note 2)	25°C	1.5	1.8	2.1	I	V
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA	25°C			800	I	mV
V_{OH} Output High Voltage	I_{OH} = −40 µA I_{OH} = −1.6 mA	25°C	4 2.4			IV I	V

Note 1: No video signal, outputs unloaded.
Note 2: Tested for V_{DD} 5V ±5% which guarantees timing of output pulses over this range.

EL4581C
Video Sync Separator

Dynamic Characteristics

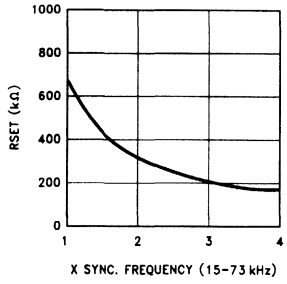
V_{DD} = 5V, I_V pk-pk video, T_A = 25°C, C_L = 15 pF, I_{OH} = −1.6 mA, I_{OL} = 1.6 mA. Signal voltages are peak to peak.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Vertical Sync Width	(Note 3)	25°C	190	230	300	I	µs
Burst Gate Width	(Note 3)	25°C	2.5	3.5	4.5	I	µs
Vertical Default Time		25°C	40	55	70	I	µs
Filter Attenuation	F_{IN} = 3.4 MHz (Note 4)	25°C		24		V	dB
Propagation Delay	V_{IN} − Composite Sync (Note 3)	25°C		260	400	I	ns
Input Signal Dynamic Range	p-p NTSC Signal (Note 5)	25°C	0.5		2	I	V
Sync. Slice Level	Input Voltage = $1V_{P-P}$ (Note 6)	25°C Full	40% 40%	50% 50%	60% 60%	I IV	

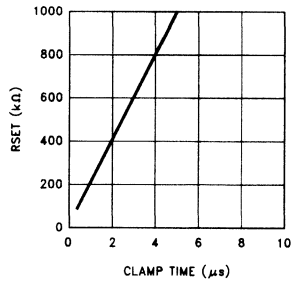
Note 3: C/S, Vertical and Burst outputs are all active low − V_{OH} = 2.4V, V_{OL} = 0.8V.
Note 4: Attenuation is a function of Rset (PIN6).
Note 5: Typical min. is 0.3 V_{P-P}.
Note 6: Refers to threshold level of sync. tip to back porch amplitude.

Typical Performance Characteristics

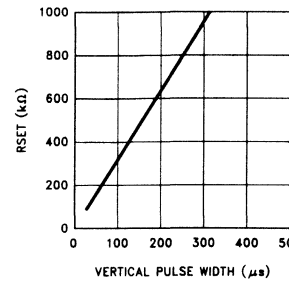
RSET Value Selection vs Horizontal Scan Rate



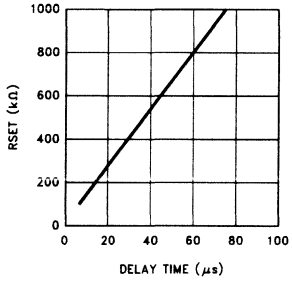
Back Porch Clamp On Time vs RSET



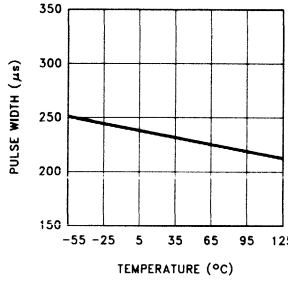
Vertical Pulse Width vs RSET



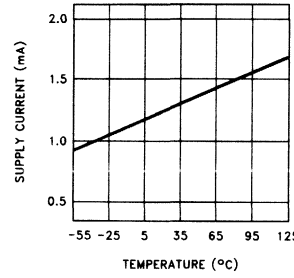
Vertical Default Delay Time vs RSET



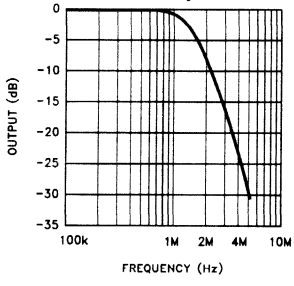
Vertical Pulse Width vs Temperature



Supply Current vs Temperature



Input Signal = 300 mV$_{P-P}$ EL4581 Filter Characteristic Constant Delay 240 ns

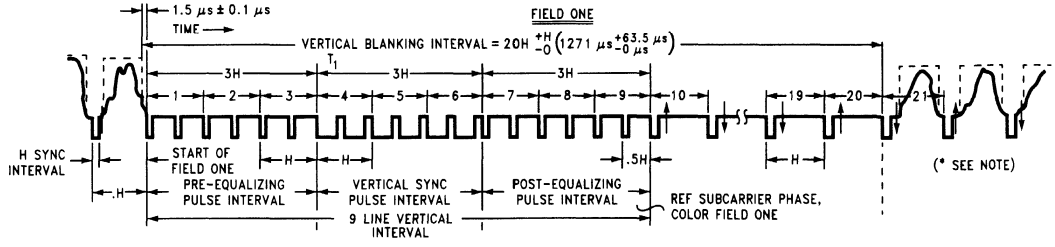


4581-2

EL4581C
Video Sync Separator

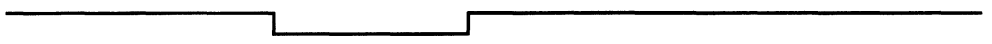
Timing Diagrams

SIGNAL 1a. COMPOSITE VIDEO INPUT, FIELD ONE

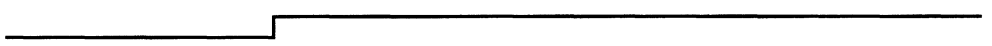


SIGNAL 1b. COMPOSITE SYNC. OUTPUT, PIN 1

SIGNAL 1c. VERTICAL SYNC. OUTPUT, PIN 3



SIGNAL 1d. ODD – EVEN OUTPUT, PIN 7



SIGNAL 1e. BACK PORCH OUTPUT, PIN 5

4581-3

Figure 1

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

* Signal 1a drawing reproduced with permission from EIA.

Description of Operation

A simplified block schematic is shown in Figure 2. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC coupled to pin 2 via the capacitor C_1, nominally 0.1 μF. The clamp circuit A1 will prevent the input signal on pin 2 going any more negative than 1.5V, the value of reference voltage V_{R1}. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I_1, nominally 10 μA, charges the coupling capacitor during the remaining portion of the H line, approximately 58 μs for a 15.75 kHz timebase. From $I \bullet t = C \bullet V$, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x 12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C_I will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be V_{DD} less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I_1 directly tracks reference current I_{TR} and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24 dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6 dB to improve the detection accuracy. Note that the filter cut-off frequency is a function of RSET through I_{OT} and is proportional to I_{OT}.

Internal reference voltages (block V_{REF}) with high immunity to supply voltage variation are derived on the chip. Reference V_{R4} with op-amp A2 forces pin 6 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance RSET will determine the value of the reference current I_{TR}. The internal resistance R3 is only about 6 kΩ, much less than RSET. All the internal timing functions on the chip are referenced to I_{TR} and have excellent supply voltage rejection.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync. pulse with a threshold voltage V_{R2} which is referenced at a fixed level above the clamp voltage V_{R1}. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8 μs to enable the actual sample of 2 μs to be taken on the optimum section of the sync. pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track RSET through I_{OT}.

The 50% level of the sync tip is derived, through the resistor divider R1 and R2, from the sample and held voltages V_{TIP} and V_{BP}, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S ouput buffer B1 and the other internal circuit blocks, the vertical, back porch and odd/even functions.

The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer

EL4581C
Video Sync Separator

Description of Operation — Contd.

vertical sync. pulse widths. The internal timing circuits are referenced to I_{OT} and V_{R3}, the time-out period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absense of a serration pulse, an internal timer will default the start of vertical.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of I_{OT} and will therefore track the scan rate set by RSET.

The odd/even circuit (O/E) comprises of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 7 is high during the odd field.

Loss of video signal can be detected by monitoring the C/S output. The 50% level of the previous video signal will remain held on the S/H capacitors after the input video signal has gone and the input on pin 2 has defaulted to the clamp voltage. Consequently the C/S output will remain low longer than the normal vertical pulse period. An external timing circuit could be used to detect this condition.

Block Diagram

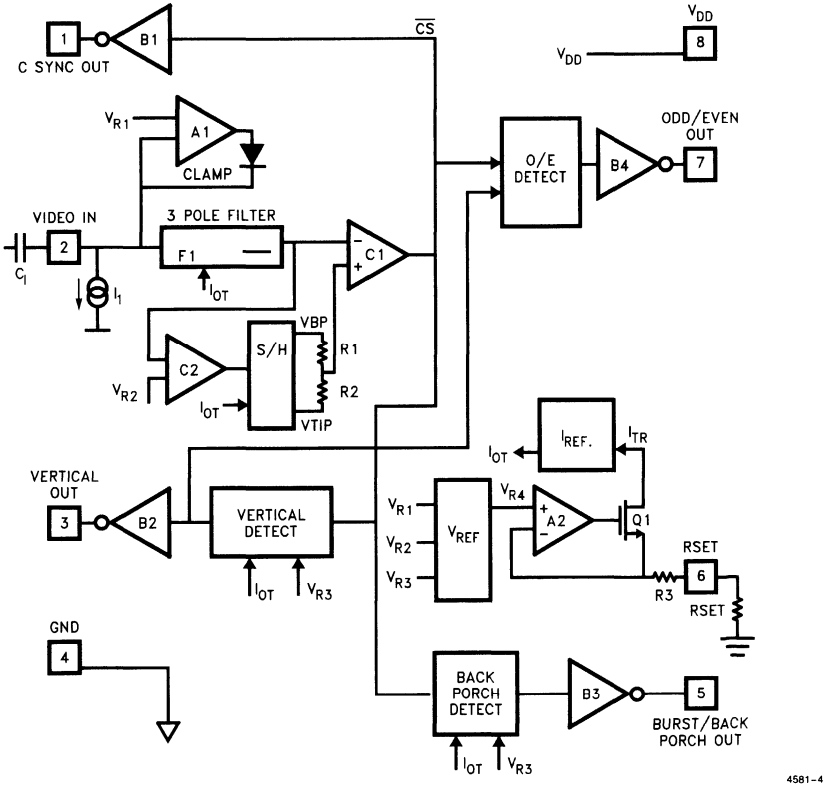


Figure 2

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL4583C
Video Sync Separator

Features

- NTSC, PAL and SECAM sync separation
- Single supply, +5V operation
- Precision 50% slicing, internal caps
- Built in programmable color burst filter
- Decodes non-standard verticals
- Horizontal sync output
- Sync. pulse amplitude output
- Same socket can be used for 8-pin EL4581
- Low power CMOS
- Detects loss of signal
- Resistor programmable scan rate
- Few external components
- Available in 16-Pin DIP and SO-16 pkg.

Applications

- Video special effects
- Video test equipment
- Video distribution
- Multimedia
- Displays
- Imaging
- Video data capture
- Video triggers

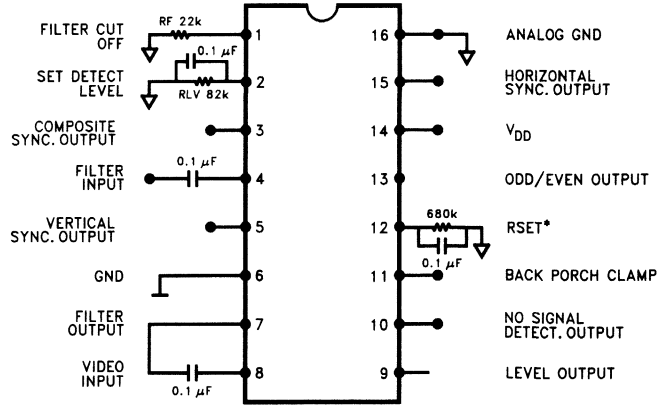
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL4583CN	−40°C to +85°C	16-Pin DIP	MDP0021
EL4583CS	−40°C to +85°C	16-Lead SO	MDO0027

General Description

The EL4583C video sync separator is manufactured using Elantec's high performance analog CMOS process. This device extracts timing information including composite and vertical sync, horizontal output, burst/back porch timing, and odd/even field information from standard negative going sync NTSC, PAL®, and SECAM video signals with amplitude from 0.5V to 2 V_{p-p}. The Precision 50% slicing feature provides precise sync edge detection in the presence of noise and variable signal amplitudes. An optional built in linear phase, third order, color burst filter minimizes spurious timing information and reduces external components. The integrated circuit is also capable of providing sync separation for non-standard, faster horizontal rate video signals by changing an external horizontal scan rate setting resistor. The vertical output is produced on the rising edge of the first serration in the vertical sync period. The vertical and odd-even detection circuits have improved immunity to spurious noise pulses in the input signal. Additional features include a minimum signal level detection output. A default vertical output is produced after a time delay if the rising edge mentioned above does not occur within the internally set delay period, such as might be the case for a non-standard video signal. Level out signal provides a d.c. measure of the sync. pulse amplitude, which can be used for AGC applications.

Connection Diagram



Top View

*Note: R SET must be a 1% resistor.

EL4583C
Video Sync Separator

Absolute Maximum Ratings (T_A = 25°C)

V_{CC} Supply	7V	Pin Voltages	−0.5V to V_{CC} +0.5V
Storage Temperature	−65°C to +150°C	Operating Temperature Range	−40°C to +85°C
Lead Temperature	260°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level / Test Procedure
100% production tested and QA sample tested per QA test plan QCX0002.
100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C.
QA sample tested per QA test plan QCX0002.
QA sample tested per QA test plan QCX0002.
Parameter is guaranteed (but not tested) by Design and Characterization Data.
Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (V_{DD} = 5V, T_A = 25°C, RSET = 680k, RF = 22k, RLV = 82k)

Parameter	Description	Temp	Min	Typ	Max		Units
I_{DD}	V_{DD} = 5V (Note 1)	25°C		2.5	4		mA
Clamp Voltage	Pins 4, 8, unloaded	25°C	1.3	1.55	1.8		V
Discharge Current	Pins 4, 8, with Signal (Note 2) No Signal	25°C	3	1 6	12		µA
Clamp Charge Current	Pins 4, 8, V_{IN} = IV	25°C	2	3	4		mA
Ref. Voltage V_{REF}	Pin 12, V_{DD} = 5V (Note 3)	25°C	1.5	1.75	2		V
Filter Reference Voltage, VRF	Pin 1	25°C	0.35	0.5	0.65		V
Level Reference Current	Pin 2 (Note 4)	25°C	1.5	2.5	3.5		µA
V_{OL} Output Low Voltage	I_{OL} = 1.6 mA	25°C		350	800		mV
V_{OH} Output High Voltage	I_{OH} = −40 µA I_{OH} = −1.6 mA	25°C	4 2.4	4			V

Note 1: No video signal, outputs unloaded.
Note 2: At loss of signal (pin 10 high) the pull down current source switches to a value of 10 µA.
Note 3: Tested for V_{DD} 5V ±5%.
Note 4: Current sourced from pin 2 is V_{REF}/RSET.

EL4583C

Dynamic Characteristics

RF = 22 kΩ, RSET = 680 kΩ, V_{DD} = 5V, 1 V_{p-p} VIDEO, T_A = 25°C, C_L = 15 pF, I_{OH} = −1.6 mA, I_{OL} = 1.6 mA

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
Horizontal Pulse Width, Pin 15	(Note 5)	25°C	3.8	5	6.2		µs
Vertical Sync Width, Pin 5	(Note 6)	25°C		192.6			µs
Back Porch Width, Pin 11	(Note 5)	25°C	2.7	3.7	4.7		µs
Filter Attenuation	F_{IN} = 3.6 MHz (Note 7)	25°C		12			dB
Propagation Delay	V_{IN} (Pin 4)—Comp Sync	25°C		250	350		ns
Input Signal Dynamic Range	p-p NTSC Signal (Note 8)	25°C	0.4		2		V
Sync Slice Level	Input Voltage = 1 V_{p-p} (Note 9)	25°C Full	40% 40%	50% 50%	60% 60%		
Level Out, Pin 9	Input Volatge = 1 V_{p-p} Pin 4		555	620	685		mV
Vertical Default Time	(Note 10)	25°C	27	36	45		µs
Loss of Signal Time-Out	Pin 10	25°C	400	600	800		µs

Note 5: Width is a function of RSET.
Note 6: c/s, Vertical, Back porch and H are all active low, V_{OH} = 0.8V. Vertical is 3H lines wide of NTSC signal.
Note 7: Attenuation is a function of RF. See filter typical characteristics.
Note 8: Typical min is 0.3 V_{p-p}.
Note 9: Refers to threshold level of sync tip to back porch amplitude.
Note 10: Vertical pulse width in absence of serrations on input signal.

Pin Description

Pin No.	Pin Name	Function
1	Filter Cut-Off	A resistor RF connected between this input and ground determines the input filter characteristic. Increasing RF increases the filter 3.58 MHz color burst attenuation. See the graph showing filter characteristics.
2	Set Level	A resistor RLV connected between pin 2 and ground determines the value of the minimum signal which will trigger the loss of signal output on pin 10. The relationship is V_PMIN = 0.75 RLV/RSET, where V_PMIN is the minimum detected sync pulse amplitude applied to pin 4. See characterization curve.
3	Composite Sync Output	This output replicates all the sync inputs on the input video.
4	Filter Input	The filter is a 3 pole active filter with a gain of 2, designed to produce a constant phase delay of nominally 260 ns with signal amplitude. Resistor RF on pin 1 controls the filter cut-off. An internal clamp sets the minimum voltage on pin 4 at 1.55V when the input becomes low impedance. Above the clamp voltage, an input current of 1 µA charges the input coupling capacitor. With loss of signal, the current source switches to a value of 10 µA, for faster signal recovery.
5	Vertical Sync	The vertical sync output is synchronous with the first serration pulse rising edge in the vertical interval of the input signal and ends on the trailing edge of the first equalizing Output pulse after the vertical interval. It will therefore be slightly more than 3H lines wide.

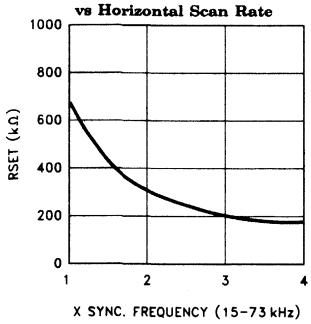
EL4583C
Video Sync Separator

Pin Description — Contd.

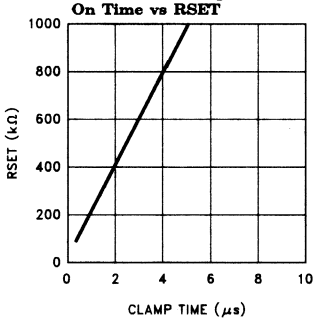
Pin No.	Pin Name	Function
6	Digital Ground	This is the ground return for digital buffer outputs.
7	Filter Output	Output of the active 3 pole filter which has its input on pin 4. It is recommended to ac couple the output to pin 8.
8	Video Input	This input can be directly driven by the signal if it is desired to bypass the filter, for example, in the case of strong clean signals. This input is 6 dB less sensitive than the filter input.
9	Level Output	This pin provides an analog voltage which is nominally equal to twice the sync pulse amplitude of the video input signal applied to pin 4. It therefore provides an indication of signal strength.
10	No Signal Detect Output	This is a digital output which goes high when either a) loss of input signal or b) the input signal level falls below a predetermined amplitude as set by RLV on pin 2. There will be several horizontal lines delay before the output is initiated.
11	Back Porch Clamp	The start of back porch output is triggered on the trailing edge of normal H sync, and on the rising edge of serration pulses in the vertical interval. The pulse is timed out internally to produce a one-shot output. The pulse width is a function of RSET. This output can be used for d.c. restore functions where the back porch level is a known reference.
12	RSET	The current through the resistor RSET determines the timing of the functions within the I.C. These functions include the sampling of the sync pulse 50% point, back porch output and the 2H eliminator. For faster scan rates, the resistor needs to be reduced inversely. The nominal required current out of pin 12 for NTSC 15.7 kHz scan rate is 2.5 μA. RSET must be a 1% resistor.
13	Odd/Even Output	Odd-even output is low for even field and high for odd field. The operation of this circuit has been improved for rejecting spurious noise pulses such as those present in VCR signals.
14	V_{DD} 5V	The internal circuits are designed to have a high immunity to supply variations, although as with most I.C.s a 0.1 μF decoupling capacitor is advisable.
15	Horizontal Sync Output	This output produces only true H pulses of nominal width 5 μs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync. The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2H eliminator circuit.
16	Analog Ground	This is the ground return for the signal paths in the chips, RSET, RF and RLV.

Typical Performance Characteristics

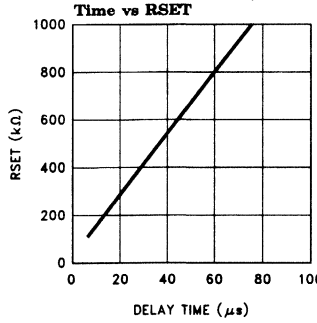
RSET Value Selection vs Horizontal Scan Rate



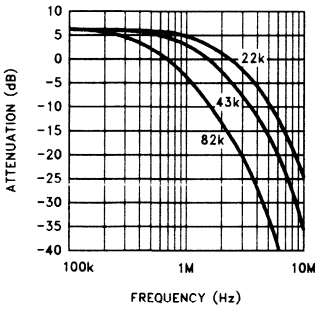
Back Porch Clamp On Time vs RSET



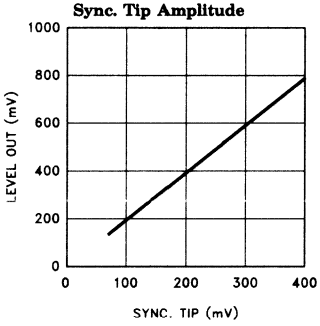
Vertical Default Delay Time vs RSET



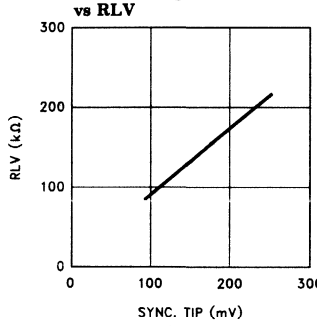
Filter 3 dB BW vs RF



Level Out (Pin 9) vs Sync. Tip Amplitude

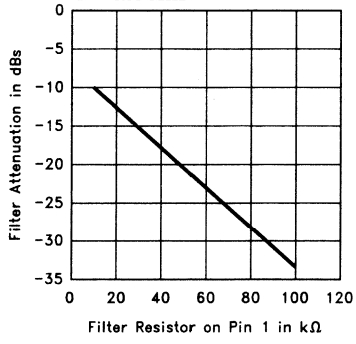


Minimum Signal Detect vs RLV



4583-3

Filter Attenuation vs RF @ f = 3.58 MHz

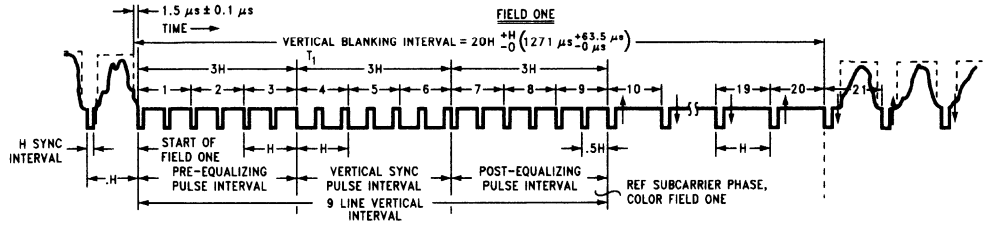


4583-4

Note 1: For RLV < 100 kΩ, no signal detect output (pin 10) will default high at minimum signal sensitivity specification, or at complete loss of signal.

Timing Diagram

SIGNAL 1a. COMPOSITE VIDEO INPUT, FIELD ONE



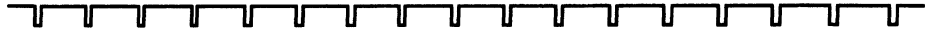
SIGNAL 1b. COMPOSITE SYNC. OUTPUT, PIN 1

SIGNAL 1c. VERTICAL SYNC. OUTPUT, PIN 3

SIGNAL 1d. ODD – EVEN OUTPUT, PIN 7

SIGNAL 1e. BACK PORCH OUTPUT, PIN 5

SIGNAL 1f. HORIZONTAL SYNC. OUTPUT, PIN 15



4583-5

Notes:

b. The composite sync output reproduces all the video input sync pulses, with a propagation delay.

c. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge, with a propagation delay.

d. Odd-even output is low for even field, and high for odd field.

e. Back porch goes low for a fixed pulse width on the trailing edge of video input sync pulses. Note that for serration pulses during vertical, the back porch starts on the rising edge of the serration pulse (with propagation delay).

f. Horizontal sync output produces the true "H" pulses of nominal width of 5μs. It has the same delay as the composite sync.

Description of Operation

A simplified block schematic is shown in Figure 1. The following description is intended to provide the user with sufficient information to be able to understand the effects that the external components and signal conditions have on the outputs of the integrated circuit.

The video signal is AC compuled to pin 4 via the capacitor C_1, nominally 0.1 μF. The clamp circcuit A1 will prevent the input signal on pin 4 going any more negative than 1.5V, the value of reference voltage V_{R1}. Thus the sync tip, the most negative part of the video waveform, will be clamped at 1.5V. The current source I_1, nominally 10 μA, charges the coupling capacitor during the remaining portion of the H line, approximately 58 μs for a 15.75 kHz timebase. From $I \bullet t = C \bullet V$, the video time-constant can be calculated. It is important to note that the charge taken from the capacitor during video must be replaced during the sync tip time, which is much shorter, (ratio of x 12.5). The corresponding current to restore the charge during sync will therefore be an order of magnitude higher, and any resistance in series with C_I will cause sync tip crushing. For this reason, the internal series resistance has been minimized and external high resistance values in series with the input coupling capacitor should be avoided. The user can exercise some control over the value of the input time constant by introducing an external pull-up resistance from pin 2 to the 5V supply. The maximum voltage across the resistance will be V_{DD} less 1.5V, for black level. For a net discharge current greater than zero, the resistance should be greater than 450k. This will have the effect of increasing the time constant and reducing the degree of picture tilt. The current source I_1 directly tracks reference current I_{TR} and thus increases with scan rate adjustment, as explained later.

The signal is processed through an active 3 pole filter (F1) designed for minimum ripple with constant phase delay. The filter attenuates the color burst by 24 dB and eliminates fast transient spikes without sync crushing. An external filter is not necessary. The filter also amplifies the video signal by 6 dB to improve the detection accuracy. The filter cut-off frequency is controlled by an external resistor from pin 1 to ground.

Internal reference voltages (block V_{REF}) with high immunity to supply voltage variation are derived on the chip. Reference V_{R4} with op-amp A2 forces pin 12 to a reference voltage of 1.7V nominal. Consequently, it can be seen that the external resistance RSET will determine the value of the reference current I_{TR}. The internal resistance R3 is only about 6 kΩ, much less than RSET. All the internal timing functions on the chip are referenced to I_{TR} and have excellent supply voltage rejection.

To improve noise immunity, the output of the 3 pole filter is brought out to pin 7. It is recommended to AC couple the output to pin 8, the video input pin. In case of strong clean video signal, the video input pin, pin 8, can be driven by the signal directly.

Comparator C2 on the input to the sample and hold block (S/H) compares the leading and trailing edges of the sync. pulse with a threshold voltage V_{R2} which is referenced at a fixed level above the clamp voltage V_{R1}. The output of C2 initiates the timing one-shots for gating the sample and hold circuits. The sample of the sync tip is delayed by 0.8 μs to enable the actual sample of 2 μs to be taken on the optimum section of the sync. pulse tip. The acquisition time of the circuit is about three horizontal lines. The double poly CMOS technology enables long time constants to be achieved with small high quality on-chip capacitors. The back porch voltage is similarly derived from the trailing edge of sync, which also serves to cut off the tip sample if the gate time exceeds the tip period. Note that the sample and hold gating times will track RSET through I_{OT}.

The 50% level of the sync tip is derived, through the resistor divided R1 and R2, from the sample and held voltages V_{TIP} and V_{BP}, and applied to the plus input of comparator C1. This comparator has built in hysteresis to avoid false triggering. The output of C2 is a digital 5V signal which feeds the C/S output buffer B1 and the other internal circuit blocks, the vertical, back porch and odd/even functions.

EL4583C
Video Sync Separator

Description of Operation — Contd.

The vertical circuit senses the C/S edges and initiates an integrator which is reset by the shorter horizontal sync pulses but times out the longer vertical sync. pulse widths. The internal timing circuits are referenced to I_{OT} and V_{R3}, the timout period being inversely proportional to the timing current. The vertical output pulse is started on the first serration pulse in the vertical interval and is then self-timed out. In the absence of a serration pulse, an internal timer will default the start of vertical.

The Horizontal circuit senses the C/S edges and produces the true horizontal pulses of nominal width 5 μs. The leading edge is triggered from the leading edge of the input H sync, with the same prop. delay as the composite sync. The half line pulses present in the input signal during vertical blanking are eliminated with an internal 2 H eliminator circuit. The 2 H eliminator circuit initiates a time out period after a horizontal pulse if generated. The time out period is a function of I_{OT} which is set by RSET.

The back porch is triggered from the sync tip trailing edge and initiates a one-shot pulse. The period of this pulse is again a function of I_{OT} and will therefore track the scan rate set by RESET.

The odd/even circuit circuit (O/E) is comprised of flip flops which track the relationship of the horizontal pulses to the leading edge of the vertical output, and will switch on every field at the start of vertical. Pin 13 is high during the odd field.

Loss of video signal can be detected by monitoring the No Signal Detect Output pin 10. The VTIP voltage held by the sample and hold is compared with a voltage level set by RLV on pin 2. Pin 10 output goes high when the VTIP falls below RLV set value.

VTIP voltage is also passed through an amplifier with gain of 2 and buffed to pin 9. This is done to provide an indication of signal strength. The Level Output signal can be used for AGC applications.

Block Diagram

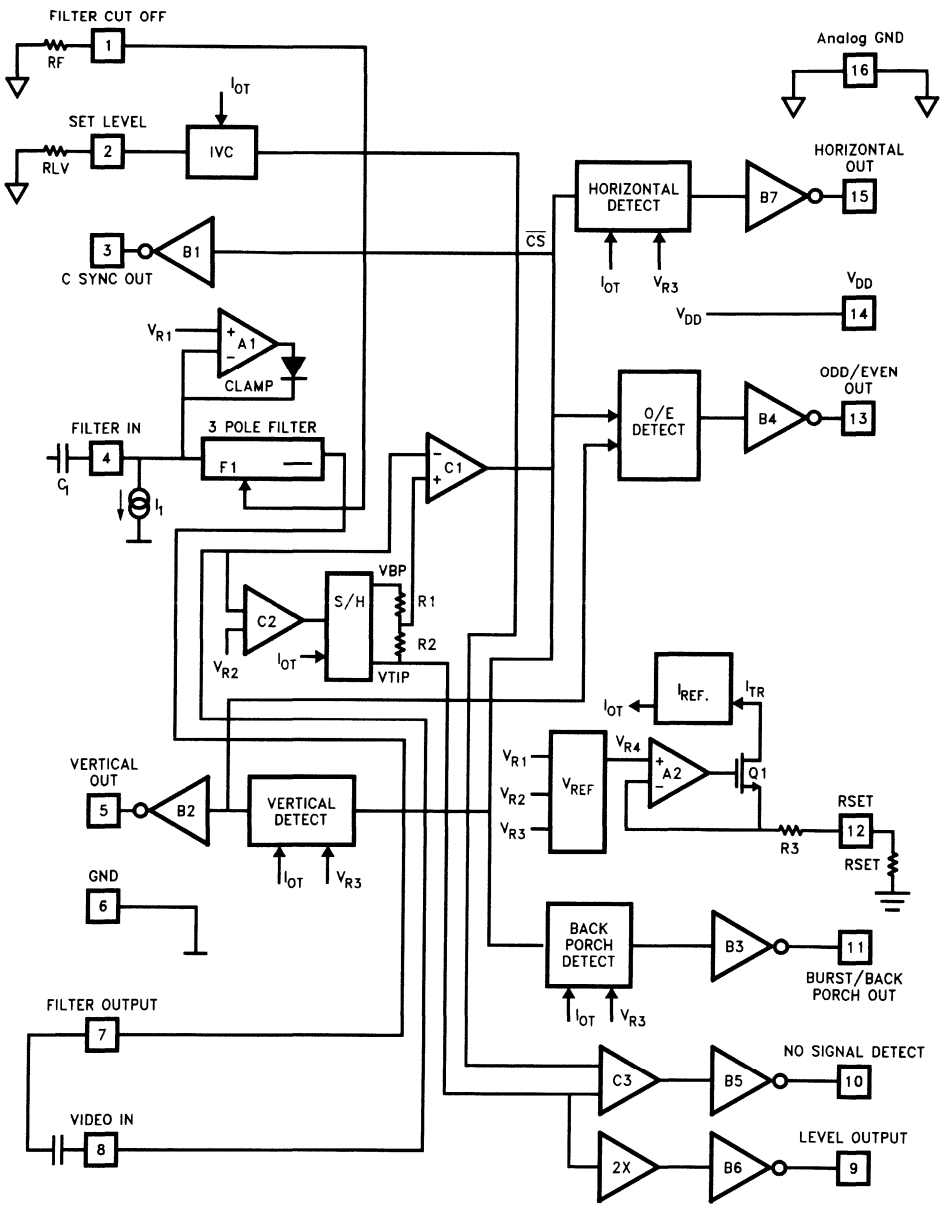


Figure 1

EL5003C
High Speed CRT Amplifier

Features
- Input buffer
- 7.5 V/V nominal gain
- +0 dB to −50 dB gain control
- Clamp/DC-restore
- 300 MHz small-signal bandwidth
- 300 MHz large-signal bandwidth
- 1.5 ns rise and fall time
- 12V supply

Applications
- High resolution CRT driver
- RGB and Monochrome monitors
- HDTV video processing

Ordering Information

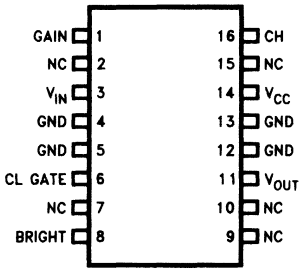
Part No.	Temp. Range	Package	Outline #
EL5003CN	−40°C to +85°C	16-Pin P-DIP	MDP0031

General Description
The EL5003C is a single channel high-speed CRT Amplifier which is intended for use in high resolution monochrome or RGB applications. To drive a CRT, the EL5003C is used with an external high-voltage stage which is directly connected to its output. The EL5003C contains the following blocks:
- A high-bandwidth video amplifier;
- A variable gain control for contrast adjustment; and
- Gated DC-restore circuitry for brightness control.

The EL5003C features 300 MHz of large- and small-signal bandwidth. Rise and fall times are an impressive 1.5 ns for a 4V step. The EL5003C has a voltage gain of 7.5 V/V (with 12V at the GAIN pin), and by reducing the GAIN pin voltage, the video signal can be continuously attenuated by up to 50 dB. A TTL- or CMOS-compatible HIGH signal at the CL GATE pin activates the clamp circuitry to offset the EL5003C's output signal based on the video reference voltage during the Back Porch portion of the input signal. This DC-restoration circuitry allows a constant black-level across the CRT, regardless of the DC-offset of the incoming video signal.

Connection Diagram

16-Pin P-DIP Package
Top View



5002-1

EL5003C
High Speed CRT Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage at Pin 14	−0.3V to 13.2V
V_{IN} (Logic)	Logic Input at Clamp Gate (Pin 6)	−0.3V to 6V
V_{IN} (Signal)	Signal Inputs (Pins 1, 3, 8)	−0.3V to V_S
V_{CAP}	Voltage at Ch (Pin 16)	−0.3V to V_S + 0.8V
I_{OUT}	Output Current at V_{OUT} (Pin 11)	±36 mA
I_{IN}	Input Current (Pins 1, 3, 6, 8)	±5 mA
I_{CAP}	Current at Ch (Pin 4)	±10 mA
T_J	Operating Junction Temperature	150°C
θ_{JA}	Package Thermal Resistance	56°C/W
T_A	Operating Temperature Range*	−40°C to +85°C
T_{ST}	Storage Temperature	−65°C to +150°C
T_{LD}	Lead Temperature (Soldering < 5 seconds)	300°C

*Note: Do not exceed operating junction temperature of 150°C.

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

See Test Circuit (Figure 1); $T_A = T_J$ = 25°C, $V_{CC} = V_G$ = 12V, V_{CL} = 2V, S1 Open, S2 Open, unless otherwise noted.

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
I_S	Supply Current	V_{CL} = 0.8V	25°C		65	72	I	mA
V_{REF}	Video Input Reference Voltage		25°C	2.5	2.7	2.9	I	V
I_{VID}	Video Input Bias Current	S2 Closed, V_{IN} = 2.7V	25°C	−20	0	20	I	µA
R_{IN}	Video Input Impedance	S2 Closed, V_{IN} = 2.7V to 3.4V	25°C	7	9	11	I	kΩ
V_{CLL}	Clamp Gate Low Input Voltage	Clamp Comparator Off	25°C	0.8			IV	V
V_{CLH}	Clamp Gate High Input Voltage	Clamp Comparator On	25°C			2	IV	V
I_{CLL}	Clamp Gate Low Input Current	V_{CL} = 0.8V	25°C	−20	−10		I	µA
I_{CLH}	Clamp Gate High Input Current	V_{CL} = 2V	25°C	−2	−0.2	2	I	µA
I_{CAP}^+	Clamp Capacitor Charge Current	S1 Closed, V_{CH} = 7V	25°C		−2.5	−1.7	I	mA
I_{CAP}^-	Clamp Capacitor Discharge Current	S1 Closed, V_{CH} = 11V	25°C	1.7	2.5		I	mA

Electrical Characteristics — Contd.

See Test Circuit (Figure 1); $T_A = T_J = 25°C$, $V_{CC} = V_G = 12V$, $V_{CL} = 2V$, S1 Open, S2 Open, unless otherwise noted.

Parameter	Description	Conditions	Temp	Min	Typ	Max	Test Level	Units
I_{LEAK}	Clamp Capacitor Leakage Current	$V_{CL} = 0.8V$	25°C		15	30	I	µA
V_{OUTL}	Video Output Low Voltage	S1 Closed, $V_{CH} = 7V$, $V_{CL} = 0.8V$	25°C		1	1.2	I	V
V_{OUTH}	Video Output High Voltage	S1 Closed, $V_{CH} = 11V$, $V_{CL} = 0.8V$	25°C	9	9.5		I	V
$V_{REF(Comp)}$	Comparator Reference Voltage		25°C	2.1	2.18	2.25	I	mV
A_V max	Video Amplifier Gain	S2 Closed, $V_{CL} = 0.8V$, $V_{IN} = 2.7V$ to 3.4V	25°C	6	7.5	9	I	V/V
ΔA_V 6.85V	Attenuation @ $V_G = 6.85V$	$V_G = 6.85V$ (Note 1)	25°C	−5.5	−6	−6.5	I	dB
ΔA_V 0V	Attenuation @ $V_G = 0V$	$V_G = 0V$ (Note 1)	25°C	−38	−50		I	dB
THD	Video Amplifier Distortion	$V_G = 6.85V$, $V_{CL} = 0.8V$, $V_{OUT} = 1\ V_{PP}$ f = 12 kHz	25°C		0.3		V	%
SSBW	Small-Signal Bandwidth	$V_G = 12V$, $V_{CL} = 0.8V$, $V_{OUT} = 100\ mV_{PP}$	25°C		300		V	MHz
LSBW	Large-Signal Bandwidth	$V_G = 12V$, $V_{CL} = 0.8V$, $V_{OUT} = 4\ V_{PP}$	25°C		300		V	MHz
t_r, t_f	Output Rise Time, Fall Time	$V_{CL} = 0.8V$, $V_{OUT} = 4\ V_{PP}$	25°C		1.5	2	IV	ns

Note 1: S2 Closed, $V_{CL} = 0.8V$, $V_{IN} = 2.7V$ to 3.4V, Referred to $V_G = 12V$ data.

EL5003C Test Circuit

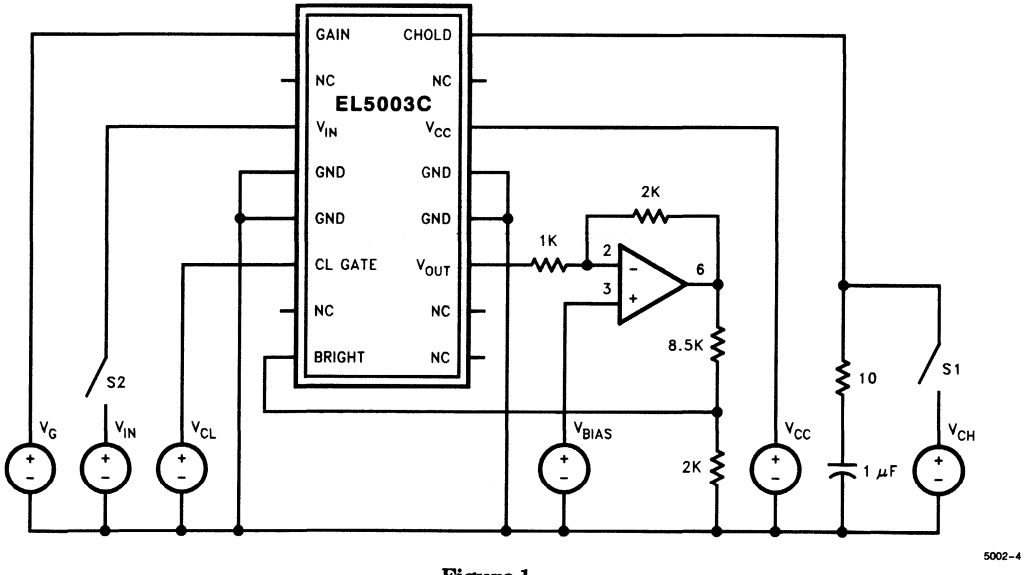
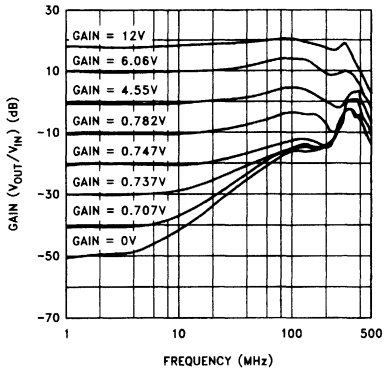


Figure 1

EL5003C
High Speed CRT Amplifier

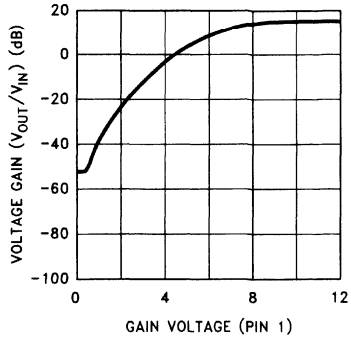
Performance Curves

Voltage Gain vs. Frequency



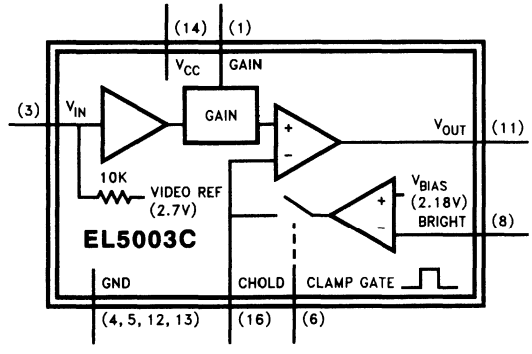
5002-6

Voltage Gain vs. Gain Voltage



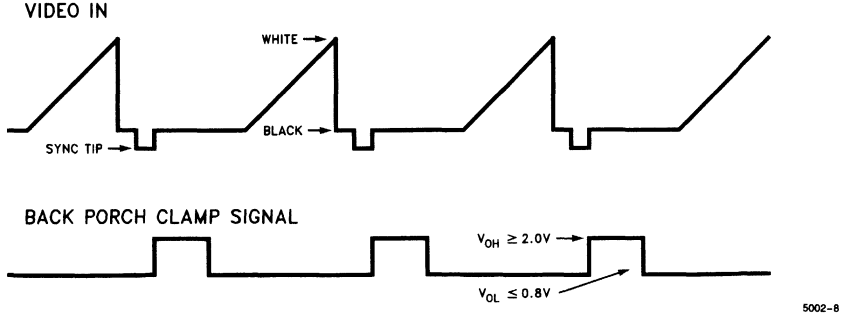
5002-7

EL5003C Block Diagram



5002-3

Figure 2



5002-8

Figure 3

Applications Information

Product Description

As seen in the block diagram (Figure 2), the EL5003C CRT Amplifier consists of an input buffer, a gain control, a post-amplifier, and DC-restore circuitry which combine to allow control of both the contrast (gain) and brightness (offset) of a video signal when driving an external high-voltage stage connected to the cathode of a CRT.

If we describe the EL5003C functionality by first following the video input signal path, we find that an AC-coupled video signal is applied to V_{IN} (Pin 3), which is internally biased to 2.7V through a 10 kΩ resistor. The video signal is then buffered and passes through a variable attenuator which is controlled by the GAIN pin (Pin 1). Attenuation ranges from 0 dB (GAIN pin at 12V) to −50 dB (GAIN pin at 0V), and is used to vary the contrast level of the outgoing video signal. The signal is then amplified by the post-amplifier with a gain of 7.5 V/V, and exits at V_{OUT} (Pin 11). The output stage is self-biasing and does not need an external pull-down resistor for proper operation.

The DC-restore portion of the EL5003C is switchable, and is enabled by placing a TTL- or CMOS-compatible HIGH signal at the CLAMP GATE pin (Pin 6). When enabled, the DC-restore circuitry adds a controlled DC-offset to the EL5003C's internal post-amplifier so that the output of the EL5003C correctly biases the external high-voltage amplifier connected to V_{OUT}. This controlled variation of the EL5003C's output offset voltage is used to vary the brightness of the CRT when the external high-voltage amplifier is DC-coupled to the CRT cathode. If AC-coupling is used in the high-voltage stage, the DC-restore portion of the EL5003C can be used to properly bias the output stage transistors of the external high-voltage stage.

In normal applications, this clamping function is enabled by an external back-porch clamp signal which appears during the black level reference period of the video signal following the horizontal sync pulse (Figure 3). This allows DC-restoration to occur at the beginning of each horizontal scan line.

To accomplish the DC-restoration, the EL5003C requires an external high-voltage output stage with inverting gain. The EL5003C contains an amplifier which compares an internal 2.18V reference voltage with an external feedback voltage provided at the BRIGHT pin (Pin 8). When using a high-voltage output stage which is DC-coupled to the CRT cathode (Figure 4), the external feedback voltage is normally provided by a high-impedance resistor-divider from the final output at the CRT cathode. When using a high-voltage output stage with AC-coupled brightness (Figure 5), the external feedback voltage is normally provided by a high-impedance resistor-divider from the output of the contrast portion of the high-voltage output stage, i.e. before the coupling capacitor. In this case, the brightness control of the EL5003C is used to set the biasing of the output stage transistors, and the DC-restoration occurs with separate external circuitry after the coupling capacitor.

The output of the DC-restore amplifier is used to charge (or discharge) an external 1 μF capacitor located at the CHOLD pin (Pin 16) until the voltage applied to the BRIGHT pin (Pin 8) matches the 2.18V internal bias voltage. For proper operation of the EL5003C, the capacitor should also have a 10Ω resistor placed in series with it. In turn, the voltage held on this capacitor is used to drive the internal circuitry creating the DC-offset required for proper DC-restoration.

The EL5003C is designed for use on +12V (Pin 14) and Ground (Pins 4, 5, 12, and 13). The remaining package pins (2, 7, 9, 10, 15) are not connected internally and should be grounded for best operation.

EL5003C
High Speed CRT Amplifier

Applications Information — Contd.

DC-Coupling vs AC-Coupling in the Output Stage

The EL5003C can easily be used with a high-voltage output stage which is either AC- or DC-coupled to the CRT. DC-coupling is less complex because the EL5003C controls both brightness and contrast, but the DC-coupled signal to the CRT can have about 40V of peak-to-peak contrast voltage on top of about 80V of brightness voltage. These large voltages require external transistors capable of sustaining more than 100V of breakdown.

AC-coupling has advantages in terms of power dissipation and transistor cost. It allows the approximately 40V of peak-to-peak contrast voltage to be created by the output stage, independent of the brightness voltage. This signal would then be AC-coupled to the CRT where the additional brightness voltage would be added. By AC-coupling, the breakdown requirements of the transistors in the high-voltage output stage are reduced from about 100V to about 60V. This reduction in breakdown voltage allows the use of less expensive (or higher performance) transistors, and the power-dissipation in the high-voltage output stage is reduced to about 50% of the DC-coupled application.

The disadvantage of AC-coupling is that the brightness control of the EL5003C will only affect the biasing of the high-voltage output stage, and not the actual brightness voltage applied to the CRT. To correctly set the brightness, an additional DC-restore is required to perform the clamping after the coupling capacitor.

DC-Coupled Monochrome Application

Figure 4 is an example using the EL5003C in a DC-coupled Monochrome application. The 1k pot R1 is used for contrast control, where 12V at the GAIN pin (Pin 1) provides 0 dB of attenuation, and 0V provides 50 dB of attenuation. C1 is used to AC-couple the video signal to the EL5003C. A value of 10 μF is suggested for C1 so that the voltage droop from the EL5003's 8 kΩ input impedance remains acceptably low during each horizontal scan. C2 is charged or discharged by the DC-restore circuitry to offset the output voltage of the EL5003C. A value of 1 μF is suggested for C2 so that the input bias currents of the DC-restore circuitry have a minimal effect on output voltage droop during each horizontal scan. R2 has been added in series with C2 to improve stability of the DC-restore circuitry. A value of 10Ω is suggested for R2. R10 has been included to further reduce the voltage droop during each horizontal scan by adding a bleed current to approximately cancel the bias current of the DC-restoration circuitry. A value of 330 kΩ for R10 provides enough bleed current into C2 to center the droop current about 0 μA over variations in gain and offset. C5 and C6 have been added for supply bypassing of the EL5003C. It is important that C6 be as close as possible to the V_{CC} pin (Pin 14), with C5 nearly as close as C6. Recommended values are 0.1 μF ceramic for C6, and 4.7 μF tantalum for C5.

Looking at the components in the high-voltage output stage, R3 and C3 have been chosen for reasonable biasing and peaking of the gain. R3 has a suggested value of 15Ω, and C3 has a suggested value of 10 pF. R4 and L1 create the proper biasing and peaking at the gain node of the output stage. With R4 = 220Ω and L1 = 0.1 μH, the output stage has a voltage gain of about 10 V/V. Q1 is a Motorola LT1001A NPN transistor used in a common-emitter configuration. It is responsible for setting up the biasing of the entire high-voltage output stage. It has a low breakdown-voltage, so it is cascoded by transistor Q2 which is a Motorola LT1817 NPN transistor. Both Q1 and Q2 may require some series resistance at their base for proper stability of the high-voltage output stage. R5 and R6 provide some degeneration for the output transistors Q3 and Q4. R5 and R6 have values of 10Ω, while Q3 is a Motorola LT5839 PNP transistor and Q4 is a Motorola LT1839 NPN transistor. C4 helps maintain the dynamic performance of the high-voltage output stage over frequency. It has a recommended value of 1000 pF. D1 and D2 are large, slow rectifier diodes with no more than 600 mV of forward bias at 70 mA. D1 and D2 remain predominantly capacitive at high frequencies, and they should be connected with short leads between the bases of Q3 and Q4.

Applications Information — Contd.

R7, R8, and R9 are used to determine the voltage at the CRT after DC-restoration. R8 has a suggested value of 100 kΩ, R9 has a suggested value of 2 kΩ, and R7 is a potentiometer with a suggested value of 3 kΩ. When DC-restoration has been gated on (CLAMP GATE is HIGH) then in steady-state, we know that the voltage at the wiper of the potentiometer R7 will match the internal VBIAS of the EL5003C (2.18V). So, for example, if the wiper is at the top of R7, then there is a 21:1 resistor divider between the cathode of the CRT and Pin 8 of the EL5003C. If Pin 8 is at 2.18V in steady state, then the CRT voltage is at 45.78V. Similarly, if the wiper is at the bottom of R7, then there is a 51.5:1 resistor divider, and the CRT is at 112.27V. This should provide more than enough brightness range for most applications.

For this example, the high-voltage supply has been chosen at 120V under the assumption that the G1 connection of the CRT is grounded. However, for most modern high speed monochrome applications, G1 is either driven differentially with respect to the CRT cathode, or biased below ground to allow a lower final supply voltage.

AC-Coupled Monochrome Application

Figure 5 shows an example of an AC-coupled monochrome application. The basic circuit is very similar to the DC-coupled application of Figure 4, with the addition of an AC-coupling capacitor C8 and a relatively simple secondary DC-restore circuit at the high-voltage stage output. In addition, the 120V power supply of Figure 4 has been reduced to 60V, and another 120V supply has been added after the coupling capacitor. The value of the divider resistor R8 has also changed from 100 kΩ to 51 kΩ due to the reduction in supply voltage.

The external DC-restore circuitry has the advantage of being quite simple, but has the disadvantage of clamping on the most positive voltage of the outgoing signal (which is the most negative voltage of the incoming signal). In most applications, this corresponds to the sync-tip voltage rather than the black-reference voltage. In practice, these voltages are usually well correlated, so DC-restoration to the sync-tip is not generally an issue.

Just as in the DC-coupled application above, this example assumes that G1 of the CRT is grounded. In most modern high speed monochrome circuits, G1 is either driven differentially with respect to the CRT cathode, or biased below ground to allow a lower supply voltage for the high-voltage stage.

AC-Coupled Color Application

The color application of Figure 6 is based on the monochrome application of Figure 5. The 3 channels are each identical to the monochrome application, except for gain and contrast control. In this application, contrast is varied with a main contrast potentiometer, while each channel has an additional potentiometer for contrast trim. Similarly, there is a main brightness potentiometer, and an additional brightness trim potentiometer for each channel.

Power Dissipation

The EL5003C has been packaged in a 16-Pin PDIP with a special leadframe for improved power dissipation. This package allows almost twice the power dissipation of a regular package by connecting the internal die-attach area directly to pins 4, 5, 12, and 13 (the GND connection of the EL5003C). Heat is conducted via these 4 leads, out of the package, and into the PC-board. It is therefore highly recommended that a socket not be used, and that as much ground plane as possible be connected to the GND pins.

Under the conditions listed above, the package thermal resistance is 56°C/W. At a maximum supply current of 72 mA, and an absolute maximum supply voltage of 13.2V, worst-case quiescent power dissipation is:

$$PD(Quiescent) = 13.2V \times 72\ mA = 950\ mW.$$

If we assume 15 pF of load capacitance and that the output is slewing at (0.8 × 4V) ÷ 1.5 ns, we get a slew-rate of 2.13 V/ns and a slewing current of 32 mA. If we assume that the output is slewing half of the time, we get an additional worst-case power dissipation of:

$$PD(Active) = 0.5 \times 13.2V \times 32\ mA = 211\ mW.$$

EL5003C
High Speed CRT Amplifier

Applications Information — Contd.

The total power dissipation is then:

PD(Total) = 950 mW + 211 mW = 1.16W.

The maximum die temperature is then:

T_{MAX}(die) = T_{MAX}(ambient) + (1.16W) × (56°C/W) = 140°C.

Even under this worst-case scenario, the die temperature remains below the absolute rating of 150°C.

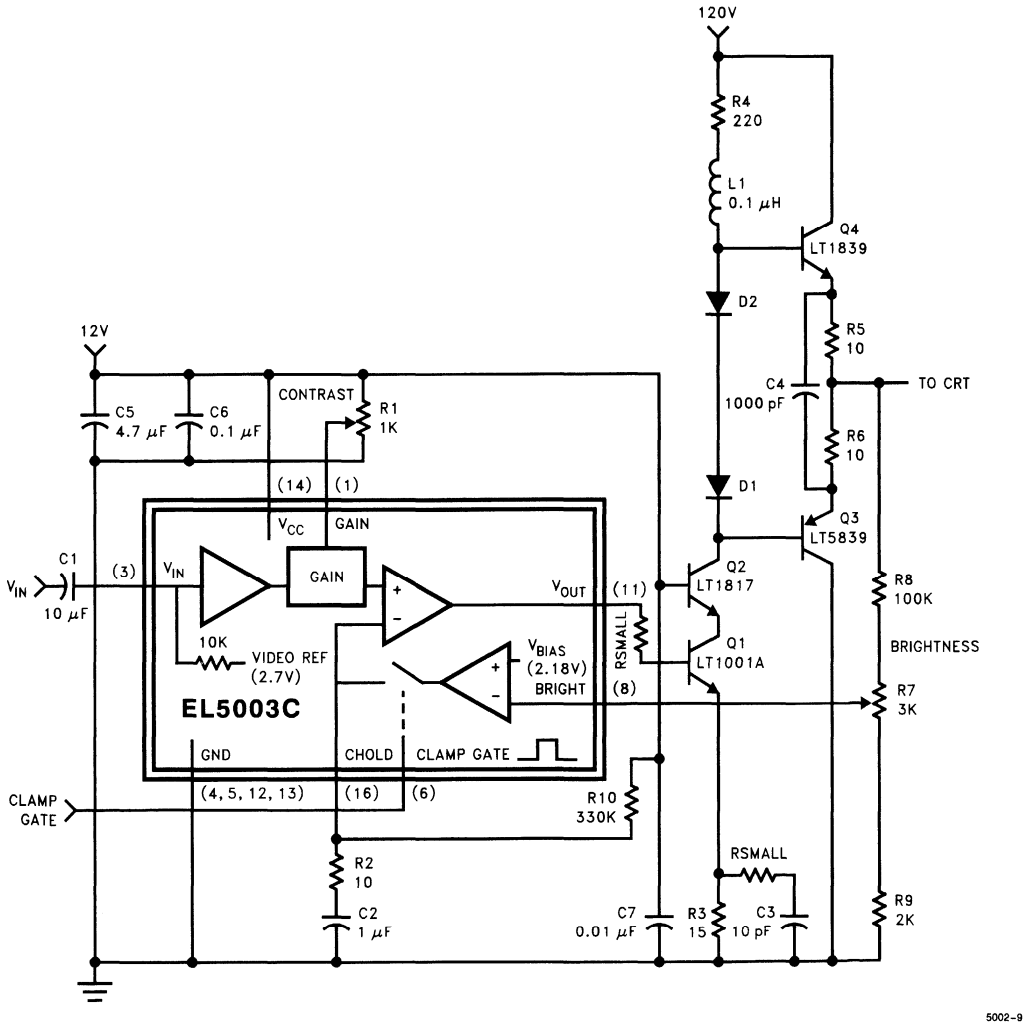


Figure 4. Monochrome Application Example HV-Stage DC-Coupled to CRT Cathode

Applications Information — Contd.

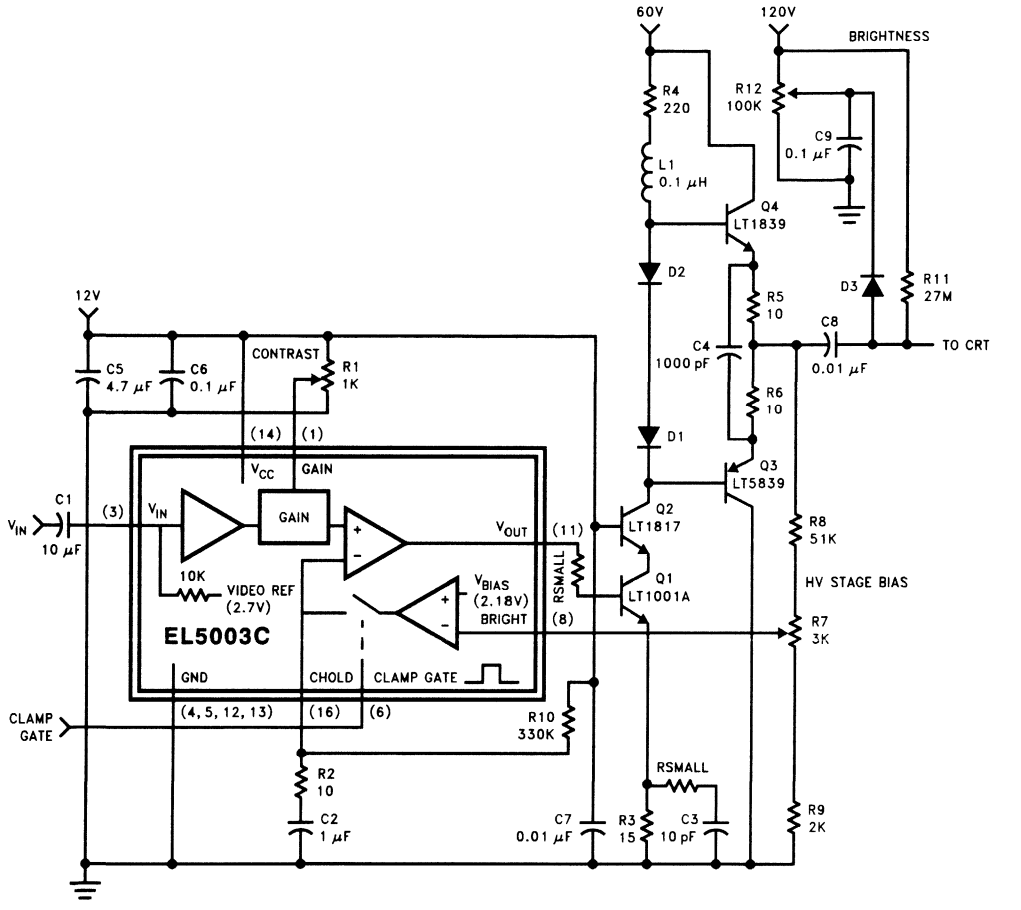


Figure 5. Monochrome Application Example
HV-Stage AC-Coupled to CRT Cathode

EL5003C
High Speed CRT Amplifier

Applications Information — Contd.

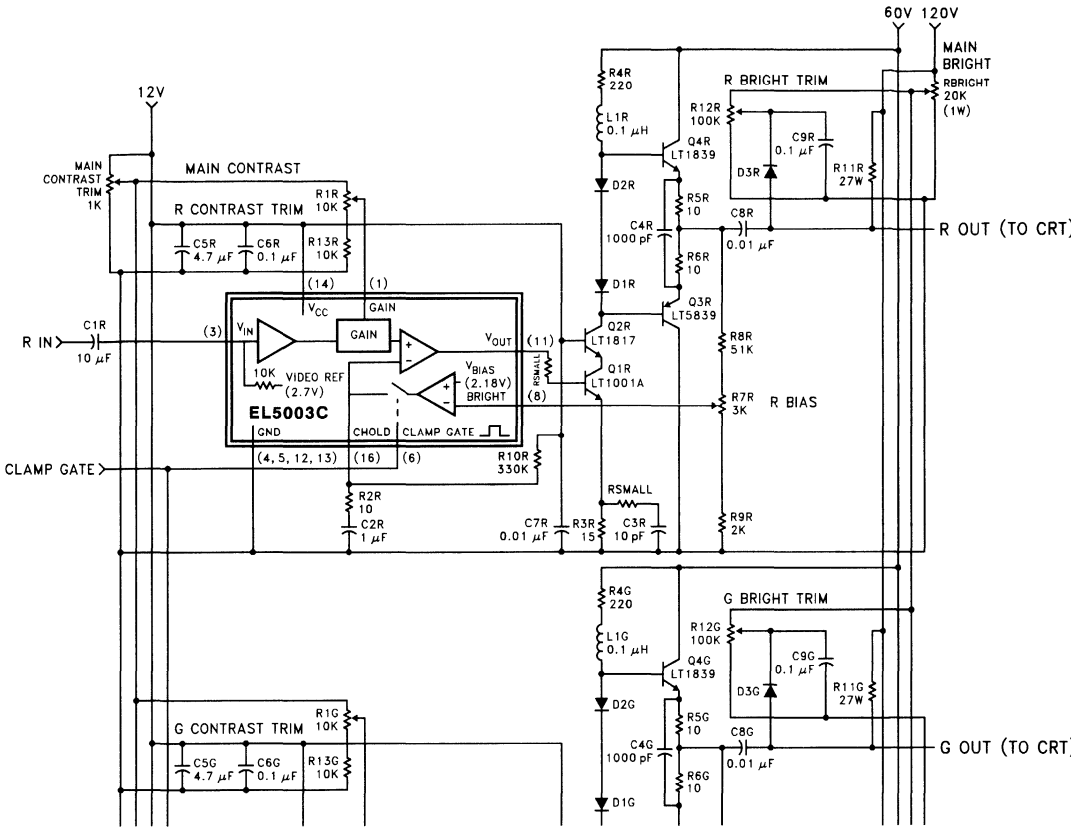
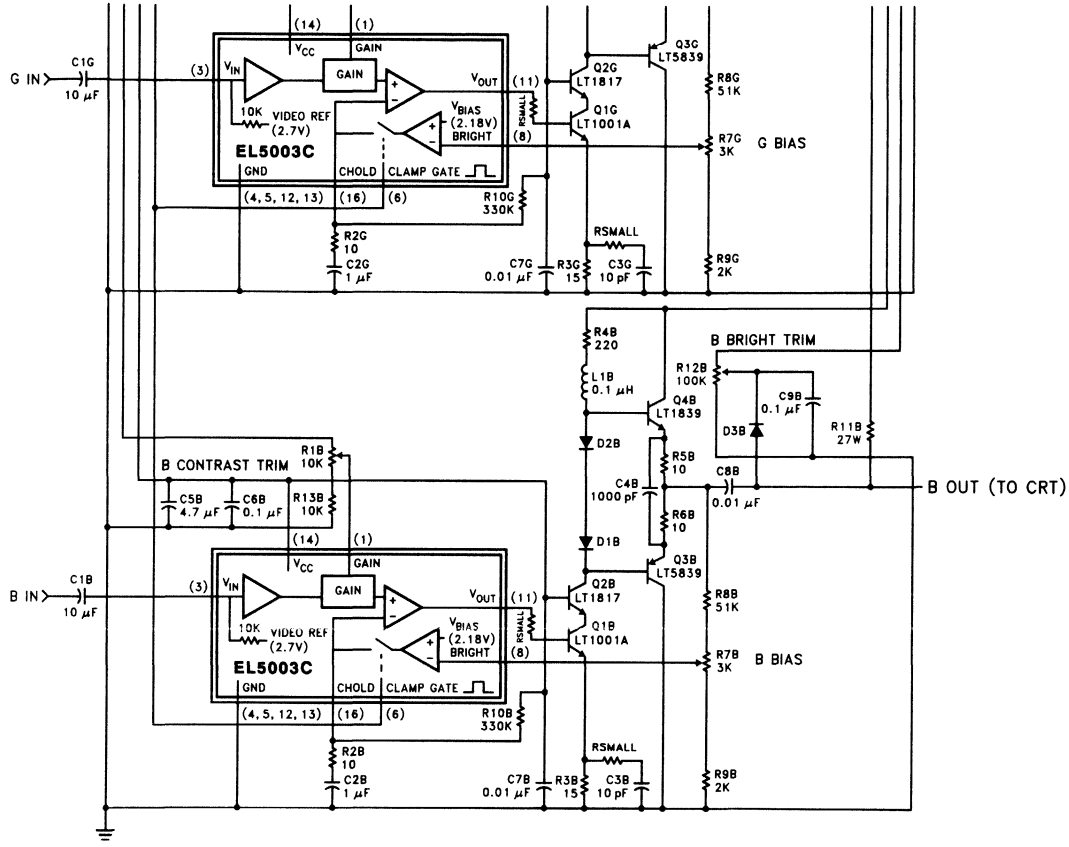


Figure 6. Color Application Example: HV-Stage AC-Coupled to CRT Cathode

Applications Information — Contd.



5002-12

Figure 6. Color Application Example: HV-Stage AC-Coupled to CRT Cathode — Contd.

Application Specific A.T.E.

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELANTEC Part Number	Description	Features	V_O		I_O Min	Slew Rate		Max I_S	Max Standby I_S	Package
			Min	Max		Min	Max			
EL2021C	Monolithic Pin Driver for ATE Applications	Tristate Output Programmable Slew Rate, Short Circuit Current Sense	−6.1V to 10.9V	−5.9V to 11.1V	±500 mA	80 V/μs to 120 V/μs	150 V/μs to 360 V/μs	45 mA	2.5 mA	18-Pin CerDIP
EL1056C EL1056AC	Monolithic High-Speed Pin Driver	Adjustable Slew Rate, Wide Voltage Range, Power Down	±0.2V	±12V	±50 mA DC ±150 mA AC	0.1 V/ns	1.2 V/ns	60 mA	25 mA	24-Lead Thermal SOL

Part Number	Description	A_{VOL} (typ)	V_{OS} (max)	I_B (max)	I_S (max)	V_{HYS}	T_{PD} (typ)	Package
EL2252C	50 MHz Dual Comparator TTL Output	8000 V/V	10 mV	17 μA	+19, −20 mA both Comparators	60 mV_{PP}	6 ns	14-Pin P-DIP 20-Pin SOL

EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

Features

- Wide ±12V output levels
- 250 ps dispersion
- 3 ns delay times
- 1V/ns slew rate—adjustable
- Low overshoot and aberrations in 50Ω systems
- 3-state output
- Power-down mode reduces output leakage to nanoamperes
- Overcurrent sense flag available to protect internal output devices
- Buffered analog inputs
- Differential logic inputs are compatible with ECL, TTL, and CMOS

Applications

- Memory testers
- ASIC testers
- Functional board testers
- Analog/digital incoming component verifiers
- Logic emulators

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL1056CM	0°C to +75°C	24-Lead Thermal SOL	MDP0027
EL1056ACM	0°C to +75°C	24-Lead Thermal SOL	MDP0027

General Description

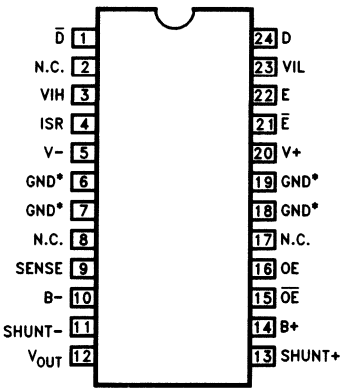
The EL1056 is designed to drive high-quality test signals into close or terminated loads. It has a dispersion of 250 ps or less — whether due to signal size or direction of edge. It can output a very wide 24V output span, encompassing all logic families as well as analog levels. The EL1056 is fabricated in Elantec's oxide isolated process, which eliminates the possibility of latch-up and provides a very durable circuit.

The output can be turned off in two ways; the OE pins allow the output to be put in a high-impedance state which makes the output look like a large resistance in parallel with 3 pF, even for back-driven signals with as much as 2.5V/μs slew rate. The E pins put the output in an even higher impedance state, guaranteed to 150 nA leakage in the EL1056A. This allows accurate measurements on the bus without disconnecting the EL1056 with a relay.

The EL1056 incorporates an output current sense which can warn the system controller that excessive output current is flowing. The trip point is set by two external resistors.

Connection Diagram

24-Lead Thermal SOL Package



*and Heat-spreader

1056-1

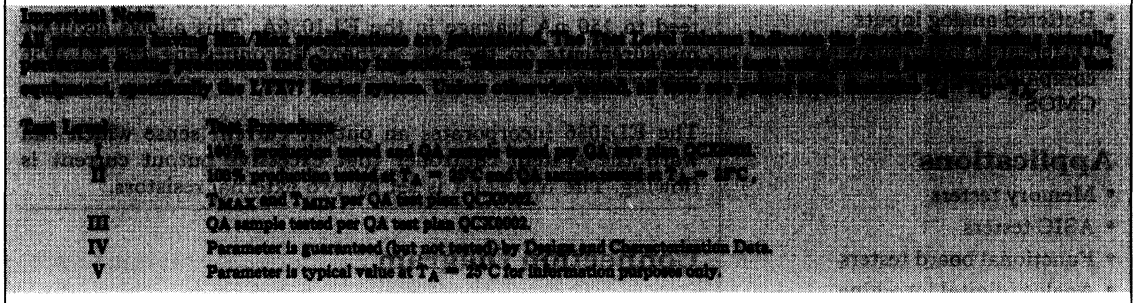
Top View

5

EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

Absolute Maximum Ratings (T_A = 25°C)

V_S	Voltage between V+ and V−	+33V
V−	Supply Voltage	−18V
B+	Supply Voltage	V_{INH} to V+
B−	Supply Voltage	V− to V_{INL}
I_{SR}	Input Current	0 mA to 3 mA
V_{SR}	Input Voltage, Power-Down Mode	−0.3V to +6V
Shunt+	Input Voltage	(B+) −5V to B+
Shunt−	Input Voltage	B− to (B−) +5V
Data, $\overline{Data}$	Input Voltages	V− to V+ or ±6V Differential
OE, $\overline{OE}$	Input Voltages	V− to V+ or ±6V Differential
E, $\overline{E}$	Input Voltages	V− to V+ or ±6V Differential
Sense	Output Voltage	V− to V+
V_{INH}	Input Voltage	V_{INL} −0.3V to B+
V_{INL}	Input Voltage	B− to V_{INH} +0.3V
I_{OUT}	Output Current	−60 mA to +60 mA
T_J	Junction Temperature	150°C
T_A	Operating Ambient Temperature Range	−0°C to +75°C
T_{ST}	Storage Temperature	−65°C to +150°C
P_D	Power Dissipation (T_A = 25°C) (See Curves)	3.1W



Test Level
I
II
III
IV
V

Test Procedure
100% production tested and QA sample tested per QA test plan QCX0002.
100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
QA sample tested per QA test plan QCX0002.
Parameter is guaranteed (but not tested) by Design and Characterization Data.
Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

T_A = 25°C, V+ = B+ = 15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω, no load. Data, E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. V_{INH} = 5V, V_{INL} = −1.6V

Parameter	Description	Min	Typ	Max	Test Level	Units
I_S	(V+) + (B+), (V−) + (B−) Supply Currents		52	60	I	mA
I_S, dis	(V+) + (B+), (V−) + (B−) Supply Currents, Disabled		17	25	I	mA
I_{VINH}		−20	−3	20	I	μA
I_{VINL}		−20	2	20	I	μA
I_{DATA}		−30	−15	30	I	μA
I_{OE}	OE Input Current	−30	−14	30	I	μA
I_E	E Input Current	−20	7	20	I	μA
V_{SR}	Voltage at I_{SR} Pin	0	20	40	I	mV
I_{SHUNT+}, I_{SHUNT-}			4	7	I	mA
V_{SHUNT+}, V_{SHUNT-}	Sense Threshold at Shunts	160	200	250	I	mV
I_{SENSE}	Sense Output Currents	1	1.5	2	I	mA
V_{OS}	Output Offset, Data High, V_{INH} = 0V, V_{INL} = −1.6V	−50		50	I	mV
	Data Low, V_{INL} = 0V, V_{INH} = 5V	−100		100	I	mV

DC Electrical Characteristics — Contd.

T_A = 25°C, V+ = B+ = 15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω, no load. Data, E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. V_{INH} = 5V, V_{INL} = −1.6V

Parameter	Description	Min	Typ	Max	Test Level	Units
Eg	Gain Error Data High, V_{INH} from 0V to 5V, V_{INL} = −1.6V, No Load	−1.5	−0.6	0	I	%
	Data Low, V_{INH} = 5V, V_{INL} from −5V to 0V, No Load	−1.5	−0.6	0	I	%
NL	Gain Nonlinearity Data High, V_{INH} from 0V to 10V, V_{INL} = −1.6V, No Load		0.04		V	%
	Data Low, V_{INH} = 5V, V_{INL} from −10V to 0V, No Load		0.06		V	%
PSRR	Power Supply Rejection Ratio of V_{OUT} with Respect to B+, B−, Shunt+, or Shunt− Potential		2.2		V	mV/V
R_o, en	Output Resistance, Enabled, Il = ±20 mA	4.5	6	7.5	I	Ω
R_o, dis	Output Resistance, Output Disabled, V_O = −1.6V to −5V, EL1056C	20K	100K		I	Ω
	EL1056AC	100K	200K			
I_o, dis	Output Current, Output, Disabled, V_O = 0V	−20	5	20	I	μA
I_o, off	Output Leakage, E Low, (Shut-Down), V_O = 0V, EL1056C	−20		20	I	μA
	EL1056AC	−150		150	I	nA

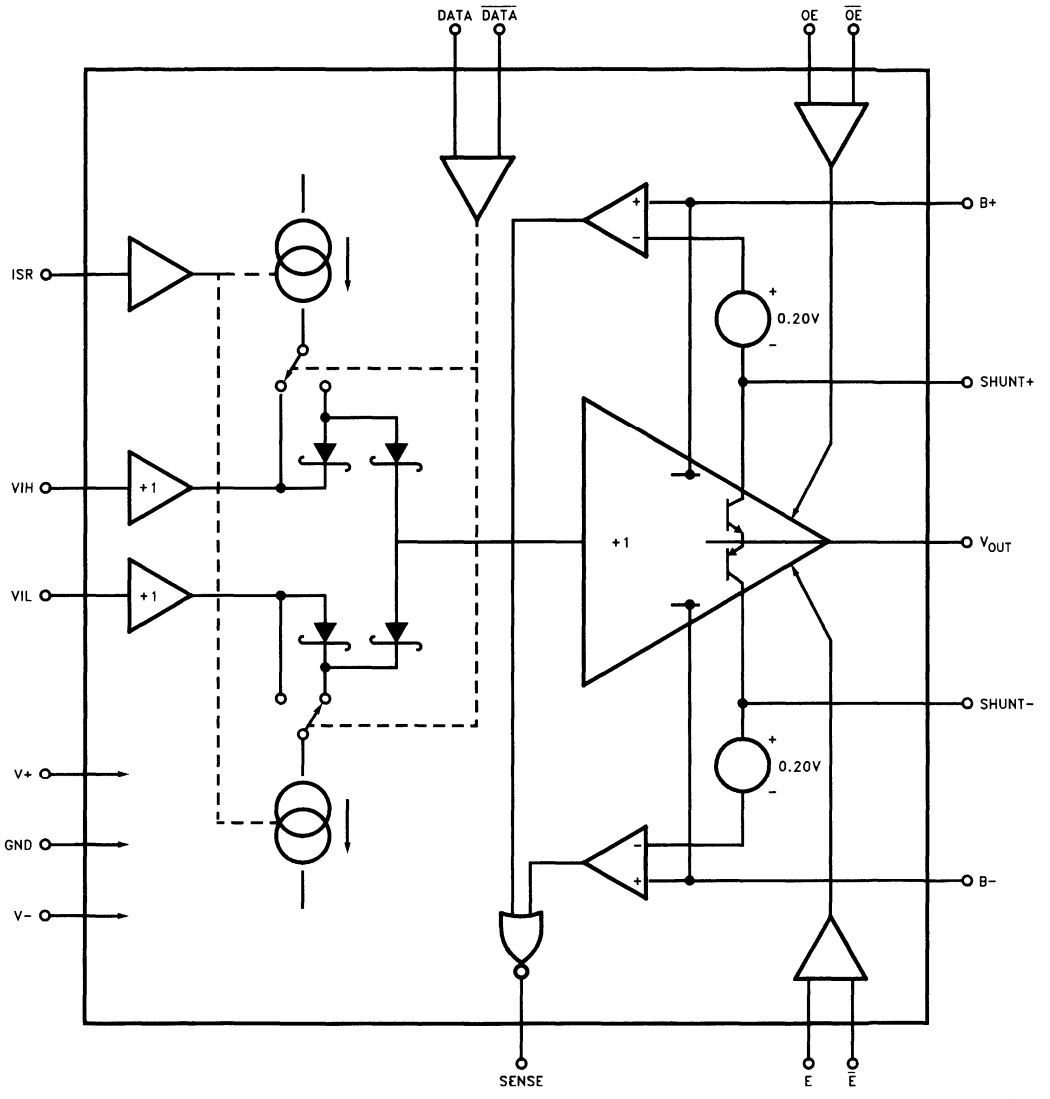
AC Electrical Characteristics

T_A = 25°C, V+ = B+ = +15V, V− = B− = −10V, R_{SHUNT+} = R_{SHUNT-} = 6.5Ω. R_L = 500Ω. 50Ω + 22 pF snubber included at output. Data E, and OE from −1.6V to −0.8V. I_{SR} = 800 μA. ECL swing is defined by V_{INH} = −0.8V and V_{INL} = −1.6V, CMOS swing defined by V_{INH} = 5V and V_{INL} = 0V. Propagation delay is measured at 0.4V movement of output.

Parameter	Description	Min	Typ	Max	Test Level	Units
T_{PD}	Propagation Delay, CMOS Swing	1.0	3.0	4.5	I	ns
Dis	Propagation Delay Dispersion					
	Due to Output Edge Direction		250	450	I	ps
	From ECL to CMOS Swings		250	450	I	ps
	Due to Repetition Rate		80		V	ps
SR	Output Slew Rate, CMOS Swing, 20%–80%	0.8	1	1.2	I	V/ns
SR_{sym}	Slew Rate Symmetry		3	10	I	%
TR	Output Rise Time, ECL Swing, 20%–80%		2.2		V	ns
OS	Output Overshoot					
	CMOS Swing		190	500	I	mV
	ECL Swing (I_{SR} = 350 μA)		65		V	mV
T_{dis}	Output Disable Delay Time		4.7	6.5	I	ns
T_{en}	Output Enable Delay Time		6.0	8.5	I	ns
C_o, dis	Output Capacitance in Disable		3		V	pF
T_{off}	Power-Down Delay Time		0.5		V	μs
T_{on}	Power-On Delay Time		90		V	ns
C_o, off	Output Capacitance in Power-Down		50		V	pF
T_{sense}	Comparator Delay Time — Switching ON		1.5		V	μs
	Switching Off		0.4		V	μs

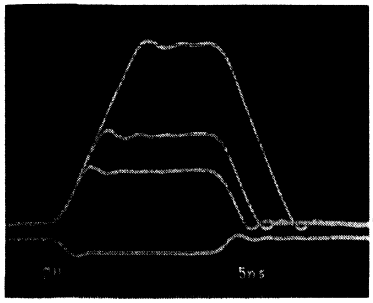
EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

Block Diagram



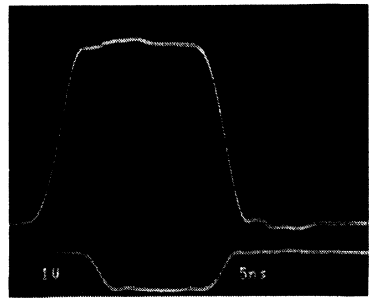
Typical Performance Curves

10V, CMOS, TTL, and ECL Outputs into 550Ω Load



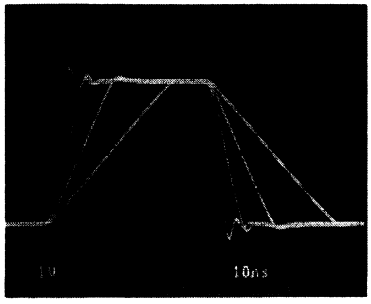
1056-6

CMOS and ECL Outputs As Seen at the End of an Unterminated Cable, Backmatched at Driver



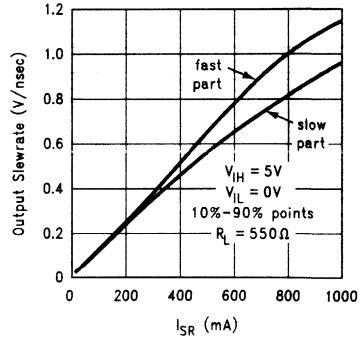
1056-7

CMOS Output at I_{SR} = 100 μA, 200 μA, 400 μA, and 1000 μA



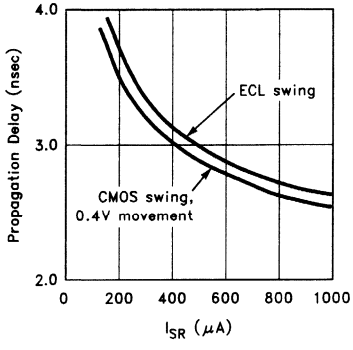
1056-8

Output Slewrate vs I_{SR} (Two Samples)



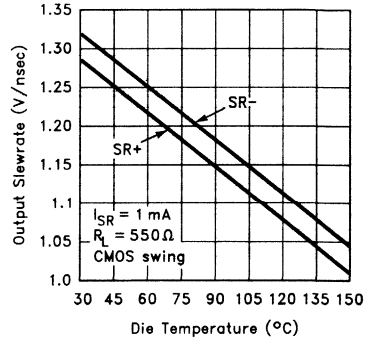
1056-9

Propagation Delay vs I_{SR}



1056-10

Output Slewrate vs Die Temperature

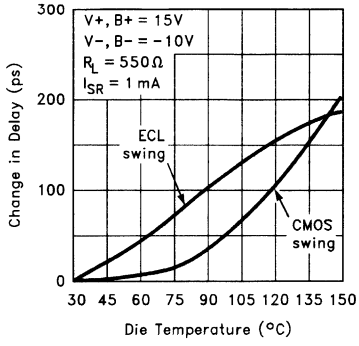


1056-11

EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

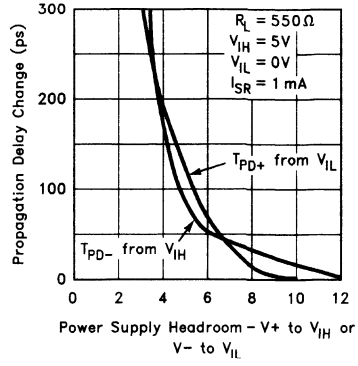
Typical Performance Curves — Contd.

Propagation Delay Change with Die Temperature



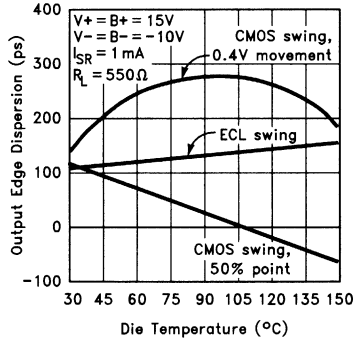
1056-12

Change in Propagation Delay with Power Supply Headroom



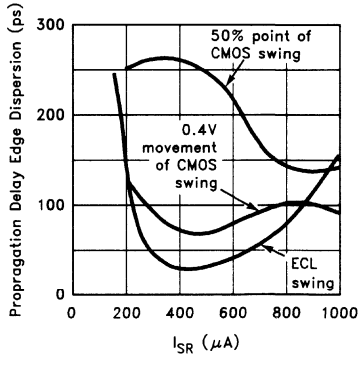
1056-13

Output Edge Dispersion vs Temperature



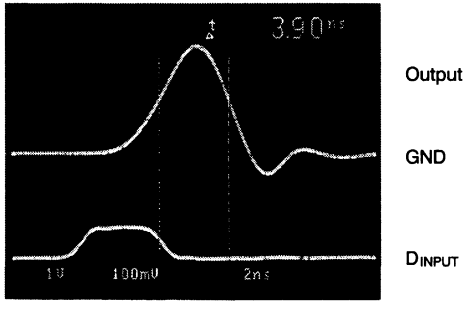
1056-14

Edge Dispersion vs I_{SR}



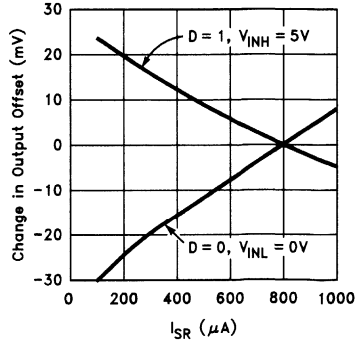
1056-15

Minimum Output Pulse Width



1056-16

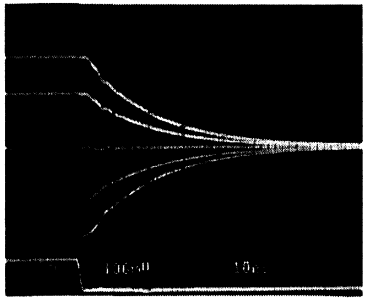
Output Offset vs I_{SR}



1056-17

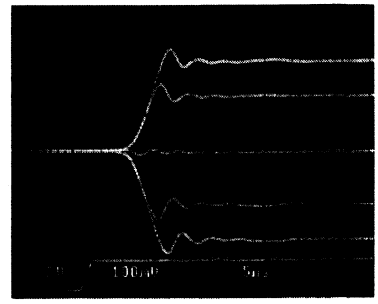
Typical Performance Curves — Contd.

Tristate Turn-off Waveforms



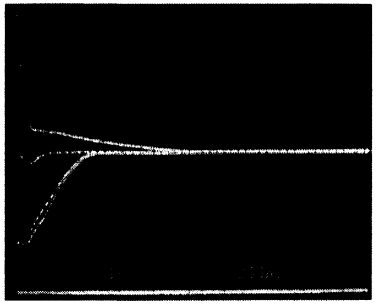
1056-18

Tristate Turn-on Waveforms



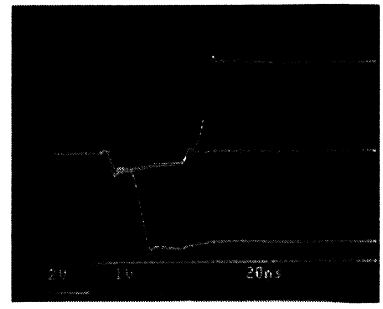
1056-19

Power-Down Disable Waveforms



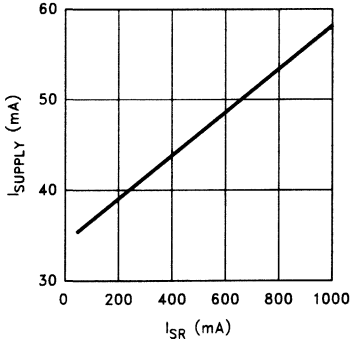
1056-20

Power-Down Enable Waveforms



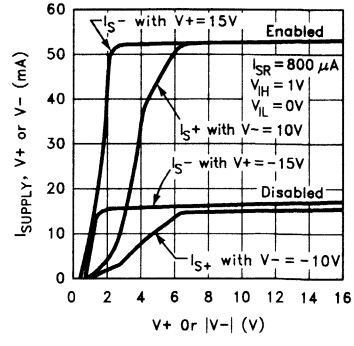
1056-21

Supply Current vs I_{SR}



1056-22

Total Supply Current vs Supply Voltage

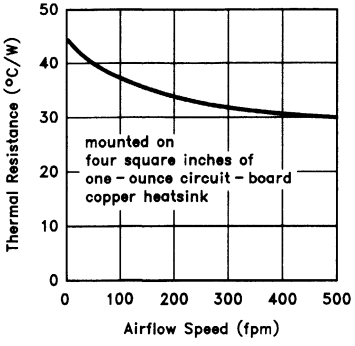


1056-23

EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

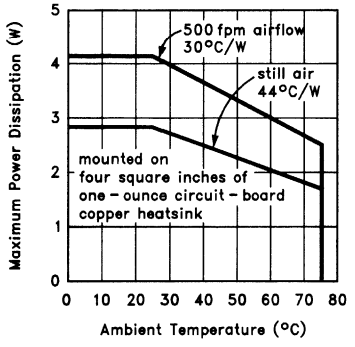
Typical Performance Curves — Contd.

Mounted Thermal Resistance of Package vs Airflow Speed



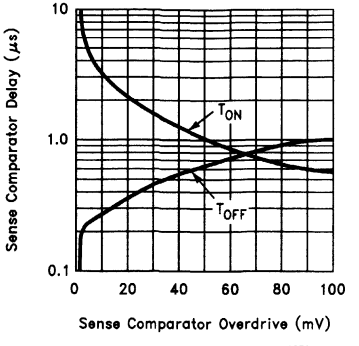
1056-24

Package Power Dissipation vs Ambient Temperature



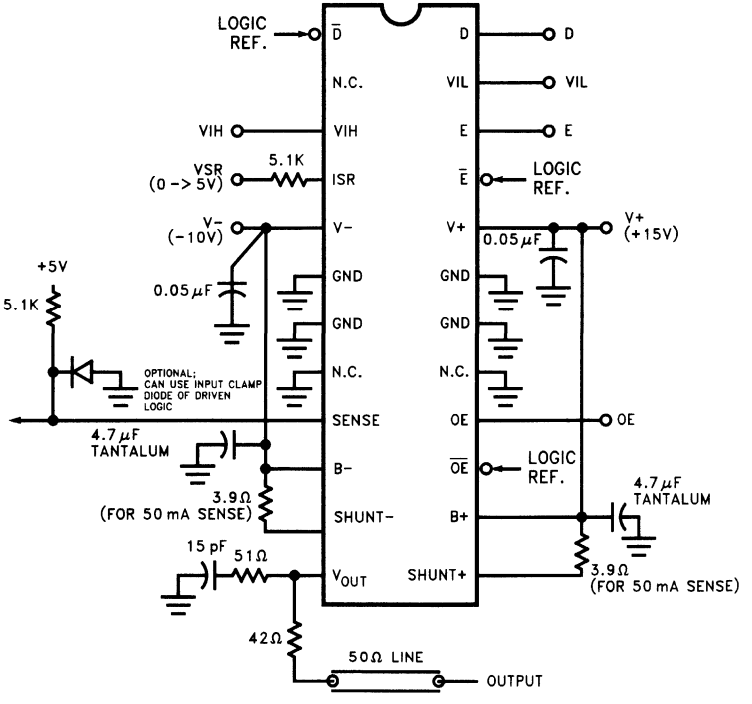
1056-25

Sense Comparator Delay vs Overdrive



1056-26

EL1056 Used in CMOS and TTL Systems



1056-4

Applications Information

Functional Description

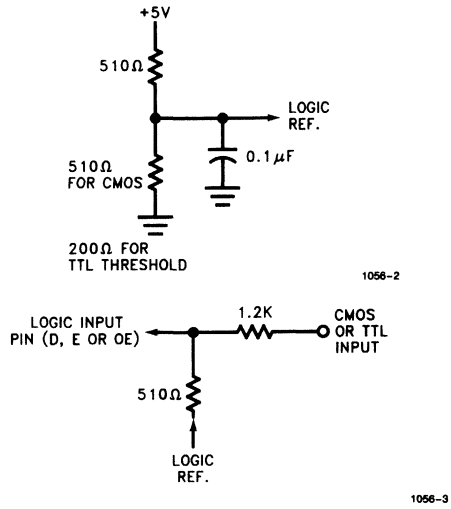
The EL1056 is a fully integrated pin driver for automatic test systems. Pin drivers are essentially pulse generators whose high and low levels can be externally programmed and accurately switched in time, as well as incorporating an output switch to disconnect the driver from a measurement bus. Additionally, the EL1056 has programmable slewrate.

Control Voltage Inputs

The analog level inputs are named V_{INH} and V_{INL}, and the output replicates them as controlled by logic inputs. The analog inputs are buffered and have bandwidths of 35 MHz and slewrates of 25V/μs. For full slewrate, 4V of headroom should be given to the inputs, that is V_{INH} should be 4V less than V+ or B+, and V_{INL} should be 4V more positive than V− or B−. At lower slewrates (I_{SR} = 500 μA or less), 3V of headroom will suffice. Insufficient headroom causes distorted output waveforms or delay errors in output transitions. V_{INH} may be lower in voltage than V_{INL}, but the output will not follow the control logic correctly. Furthermore, V_{INH} should be 200 mV more positive than V_{INL} (the minimum output amplitude) for accurate switching.

Logic Inputs

The logic inputs are all differential types, with both NPN and PNP transistors connected to each terminal. They are optimized for differential ECL drive, which optimizes + to − edge delay time matching. Larger logic levels can introduce feedthrough glitches into the output waveform. For CMOS input logic levels, an ECL output waveform will show feedthrough when the input risetime is shorter than 8 ns, differential or single-ended. CMOS output swings show less aberration, and the EL1056 can tolerate a 4 ns single-ended risetime or 2 ns risetime for differential inputs. Attenuating CMOS or TTL inputs to 1 Vp-p will eliminate all logic feedthrough as shown in Figure 1.



Alternate Logic Interface
Figure 1

Slewrate Control

The slewrate is controlled by the I_{SR} input. This is a current input and scales the output slewrate by a nominal 1.25V/ns/mA. The slewrate maintains calibration and symmetry to at least as slow as 0.2V/ns. The practical upper end of I_{SR} is 1 mA, and supply current increases with increasing I_{SR}.

The I_{SR} control can be used to adjust individual pin drivers to a system standard, by adjusting the value of its series resistor. Slewrate can also be slowed to reduce output ringing and crosstalk.

With ECL output swings, there is not enough voltage excursion to incur slewrate delays to 50% logic threshold. The risetime, delays, and dispersions do not degrade with reasonably reduced I_{SR}, and overshoot will reduce markedly. An I_{SR} of 350 μA produces a very good ECL output, and driver dissipation is also reduced.

EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

Applications Information — Contd.

The I_{SR} pin is connected to the emitter of a PNP transistor whose base is biased a diode below ground (see Figure 2). Thus, the I_{SR} input looks like a low impedance for positive input currents, and is biased close to ground. A protection diode absorbs negative currents, and the input PNP will not conduct. In power-down mode, the PNP releases its current sink and the external circuit must not present more than 6V to the disabled I_{SR} input, or emitter-base damage to the NPN will occur within the driver. A signal diode or zener can be used to clamp the I_{SR} input for positive input voltages if the voltage on the I_{SR} resistor is potentially greater than 6V when the driver is in power-down mode.

Output Stage–Tristate Mode

In tristate mode (OE low) the output transistors have their emitter-base junctions reverse-biased by a diode voltage. This turn-off voltage is in fact provided by an internal buffer whose input is connected to the output pin (see Figure 3). Transistors Q1–Q4 form the output buffer in normal mode. The tristate mode buffer Q5–Q8 replicates externally impressed voltages from the output pin onto the internal schottky switch node. They also turn off Q1–Q4 by a reverse diode voltage between bases and emitters, effectively bootstrapping the internal voltages, so that no transistor's base-emitter junction is reverse-biased by a damaging potential. Another benefit is that the capacitance seen at the output in tristate mode is reduced.

Because the tristate buffer's input is connected to the output terminal, the output is quite "alive" during tristate. For instance, the input bias current of the buffer is seen as the tristate "leakage", and its variation with applied voltage becomes tristate input impedance.

The tristate input current is like a current source, and it can drag an output to unpredictable voltages. It is not a danger to connect a tristated output that has drifted to, say, −6V to a logic pin of a device to be tested. The tristate output current will simply comply with whatever voltage the connected part normally establishes.

The tristate input impedance is also quite active over frequency. The output can oscillate when presented with resonant or inductive impedances. To prevent this, a snubber should be connected from output to ground, consisting of a resistor in series with a small capacitor. The snubber can also reduce the reflections of the coaxial line when driven from the far end, since the line appears to have an open termination during tristate. Typical values for the resistor are 50Ω to 75Ω, and 12 pF to 22 pF for the series capacitor. The effect of the snubber is to "de-Q" resonances at the output.

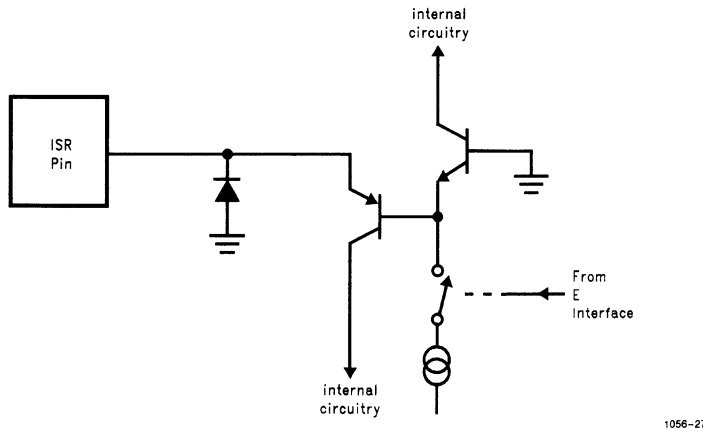


Figure 2. I_{SR} Pin Circuitry

Applications Information — Contd.

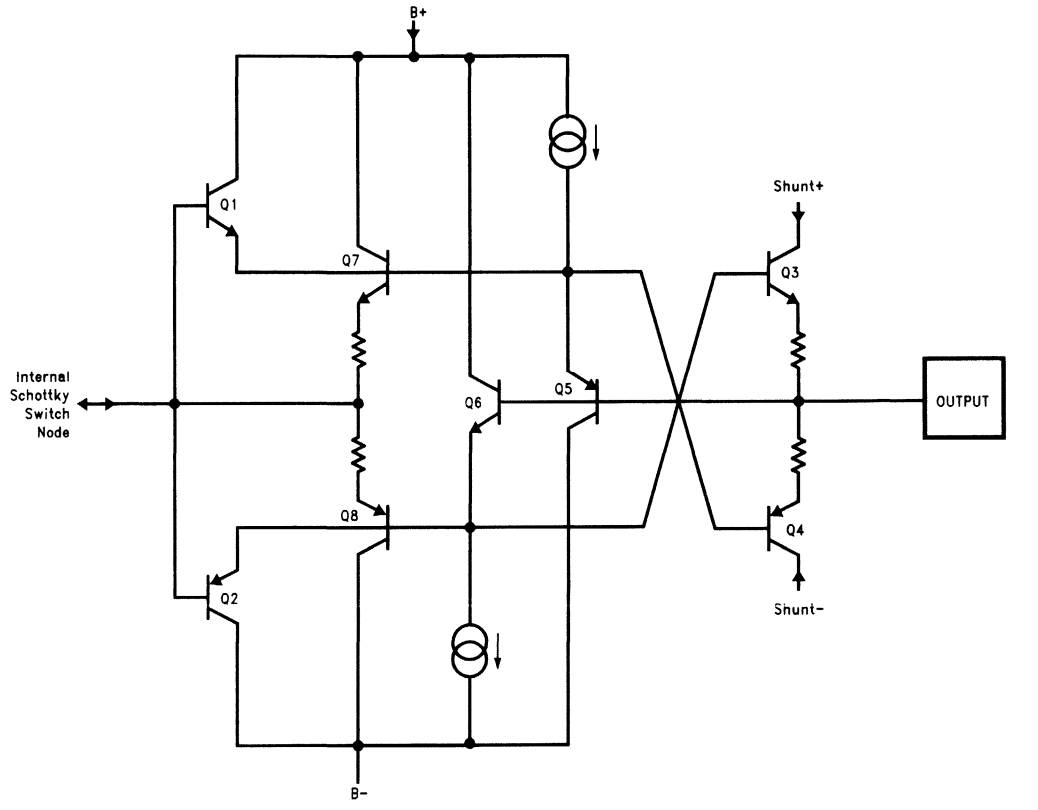


Figure 3. Output Stage Circuit in Tristate Mode

Output Stage–Normal Mode

Capacitive loads can cause the output stage to ring. Little ringing occurs for loads less than 25 pF, but substantial ringing for more than 40 pF. Terminated transmission lines cause no ringing, and actually suppress it as a snubber does. A terminated line draws heavy DC current, however, and greatly raises dissipation.

Driving a back-terminated line also causes little ringing and does not cause DC dissipation. The series matching resistor between the EL1056 output and a back-terminated line also serves to isolate the driver from capacitive loads and short-circuits. The slewrate of the driver slows by about 10% when driving a 50Ω back-matched line, as seen at the end of the line. The snubber can be on either side of the back-match resistor. When placed on the line side it creates a high-frequency termination for the line when the driver is tristated, but it slows the output small-signal risetime by about 10% (although not slewrate). When placed on the driver side of the back-match resistor, no speed reduction occurs in normal mode but the cable is more poorly terminated in tristate.

The transient currents that occur when driving capacitive or back-matched loads can be very high, approaching 100 mA. The driver is capable of outputting a peak of 140 mA, but long-term

Applications Information — Contd.

load currents must be limited to 60 mA. Short-circuits can rapidly destroy the EL1056, although the part will survive for 20 ms periods. If there is the possibility of output load fault the overcurrent sense circuitry should be used to signal alarm to the controlling system, which should ultimately activate the tristate mode to relieve the output stage. Driving large static currents also raises internal dissipation and should be part of the thermal budget.

The collectors of the output transistors are connected to the Shunt terminals, and the output stage drivers' collectors are connected to the B+ and B− terminals (see Figure 4). The Shunt lines can have transient currents as high as 120 mA and are separated from the V+ and V− terminals to keep switching noise out of the control and logic circuitry. A bypass capacitor should be connected to the B+ and B− terminals.

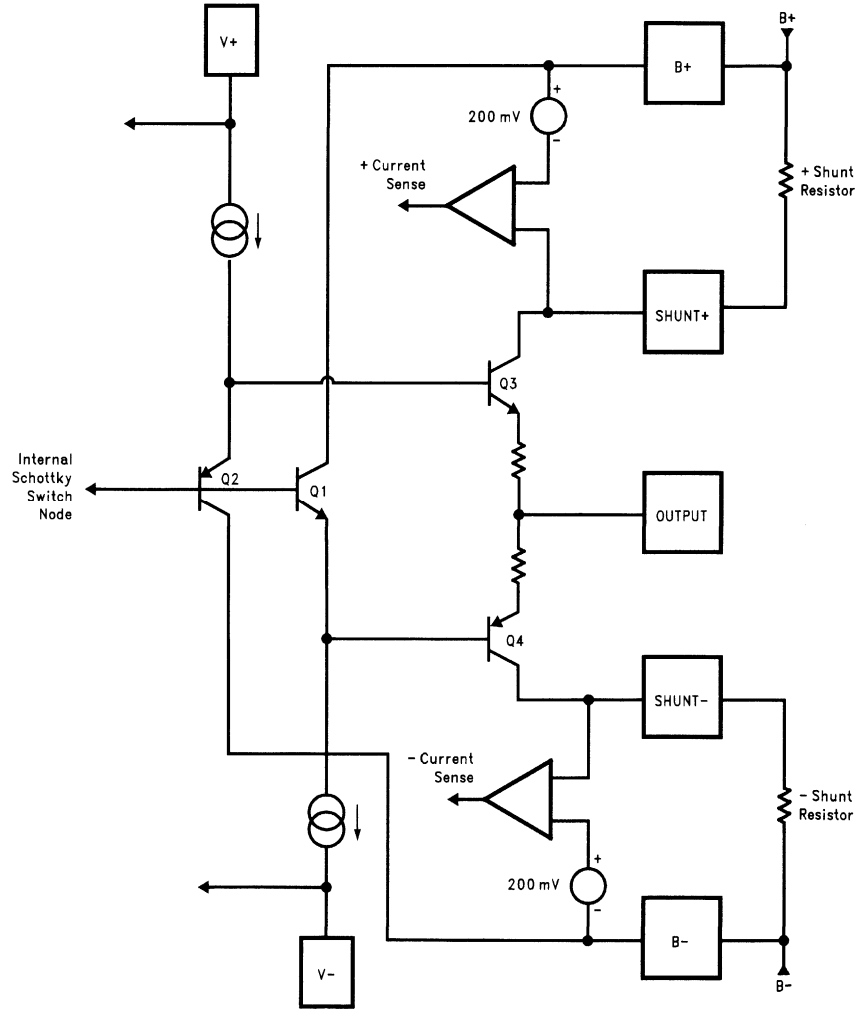


Figure 4. Output Stage in Normal Mode

Applications Information — Contd.

Overcurrent Protection

The sense comparators are available to alert the test system's controller that the driver is outputting excessive current. Shunt resistors are connected from B+ to Shunt+ and B− to Shunt−. When the internal comparators sense more than a nominal 200 mV drop on the shunts, they cause a 1.5 mA current to be sunk from the Sense terminal. The comparators are of "slow attack, fast decay" design, so that transient load currents will not trigger a sense output; only a sustained overcurrent will.

The sense resistors must not be inductive, and the skin resistance of long, narrow connections between Shunt and B+ or B− can cause transient voltages that produce output overshoot (but not ringing).

The Sense output is simply a switched current source connected to V−. It can be used to interface to CMOS, TTL, or ECL inputs. For CMOS and TTL, it can be connected to a pull-up resistor to +5V of 10K value. This establishes a logic high value, and a clamp diode (internal to TTL) establishes a low level of −0.6V. For ECL, a gate should be available to provide a static logic high level. An 820Ω pull-up resistor is wired to that output. The logic low will be more negative than is usual for ECL, but this will cause no problem. In all cases, multiple Sense outputs may be connected together from many drivers to effect a wired-or function.

A further protection scheme is to provide a series resistor from B+ to V+ and B− to V−. The resistor serves to limit the output fault current by allowing B+ and B− voltages to sag under heavy load. This also reduces the dissipation on the output transistors for valid loads. Because B+ and B− are separately bypassed, these voltages will sustain under transient loads and dynamics will not be affected.

Output Accuracy

The accuracy of the output voltage depends on several factors. The first is the gain error from V_{INH} or V_{INL} to the output, unloaded. The gain error is nominally −0.6%, and has a few tenths of a percent variation between parts. The second is supply rejection. If the B+, B−, Shunt+, or Shunt− voltages are different from those used by Elantec to test the part, there will be about 2.2 mV systematic shift in output offset per volt of supply variation. The V+ and V− supplies have much less influence on output error. Finally, there is a random V_{OS} error as specified in the data table.

Of course, the finite output impedance of the EL1056 will cause additional output error when the driver is loaded.

Power-Down

The EL1056 incorporates a power-down feature that drastically reduces power consumption of an unused driver and also drops the output leakage current to nanoamperes ("A" grade only). The output is not a low capacitance in this mode, however, and transients driven from the cable can momentarily turn on the output transistors. Power-down is intended to allow the switching of accurate DC meters onto the bus without having to relay out the driver's leakage current. It takes about 40 μs for the output leakage to sag to nanoamperes, but this is still much faster than relays or voltmeters.

Power-down is controlled by the E and $\overline{E}$ differential inputs. There is no problem with logic amplitude or slewrate, and input resistor networks are not needed.

EL1056AC/EL1056C
Monolithic High-Speed Pin Driver

Power Down — Contd.

Supply and Input Bypassing

The V+, B+, V−, and B− leads should be bypassed very closely with 0.1 μF capacitors, preferably chip type. There should be a wide ground plane between bypasses, and this can be the heatsink copper. It is wise to also have a 4.7 μF tantalum bypass capacitor within a couple of inches to the driver.

The logic inputs are active device bases, and can oscillate if presented with inductive lines. A local resistor of 1000Ω or less to ground will suffice in de-Q'ing any resonance. A 100 pF or larger capacitor can also serve as a bypass.

Thermal Considerations

The package of the EL1056 includes two fused leads on each side which are connected to the internal die mounting metal. Heat generated in the die flows through the mounting pad to the fused leads, and then to the circuit-board copper, achieving a thermal resistance to air around 40°/W. Characterization curves show the thermal resistance versus airflow rate. Consult the EL1056 Demonstration Board literature for a suggested board pattern. Note that thicker layers of copper than we used improves the thermal resistance further, to a limit of 22°C/W for an "infinite heatsink" directly soldered to the fused leads.

As a practical limit, the die temperature should be kept to 125°C rather than the allowable 150°C to retain optimum timing accuracies.

EL2021C
Monolithic Pin Driver

Features

- Wide range of programmable analog output levels
- 0.5 Ampere output drive with external transistors
- Programmable Slew Rate
- Low overshoot with large capacitive loads-stable with 500 pF
- 3-state output
- Power-down capability
- Wide supply range
- Overcurrent sense

Applications

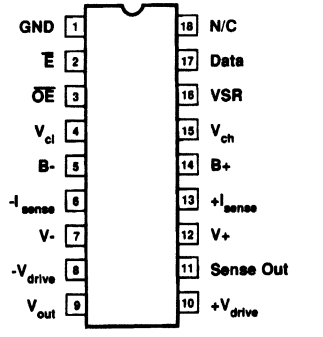
- Loaded circuit board testers
- Digital testers
- Programmable 4-quadrant power supplies

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2021CJ	0°C to +75°C	CerDIP	MDP0031

Connection Diagram

18-Pin DIP Package



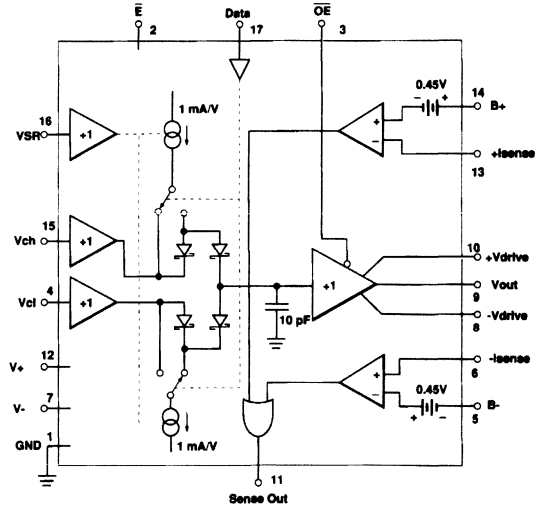
2021-1

Top View

General Description

The EL2021 is designed to drive programmed voltages into difficult loads. It has the required circuitry to be used as the pin driver electronics in board test systems. Capable of overpowering logic outputs, the part can accurately drive independently set high and low levels with programmed Slew Rates into reactive loads. It can also be placed into high impedance to monitor the load without having to disconnect. Previous board testers had multiplexing schemes to reduce the number of pin drivers required. With the small size and power consumption of the monolithic EL2021, a driver per node with little or no multiplexing becomes practical. Since only a few pins of "bed-of-nails" board testers need be active at any given time, the power-down feature saves substantial power in large systems.

Block Diagram



2021-2

Truth Table

$\overline{E}$	$\overline{OE}$	Data	V_{OUT}	Comments
0	0	0	V_{CL}	Active
0	0	1	V_{CH}	Active
0	1	X	High-Z	Third State
1	X	X	Undefined	Power-down

EL2021C
Monolithic Pin Driver

Absolute Maximum Ratings (T_A = 25°C)

V+	Supply Voltage	−0.3V to +16V	Sense Out	Output Current	−10 mA to +10 mA
V−	Supply Voltage	0.03V to −16V	V_{OUT}, Drive+, Drive−	Output Currents	−45 mA to +45 mA
B+, B−	Supply Voltages	V− to V+	T_J	Junction Temperature	150°C
Sense+	Input Voltages	(−2V + B+) to (0.3V + B+)	T_A	Operating Ambient Temperature Range	0°C to +75°C
Sense−	Input Voltages	(−0.3V + B−) to (2V + B−)			
$\overline{E}$, VSR, $\overline{OE}$, Data	Input Voltages	−0.3 to +6V	T_{ST}	Storage Temperature	−65°C to +150°C
V_{CH}, V_{CL}	Input Voltages	B− to B+ and V− to V+	P_D	Power Dissipation (T_A = 25°C) (See Curves)	1.8W

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

T_A = 25°C, V+ = 15, V− = −10V, B+ = V_{CH} +3.6V, B− = V_{CL} −3.6V, No Load. Data and $\overline{OE}$ levels are: L = 2.0V and H = 3.0V (CMOS thresholds). $\overline{E}$ levels are: L = 1.5V and H = 3.5V. All tests done using 2N2222 and 2N2907 output transistors with Beta>40 @ I_C = 400 mA and Beta>27 @ I_C = 500 mA and V_{CE} = 3.1V. $\overline{OE}$ and $\overline{E}$ low.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
I_S	V+, -Supply Currents	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = H or L	15	25	30	I	mA
		V_{CH} = 11V, V_{CL} = −6V, VSR = 5V, Data = H or L	21	33	45	IV	mA
		V_{CH} = −6V, V_{CL} = 11V, VSR+2.5V, Data = H or L	15	25	30	IV	mA
I_S, disabled	V+, -Supply Currents	V_{CH} = 5V, V_{CL} = 0V, VSR = 2.5V, Data = H or L, $\overline{E}$ = H	0	0.5	2.5	I	mA
I_{VCH}	V_{CH} Input Current	V_{CH} = −1V to +7.5V, V_{CL} = 0V, VSR = 5V, Data = H or L	−20	5	20	I	µA
I_{VCL}	V_{CL} Input Current	V_{CL} = −3.5V to +3.5V, V_{CH} = 0V, VSR = 5V, Data = H or L	−20	−5	20	I	µA
I_{Data}	Data Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0 or 5V	−50	5	50	I	µA
I_{OE}	$\overline{OE}$ Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, $\overline{OE}$ = 0V or 5V	−20	5	20	I	µA
I_E	$\overline{E}$ Input Current	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = L, $\overline{E}$ = 0V or 5V	−20	2	20	I	µA
I_{VSR}	VSR Input Current	V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 0V or 5V	−20	2	20	I	µA
$\pm I_{sense}$	Sense Input Currents	V_{CH} = 5V, V_{CL} = 0V, VSR = 5V, Data = 0V or 5V	−20	5	20	IV	µA
I_B+, I_B-	B+, B− Input Currents	V_{CH} = 5V, V_{CL} = 0V, Data = L, VSR = 5V	−20	5	20	IV	µA

DC Electrical Characteristics

T_A = 25°C, V+ = 15, V− = −10V, B+ = V_{CH} +3.6V, B− = V_{CL} −3.6V, No Load. Data and $\overline{OE}$ levels are: L = 2.0V and H = 3.0V (CMOS thresholds). $\overline{E}$ levels are: L = 1.5V and H = 3.5V. All tests done using 2N2222 and 2N2907 output transistors with Beta>40 @ I_C = 400 mA and Beta>27 @ I_C = 500 mA and V_{CE} = 3.1V. $\overline{OE}$ and $\overline{E}$ low. — Contd.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
V_O	Output Voltage	V+ = 14.5V, V− = −9.5V					
		V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = L,					
		Output Current = −100 mA, 0 mA, or +100 mA	−50		50	I	mV
		Output Current = −400 mA or +400 mA	−300		300	I	mV
		Output Current = −500 mA or +500 mA	−600		600	I	mV
		V_{CH} = 5V, V_{CL} = 0, VSR = 1V, Data = H					
		Output Current = −100 mA, 0 mA, or +100 mA	4.95		5.05	I	V
		Output Current = −400 mA or +400 mA	4.7		5.3	I	V
		Output Current = −500 mA or +500 mA	4.4		5.6	I	V
		V_{CH} = 11V, V_{CL} = −6V, VSR = 1V, I_{OUT} = 0, Data = L	−6.1		−5.9	I	V
		V_{CH} = 11V, V_{CL} = −6V, VSR = 1V, I_{OUT} = 0, Data = H	10.9		11.1	I	V
I_{sense+}	+I_{sense} Threshold	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, R_{sense} = 1Ω, Data = H	400	450	600	I	mA
I_{sense-}	−I_{sense} Threshold	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, R_{sense} = 1Ω, Data = L	−400	−450	−600	I	mA
$V_{O, sense}$	Sense Out Levels	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data L or H,					
		Output Current = −350 mA or +350 mA	0		0.6	I	V
		Output Current = −550 mA or +550 mA	3.5		5.0	I	V
$I_{OUT,TRI}$	High-Impedance Output Leakage	V_{CH} = 5V, V_{CL} = 0, VSR = 2.5V, Data = L, $\overline{OE}$ = H, Output Voltage = −2.5V or +7.5V	−100	5	100	I	µA

AC Electrical Characteristics

DC test conditions apply except where noted. For AC tests, R_L = 1k, C_L = 200 pF. Delay times are measured from $\overline{OE}$ or Data crossing 2.5V, V_{CH} = 5V, V_{CL} = 0.

Parameter	Description	Conditions	Min	Typ	Max	Test Level	Units
SR+	+Slew Rate	Data L to H, Output from 0.5V to 4.5V, VSR = 1V	80	100	120	I	V/µs
		VSR = 3V	150	240	360	I	V/µs
SR−	−Slew Rate	Data H to L, Output from 4.5V to 0.5V, VSR = 1V	−80	−100	−120	I	V/µs
		VSR = 3V	−150	−240	−360	I	V/µs
SRSYM	Slew Rate Symmetry	$\left[\frac{(SR+)-(SR-)}{(SR+)+(SR-)}\right]$ VSR = 1V	−10		10	I	%
		VSR = 2V	−20		20	IV	%
T_{pd}	Propagation Delay	Data L to H, Output to 0.2V, VSR = 2.5V	6.5	9	11.5	I	ns
		Data H to L, Output to 4.8V, VSR = 2.5V	6.5	9	11.5	I	ns
T_s	Settling Time	VSR = 5V, Data L to H, Output 4.5V to 5V ±0.2V			30	IV	ns
		VSR = 5V, Data H to L, Output 0.5V to ±0.2V			30	IV	ns
OS	Overshoot	VSR = 1V, Data L to H or H to L	−300		300	I	mV
		VSR = 1V, $\overline{OE}$ H to L, Data = L, R_L to 5V	−300		300	I	mV
		VSR = 1V, $\overline{OE}$ H to L, Data = H, R_L to 0V	−300		300	I	mV
T_{pda}	Propagation Delay, High-Z to Active	VSR = 2.5V, $\overline{OE}$ H to L, C_L = 50 pF					
		R_L to 5V, Data = L, Output to 3.5V			50	I	ns
		R_L to 0V, Data = H, Output to 1.5V			50	I	ns
T_{pdh}	Propagation Delay, Active to High-Z	VSR = 2.5V, $\overline{OE}$ L to H, C_L = 50 pF,					
		Data = L, R_L to 5V, Output to 0.5V			50	I	ns
		Data = H, R_L to 0V, Output to 4.5V			50	I	ns

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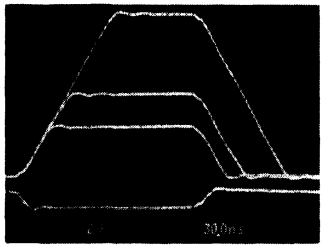
EL2021C
Monolithic Pin Driver

Pin Description Table

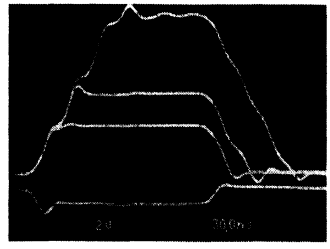
Pin #	Name	Description
1	GND	System ground.
2	$\overline{E}$	$\overline{\text{Enable}}$ control input. A logic low allows normal operation; a logic high puts the device into power down mode. No output levels are defined in powerdown nor does the output behave as a high impedance.
3	$\overline{OE}$	$\overline{\text{Output Enable}}$ input. A logic low sets the output to low-impedance driver mode; a logic high places the output into a high-impedance state.
4	V_{CL}	Lower analog control input. When Data = $\overline{OE}$ = $\overline{E}$ = L, the V_{CL} level is output as V_{OUT} (assuming $V_{CL} < V_{CH}$).
5	B−	System power supply. The EL2021 uses this pin as a negative output current monitor connection. Little current is drawn from this pin, transient or static.
6	I_{sense}−	Negative output current monitor input.
7	V−	Negative power supply. Because all negative output drive currents come from this pin (as much as 60 mA transiently), good bypassing is essential.
8	Drive−	Output to external pnp transistor base.
9	V_{OUT}	High-current input and output, depending on $\overline{OE}$.
10	Drive+	Output to external npn transistor base.
11	Sense Out	Logic output which signals that a high + or − output current is flowing.
12	V+	Positive power supply. Like V−, it should be well bypassed.
13	I_{sense}+	Positive output current monitor input.
14	B+	System power supply, similar to B−.
15	V_{CH}	Higher analog control input. When Data = H and $\overline{OE}$ = $\overline{E}$ = L, the V_{CH} level is output as V_{OUT} (assuming $V_{CH} > V_{CL}$).
16	VSR	Slew rate control input. A 1V level on this pin causes the output to slew at 100 V/μs, 0.5V causes a slew rate of 50 V/μs, etc.
17	Data	Output level control input. This pin digitally selects V_{CL} or V_{CH} as the output voltage when $\overline{OE}$ = $\overline{E}$ = L.
18	N/C	Not Connected.

Typical Performance Curves



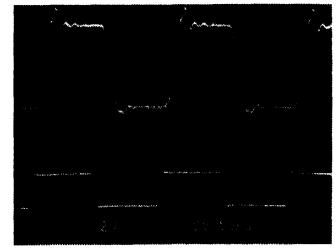
2021-3

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 50 pF, VSR = 1V.



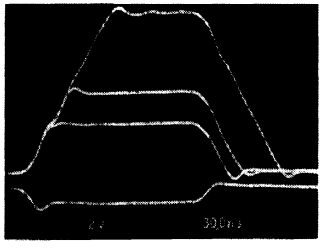
2021-4

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 200 pF, VSR = 1V.



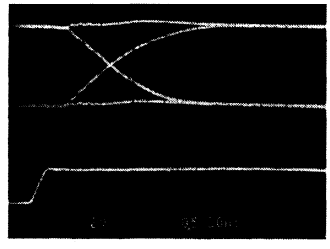
2021-5

Output waveshapes with 5 MHz data rate. C1 = 50 pF, VSR = 4V.



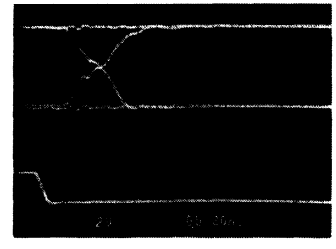
2021-6

Family of output waveshapes. ECL, TTL, CMOS, HCMOS with C1 = 200 pF, VSR = 1V, and overcompensated with 22 pF from each drive pin to ground.



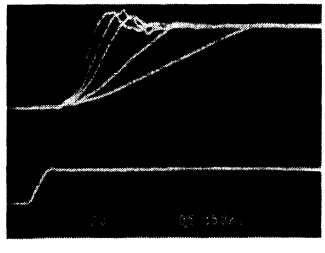
2021-7

Family of output waveshapes from active H, L to high-impedance H, L.



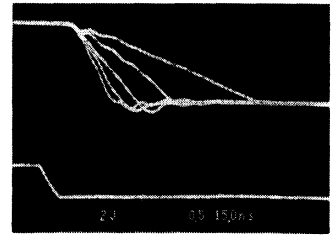
2021-8

Family of output waveshapes from high-impedance H, L to active H, L.



2021-9

Family of + output edges, 0V to 5V for VSR = 0.5V, 1V, 2V, 3V, 5V.

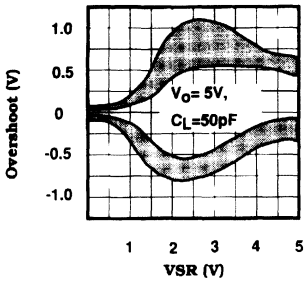


2021-10

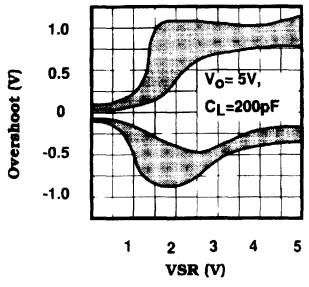
Family of—output edges, 5V to 0V or VSR = 0.5V, 1V, 2V, 3V, 5V.

Typical Performance Curves — Contd.

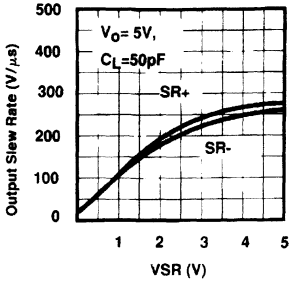
Overshoot vs VSR



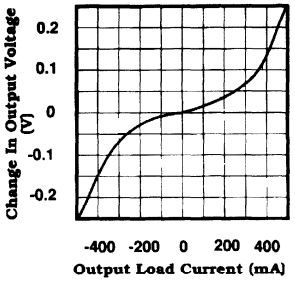
Overshoot vs VSR



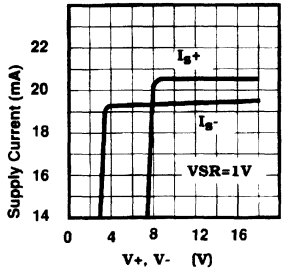
Slew Rate vs VSR



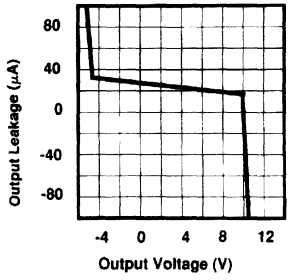
V_{OUT} vs Load Current



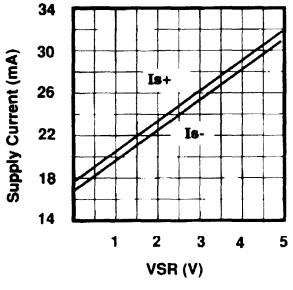
Supply Current vs Supply Voltage



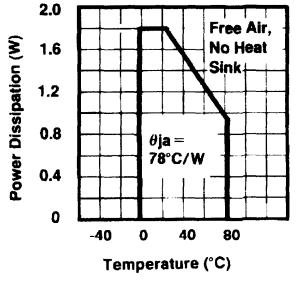
Tri-State Leakage vs Output Voltage



Supply Current vs VSR



Power Dissipation vs Temperature



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Applications Information

Output Stage

To meet the requirements of low output impedance, wide bandwidth, and large capacitive load driving capability, the EL2021 has a fairly exotic output stage. Figure 1 shows a simplified schematic of the circuit, only applicable in normal, low impedance mode. External transistors are used to handle the large load currents and peak power dissipations. Since there is no need for good AC crossover distortion performance in a pin driver, the output transistors are operated class C. That is, for small output currents, neither output transistor will conduct bias current, and when load currents do flow, one of the devices is off. This is accomplished by biasing the output transistors from Schottky diodes D1 and D2. In operation, the diode forward voltage is about 0.4V, whereas the "on" output transistor will have a V_{BE} of 0.6V. This leaves only 0.2V across the "off" transistor's base-emitter junction, not nearly enough to cause bias currents to flow in it. Schottky diodes have a temperature drift similar to silicon transistors, so the class C bias maintains over temperature. One caution is that the diodes are in the IC package and are thermally separate from the transistors, so there can exist temperature differences between packages that can cause thermal runaway. Runaway is avoided as long as the external transistors are not hotter than the EL2021 package by more than 80°C. The only way runaway has been induced as of this writing is to use "freeze spray" on the IC package while the output transistors are very hot.

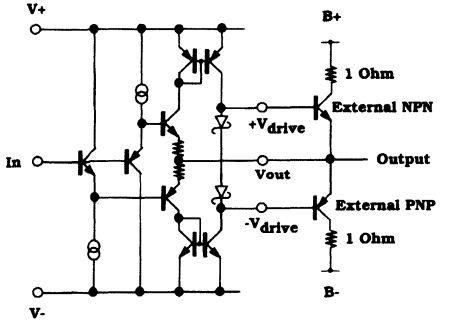


Figure 1. Simplified Output Stage (Normal Mode)

This circuit allows the external transistors to run from B+ and B− supplies that are of less voltage than V+ and V− to conserve power. Reducing B± supplies also reduces dissipations in the output devices themselves. B+ is typically made K volts more than V_{CH} and B− made K volts more negative than V_{CL}. Ideally K is made as small as possible to minimize output transistor dissipation, but two factors limit how small K can be. These factors are both related to the fact that transistors have two collector resistance numbers: "hard" and "soft" saturation resistance. As a transistor begins to saturate at high collector currents and small collector-emitter voltages, minority carriers begin to be generated from the base-collector junction. These carriers act as more collector dopant and actually reduce effective series collector resistance. At conditions of heavy saturation, the collector is flooded with minority carriers and exhibits minimum collector resistance. In this way, small geometry transistors like the 2N2222 and 2N2907 devices have excellent collector-emitter voltage drops at high currents, but are actually still in heavy saturation for 1V-2V drops. This "soft" saturation shows up as reduced beta at high currents and moderate V_{CE}'s as well as very poor AC performance. A transistor may exhibit an f_t of only 2 MHz in soft saturation when, like the 2N2222, it gives 300 MHz in non-saturated mode. The EL2021 requires the output transistors to have an f_t of at least 200 MHz to prevent degradation in overshoot, slew rate into heavy loads, and tolerance of heavy output capacitance. With a K of 3.2V and 1Ω collector resistors, almost all 2N2222 and 2N2907 devices perform well, but we have obtained devices from some vendors where the beta does indeed fall permaturely at reduced V_{CE} and high currents. It is important to characterize the external devices for the service that the EL2021 will be expected to provide.

The output stage of the EL2021 does not ring appreciably into a capacitive load in quiescent conditions, but it does ring while it slews. This is an unusual characteristic, but the output slews monotonically and the slew "ripple" does not cause problems in use. The slew ripple does cause a similar "ripple" in the overshoot-vs-VSR characteristic: the overshoot may decrease for slightly increasing VSR, then increase again for larger VSR's again. The overshoot-vs-VSR graphs

EL2021C
Monolithic Pin Driver

Applications Information — Contd.

presented in this data sheet thus reflect the range of overshoot rather than one particular device's wavy curve.

The typical 2N2222 and 2N2907 will deliver 750 mA into a short-circuit. This puts four watts of dissipation into the 2N2222 for V_{CH} = 5V. The npn can dissipate this power for a few tenths of a second as long as a metal-base TO-39 package is used. The small or non-metal-based packages have short thermal time constants and high thermal resistances, so they should withstand shorts for only a few milliseconds. The Sense Out signal should be used to control $\overline{OE}$ or reduce V_{CH} and V_{CL} to relieve the output devices from overcurrent conditions.

Transistors such as the MJE200 and MJE210 have very much improved collector resistances and high-current beta compared to the 2N2222 and 2N2907. Their f_t's are almost as good and sustain at higher currents, and high-current output accuracy will improve. They allow a K of 2V to reduce dissipations further, but short-circuit currents will be as much as two amperes! The geometries of these transistors are larger, and the added transistor capacitances will slow the maximum Slew Rates that the EL2021 can provide.

If transistors with f_t's less than 200 MHz are used, the EL2021 will need to be overcompensated. This is accomplished by connecting equal capacitors from the Drive pins to ground. These capacitors will range from 10 pF to 50 pF. The overcompensation will slow the maximum slew rate, but it will improve the overshoot and reactive load driving capability, and can be considered a useful technique.

Figure 2 shows the equivalent output stage schematic when the circuit is in high-impedance mode ($\overline{OE}$ = H). The external transistors have their base-emitter junctions each reverse-biased by a Schottky diode drop. A buffer amplifier copies the output voltage to give a bootstrapped bias for the Schottky stack. This scheme guarantees that the external transistors will be off for any output level, and the output leakage current is simply the bias current of the buffer.

The circuit works properly for AC signals up to 500 V/μs. Above this slew rate, the buffer cannot keep up and the external transistors may turn on transiently. Because of the bootstrap action, the output capacitance is less than 10 pF up to 10 MHz of small-signal bandwidth and 300 V/μs slew rate, increasing beyond these values. Adding overcompensation capacitors will degrade the slew rate that the output can withstand before current is drawn.

It is sometime necessary to provide a "snubber" network-a series R and C— to provide a local R.F. impedance for the buffer to look into. 330Ω and 56 pF should serve. Also, it is well to provide some DC path to ground (47k for instance) to bias the output stage when no actual circuit is connected to the EL2021 in high-impedance mode.

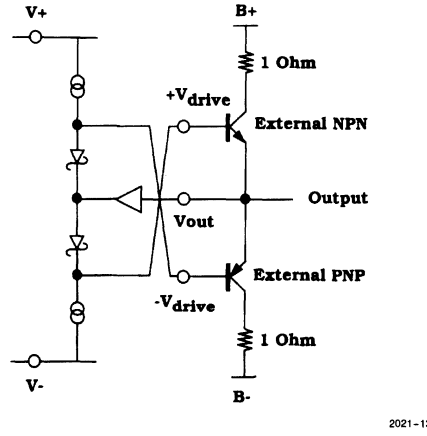


Figure 2. Simplified Output Stage (High-Impedance Mode)

Power Supplies

In typical operation, V+ and V— can be as much as ±15V and as little as V_{CH} +3V and V_{CL} −3V, respectively. When driving heavy output currents, however, it is wise to have 5V of headroom above V_{CH} and below V_{CL} to ensure no saturation of devices within the EL2021 and attendent waveshape distortions. Thus, for V_{CH} = 5V and V_{CL} = −2V, minimum operating voltages are +10, −7V. It is very important to bypass the supply terminals with low-inductance

Applications Information — Contd.

capacitors to ground, since the full base drive currents of the output transistors are derived from these supplies. Because the pulse currents can reach 60 mA, the capacitors should be at least a microfarad; 4.7 μF tantalum are ideal and require no small bypasses in parallel.

B+ and B− can be any voltage within V+ and V− and some amount previously discussed above V_{CH} and below V_{CL}. If V_{CH} or V_{CL} exceeds B+ or B−, very large internal fault currents can flow when the EL2021 attempts to bring an output transistor's base beyond the collector voltage. The bypassing care of the V± lines apply to the B± lines, as well as the fact that ampere currents can occur. Large (100 μF–500 μF) capacitors should be used to bypass perhaps every tenth EL2021.

The V_{CH}, V_{CL}, Data and $\overline{OE}$ lines should be driven locally so as to not pick up magnetic interference from the output. The inductance of interconnects to these lines can allow coupling to cause waveshape anomalies or even oscillations. If long lines are unavoidable, local 1k resistors or 50 pF–100 pF capacitors to ground can also serve the purpuse.

Data Pin

The slew rate of the input to the Data pin should be kept less than 1000 V/μs. Some feedthrough can occur for large Slew Rates which will distort the output waveshape. A 1k–2k resistor in series with the data pin will reduce feedthrough.

Current Sense

The output current is sensed by comparing the voltage dropped across the external shunt resistors to an internal 0.45V reference. The center of the trip level is adjusted for the particular output transistor betas listed in the data specifications. Transistors with less beta at high currents will cause the sense comparators to trip at slightly higher output currents. The 1Ω shunt resistors should be non-inductive. The family of wirewound resistors called "non-inductive" are too inductive for these shunts.

The response of the Sense Out can be thought of as slow attack and fast decay. A continuous overcurrent condition must last for at least 2 μs before Sense Out will go high, but will clear to low only about 200 ns after the overcurrent is withdrawn. This allows transient currents due to slewing capacitive load to not generate a flag. On the other hand, the output transistors will not be damaged with only a 2 μs system reaction time to a short-circuit.

Construction Practices

The major cautions in connecting to the EL2021 involve magnetic rather than capacitive parasitic concerns. The circuits can output as much as 100 A/μs. Even with normal Slew Rates and moderately large capacitive loads, the dI/dT can cause magnetic fields in harmless looking wires to fill adjacent lines with noise, and sometimes ringing or even sustained feedback. Thus, rules for wiring the EL2021 are:

(a) Keep leads short and large. Short wires are less inductive, as are wires with large surface area. The large surface area also reduces skin resistance at high frequencies, important at high currents (at 100 MHz, current penetrates only a few microns in metals).

(b) Use a ground plane. Due to inductance and skin effect, "ground" voltages will be different only inches apart on a copper ground plane. Individual wires do not create ground at high frequencies. The common "star" ground is a very bad idea for high-current and high-frequency circuits.

(c) Dress all wires against the ground plane. The magnetic fields that the wires would have generated will be intercepted by the ground plane and absorbed, thus reducing the wire's effective inductance. The capacitance added by this method is not important to EL2021 operation.

(d) The external transistors should have short interconnects to the EL2021, the collector shunt resistors, and the bypass capacitors. As previously stated, the shunt resistors must not be wire wound because of their inductance.

EL2021C
Monolithic Pin Driver

Applications Information — Contd.

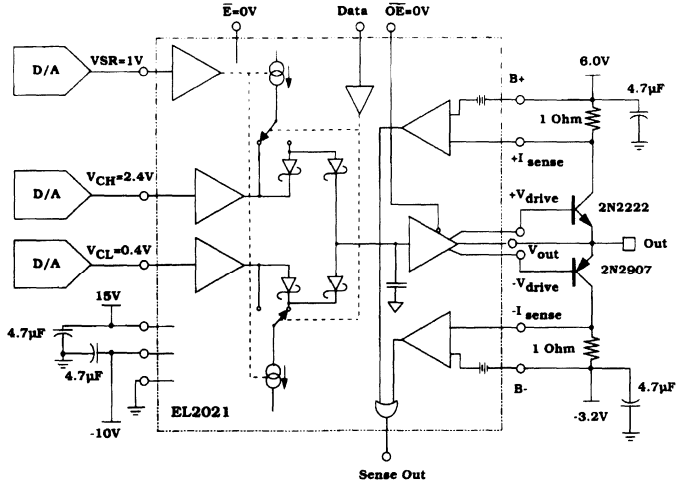
(e) The bypass capacitors should have low series resistance and inductance, but should not have a high Q. This may seem contradictory, but a 4.7 μF tantalum capacitor seems to work the best. An electrolytic capacitor should be added to help bolster the supply levels in the 0.1 μs–1 μs after a transition. No small capacitors are needed in parallel with the tantalums. The bypasses' ground returns are best connected to the area of ground inside the package outline to reduce the circulating current path length, if possible.

Using the EL2021 without External Transistors

By connecting both drive pins to the output pin, the EL2021 can be used as a stand-alone driver, not requiring the external transistors. The EL2021 is good for more than 50 mA in this mode. The output impedance rises to 12Ω, however, and the current sense and high-impedance mode are not available. The ripple seen in slew edges using the external transistors is largely absent from the standalone waveshapes; and overshoot is markedly improved at VSR > 1V, especially with large capacitive loads.

Typical Applications

100 V/μs High-Current Pin Driver Outputting TTL Levels



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EL2252C
Dual 50 MHz Comparator/Pin Receiver

Features

- Fast response—7 ns
- Inputs tolerate large overdrives with no speed nor bias current penalties
- Propagation delay is relatively constant with variations of input Slew Rate, overdrive, temperature, and supply voltage
- Output provides proper CMOS or TTL logic levels
- Hysteresis is available on-chip
- Large voltage gain—8000 V/V
- Not oscillation-prone
- Can detect 4 ns glitches
- MIL-STD-883 Rev. C compliant

Applications

- Pin receiver for automatic test equipment
- Data communications line receiver
- Frequency counter input
- Pulse squarer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2252CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2252CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EL2252 dual comparator replaces the traditional input buffer + attenuator + ECL comparator + ECL to TTL translator circuit blocks used in digital equipment. The EL2252 provides a quick 7 ns propagation delay while complying with ±10V inputs. Input accuracy and propagation delay is maintained even with input signal Slew Rates as great as 4000 V/μs. The EL2252 can run on supplies as low as −5.2V and +9V and comply with ECL and CMOS inputs, or use supplies as great as ±18V for much greater input range.

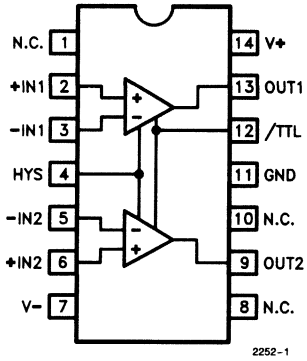
The EL2252 has a /TTL pin which, when grounded, restricts the output V_{OH} to a TTL swing to minimize propagation delay. When left open, the output V_{OH} increases to a valid CMOS level.

The comparators are well behaved and have little tendency to oscillate over a variety of input and output source and load impedances. They do not oscillate even when the inputs are held in the linear range of the device. To improve output stability in the presence of input noise, an internal 60 mV of hysteresis is available by connecting the HYS pin to V−.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1; "*Elantec's Processing, Monolithic Integrated Circuits*".

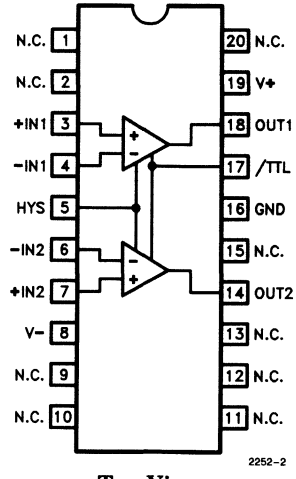
Connection Diagrams

14-Pin DIP



Top View

20-Pin SOL



Top View

EL2252C
Dual 50 MHz Comparator/Pin Receiver

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Operating Junction Temperature	150°C
Voltage at V+	18V	Storage Temperature Range	−65° to +150C
Voltage between −IN and +IN pins	36V	Lead Temperature	
Output Current	12 mA	DIP Package	
Current into +IN, −IN, HYS		(Soldering, <10 seconds)	300°C
or /TTL	5 mA	SOL Package	
Internal Power Dissipation	See Curves	Vapor Phase (<60 seconds)	215°C
Operating Ambient Temperature Range	−25°C to +85°C	Infrared (<15 seconds)	220°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; HYS and /TTL grounded; T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level EL2252C	Units
V_{OS}	Input Offset Voltage	25°C		1	6	I	mV
		Full			10	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		7		V	µV/C
I_B	Input Bias Current at Null	25°C		6	12	I	µA
		Full			17	III	µA
I_{OS}	Input Offset Current	25°C		0.2	1	I	µA
		Full			2	III	µA
R_{IN}, diff	Input Differential Resistance	25°C		30		V	kΩ
R_{IN}, comm	Input Common-Mode Resistance	25°C		10		V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	pF
V_{CM}+	Positive Common-Mode Input Range	Full	10	13		II	V
V_{CM}−	Negative Common-Mode Input Range	Full	−9	−12		II	V
A_{VOL}	Large Signal Voltage Gain V_O = 0.8V to 2.0V	25°C	4000	8000		I	V/V
		Full	3000			III	V/V

DC Electrical Characteristics

V_S = ±15V; HYS and /TTL grounded; T_A = 25°C unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level EL2252C	Units
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	70	95		II	dB
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	70	90		II	dB
V_{HYS}	Peak-to-Peak Input Hysteresis with HYS connected to V−	25°C		60		V	mV
V_{OH}	High Level Output, CMOS Mode	Full	4.0	4.6	5.1	II	V
	TTL Mode	Full	2.4	2.7	3.2	II	V
V_{OL}	Low Level Output, I1 = 0	Full	−0.2	0.2	0.4	II	V
	I1 = 5 mA	Full	−0.2	0.4	0.8	II	V
I_S+	Positive Supply Current	Full		16	19	II	mA
I_S-	Negative Supply Current	Full		17	20	II	mA

AC Electrical Characteristics

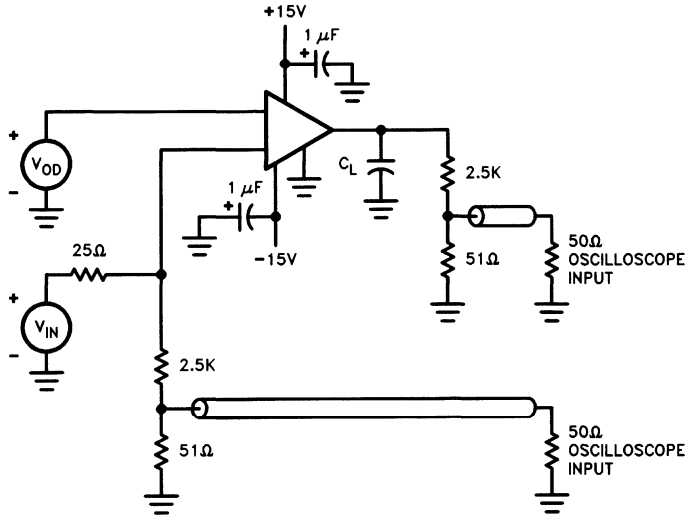
V_S = ±15V; C_L = 10 pF; T_A = 25°C; TTL output threshold is 1.4V, CMOS output threshold is 2.5V; unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level EL2252C	Units
$T_{PD}+$, $T_{PD}-$	Input to Output Propagation Delay, 0 < V_{IN} < 5V, 500 mV Overdrive, 2000 V/μs Input Slew Rate TTL Output Swing		6	9	III	ns
	CMOS Output Swing		8		V	ns
$T_{PD}+$, $T_{PD}-$	Input to Output Propagation Delay, −2V < V_{IN} < −1V, 500 mV Overdrive, 2 ns Input Rise Time TTL Output Swing		5	9	III	ns
	CMOS Output Swing		9		V	ns
T_{PDSYM}	Propagation Delay Change between Positive and Negative Input Slopes		1.25		V	ns

Note 1: Two tests are performed with V_{CM} = 0V to −9V and V_{CM} = 0V to 10V.
Note 2: Two tests are performed with V+ = 15V, V− changed from −10V to −15V;
V− = −15V, V+ changed from 10V to 15V.

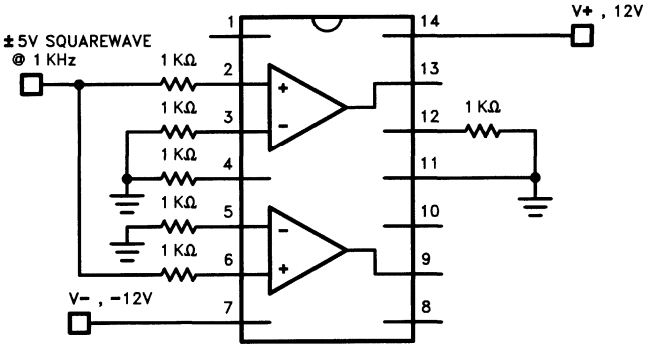
EL2252C
Dual 50 MHz Comparator/Pin Receiver

AC Test Circuit



2252-3

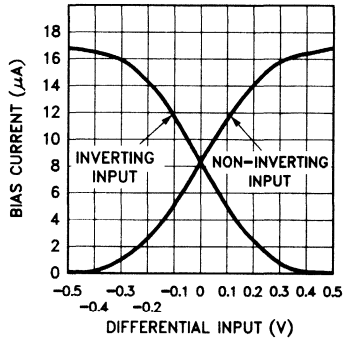
Burn-In Circuit



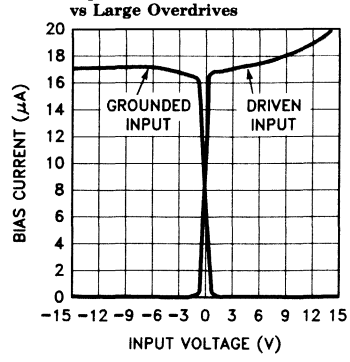
2252-4

Typical Performance Curves

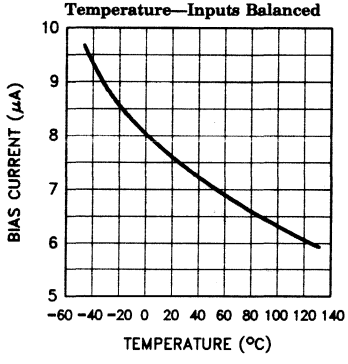
Input Bias Current vs Small Overdrives



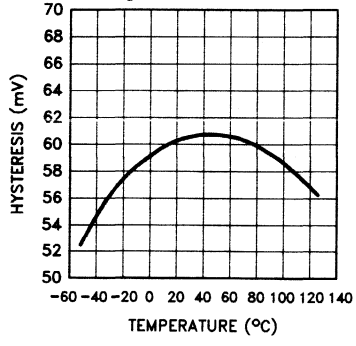
Input Bias Current vs Large Overdrives



Bias Current vs Temperature—Inputs Balanced

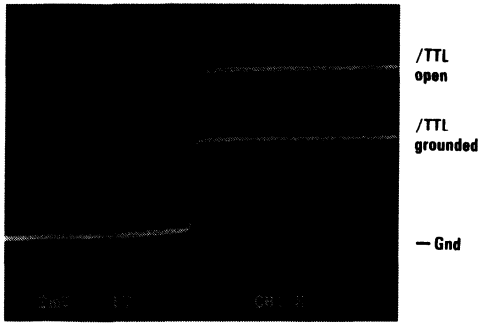


Input Hysteresis Voltage vs Temperature



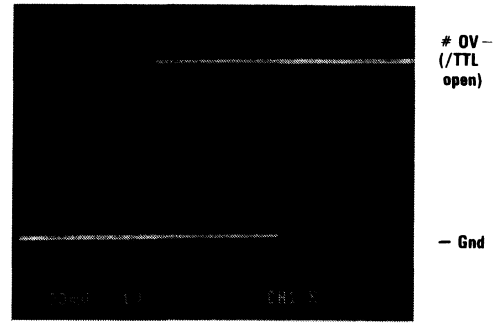
2252-5

Input/Output Transfer Function—HYS Open



2252-6

Input/Output Transfer Function—HYS Connected to V

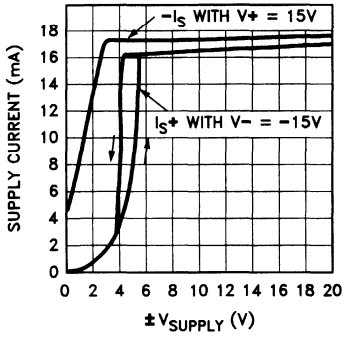


2252-7

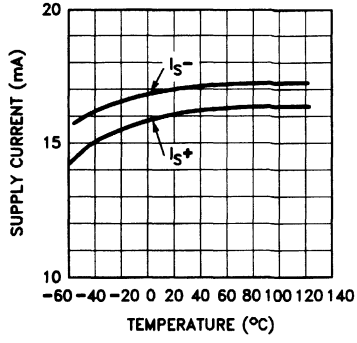
EL2252C
Dual 50 MHz Comparator/Pin Receiver

Typical Performance Curves — Contd.

Supply Current vs Supply Voltage

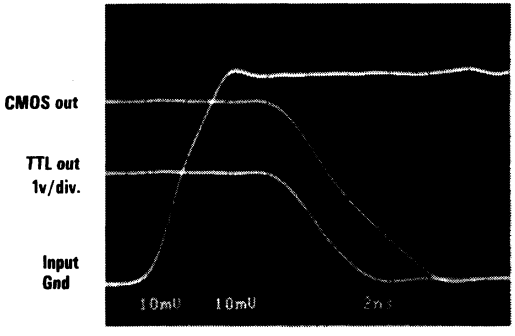


Supply Current vs Temperature (V_S = ±15V)



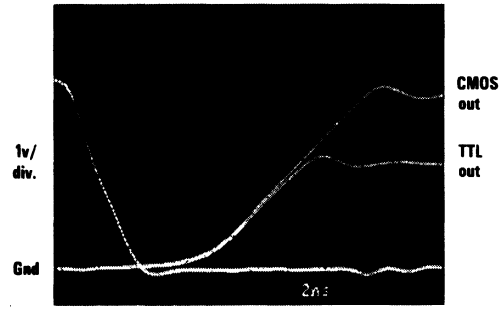
2252-8

Output Delay—0.5V Overdrive



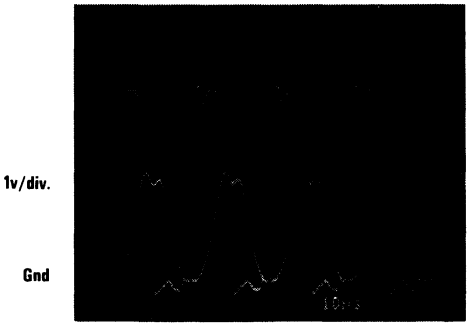
2252-9

Output Delay—0.5V Overdrive



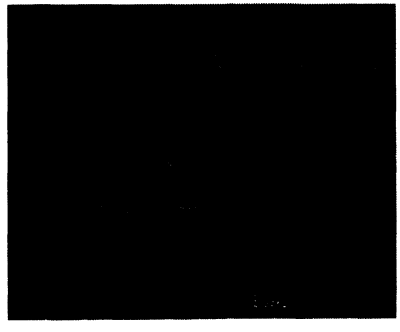
2252-10

Output with 50 MHz CMOS Input



2252-11

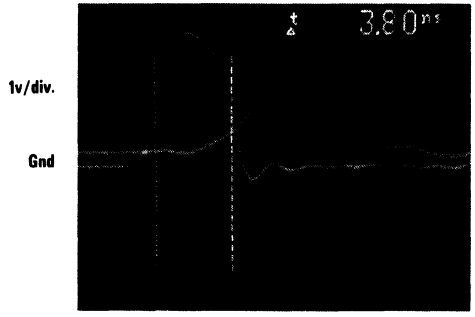
Output with 50 MHz ECL Input



2252-12

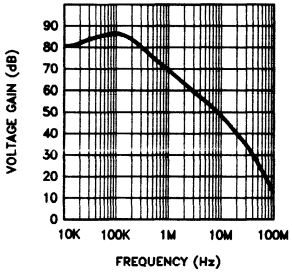
Typical Performance Curves — Contd.

4 ns TTL Glitch Detection

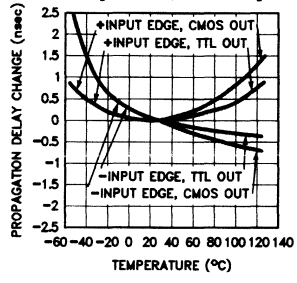


2252-13

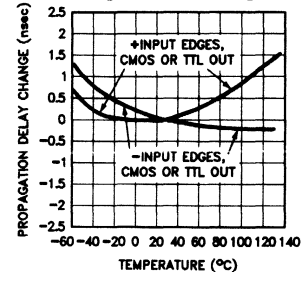
Gain vs Frequency



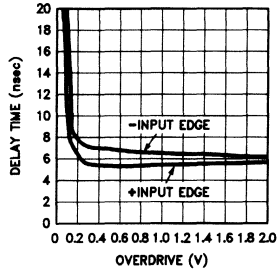
Propagation Delay vs Temperature, CMOS Input



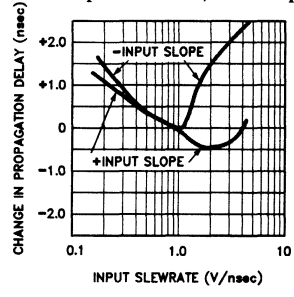
Propagation Delay vs Temperature, ECL Input



Propagation Delay vs Overdrive, CMOS Input



Propagation Delay vs Input Slew Rate, CMOS Input

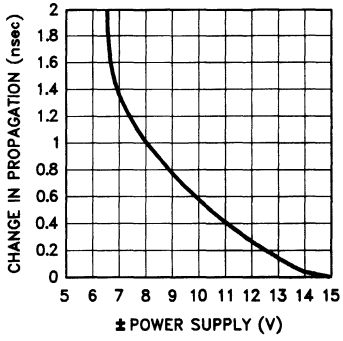


2252-14

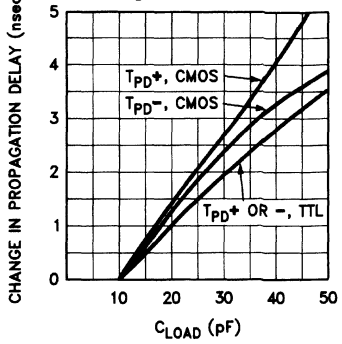
EL2252C
Dual 50 MHz Comparator/Pin Receiver

Typical Performance Curves — Contd.

Propagation Delay vs Power Supply Voltage

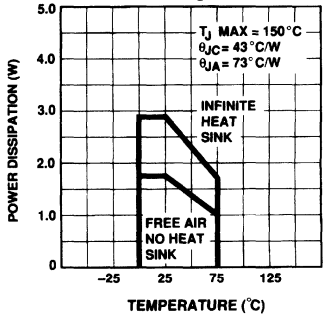


Propagation Delay vs Load Capacitance



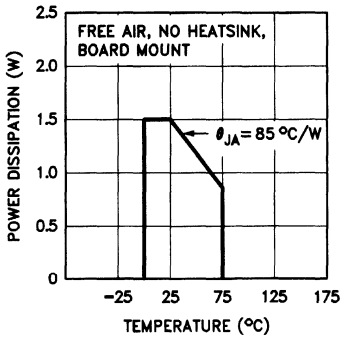
2252-15

14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2252-16

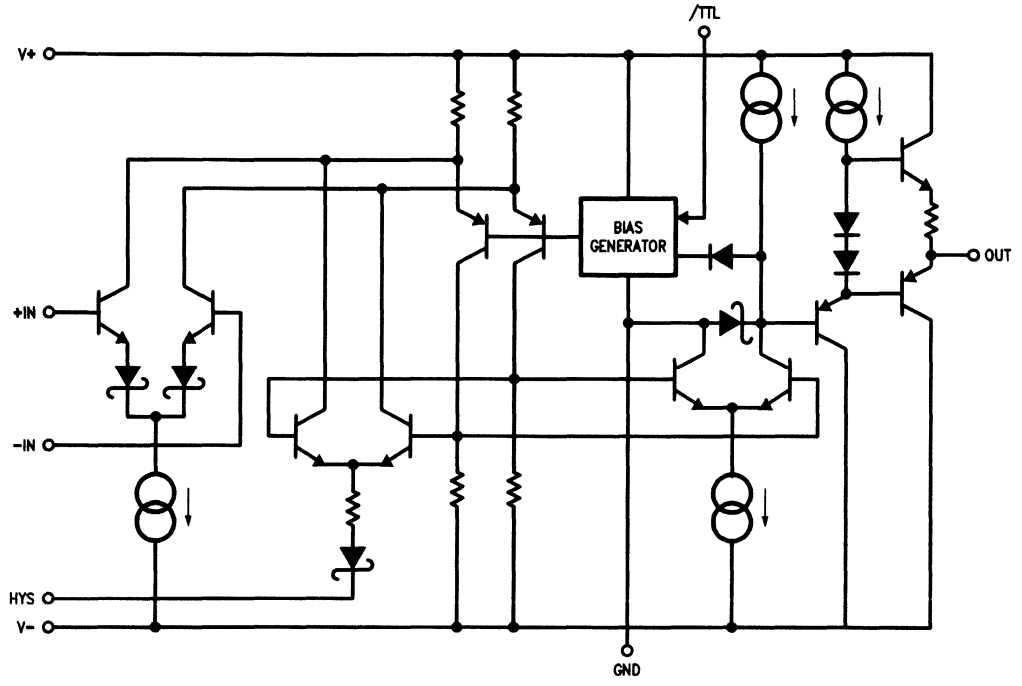
20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2252-18

Simplified Schematic

One Comparator



2252-19

Applications Information

The EL2252 is very easy to use and is relatively oscillation-free, but a few items must be attended. The first is that both supplies should be bypassed closely. 1 μF tantalums are very good and no additional smaller capacitors are necessary. The EL2252 requires V− to be at least 5V to preserve AC performance. V+ must be at least 6V for a TTL output swing, 8V for CMOS outputs.

The input voltage range will be referred to the more positive of the two inputs. That is, bringing an input as negative as V− will not cause problems; it's the other input's level that must be considered. The typical input range is +13/−12V when the supplies are ±15V. This range diminishes over temperature and varies with processing; it is wise to set power supplies such that V+ is 5V more positive than the most positive input signal and V− more negative than 6V below the most negative input. ±12V supplies will easily encompass all CMOS and ECL logic inputs. If the input exceeds the device's common-mode input capability, the EL2252 propagation delay and input bias current will increase. Fault currents will occur with inputs a diode below V− or above V+. No damage nor V_{OS} shift will occur even when fault currents within the absolute maximum ratings.

EL2252C
Dual 50 MHz Comparator/Pin Receiver

Applications Information — Contd.

One of the few ways in which oscillations can be induced is by connecting a high-Q reactive source impedance to the EL2252 inputs. Such sources are long wires and unterminated coaxial lines. The source impedance should be de-Q'ed. One method is to connect a series resistor to the EL2252 input of around 100Ω value. More resistance will calm the system more effectively, but at the expense of comparator response time. Another method is to install a "snubber" network from comparator input to ground. A snubber is a resistor in series with a small capacitor, around 100Ω and 33 pF. Each physical and electrical environment will require different treatments, although many need none.

The major use of the HYS pin is to suppress noise superimposed on the input signal. By shorting the HYS pin to V^- a ±30 mV hysteresis is placed around the V_{OS} of the comparator input. Leaving the pin open, or more appropriately, grounding the HYS pin removes all hysteresis. Connecting a resistor between HYS and V^- allows an adjustment of the peak-to-peak hysteresis level. Unfortunately, an external resistor cannot track the internal devices properly, so temperature and unit-to-unit variations of hysteresis are increased. The relationship between the resistor and resulting hysteresis level is not linear, but a 1.5k resistor will approximately halve the nominal value.

The time delay of the EL2252 will increase by about 0.7 ns when using full hysteresis.

The EL2252 is specifically designed to be tolerent of large inputs. It will exhibit very much increased delay times for input overdrives below 100 mV. If very small overdrives must be sensed, the EL2018 or EL2019 comparators would be good choices, although they lose accuracies with signal input Slew Rates above 400 V/μs. The EL2252 keeps its timing accuracy with input Slew Rates between 100 V/μs and 4000 V/μs of input Slew Rate.

The output stage drives tens of pF load capacitances without increased overshoot, but propagation delay increases about 1 ns per 10 pF. The output circuit is not a traditional TTL stage, and using an external pullup resistor will not change the V_{OH}. In general setting the output swing to TTL (by grounding the /TTL pin) will optimize overall propagation delay and ±swing symmetry.

EL2252C Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +V
*                   |     |     |     -V
*                   |     |     |     |     HYS
*                   |     |     |     |     |     TTL
*                   |     |     |     |     |     |     output
*                   |     |     |     |     |     |     |
.subckt M2252       2     3     14    7     4     5     13
*
* Application Hints:
*
* Connect pin 4 to ground through 1000 MΩ resistor to inhibit
* Hysteresis; to invoke Hysteresis, connect pin 4 to V-.
*
* Connect pin 5 to ground to invoke TTL VOH; pin 5 may left open
* for CMOS VOH.
*
* To facilitate .OP, set itl1 = 200, itl2 = 200, set node 27 to 13.8V,
* and node 30 to -12V.
*
*Input Stage
*
i1 22 7 1.7mA
r1 14 20 300
r2 14 21 300
q1 20  2 22 qn
q2 21  3 22 qn
q3 20 26 23 qn
q4 21 25 23 qn
q13 25 27 20 qp
q14 26 27 21 qp
v1 14 27 1.2V
r3 23 24 1.4k
d1 24 4 ds
r4 25 33 700
r5 26 33 700
q16 33 33 34 qn
q17 34 34 37 qn
v4 37 7 1.2V
*
* 2nd Stage
*
i2 30 7 3mA
i3 14 28 1.5mA
q7 0 35 28 qp
v2 44 0 1.2V
s1 44 35 5 0 swa
s2 45 35 5 0 swb
rsw 14 5 10k
```

EL2252C Macromodel — Contd.

```
v3 45 0 2.5V
q5 0 26 30 qn
q6 28 25 30 qn
d3 0 28 ds
*
* Output Stage
*
i4 14 38 1mA
q8 38 38 39 qn
q9 32 32 39 qp
q10 7 28 32 qp
q11 14 38 40 qn 2
q12 7 28 13 qp 2
r6 40 13 50
c1 28 0 3pF
*
* Models
*
.model qn npn (is=2e-15 bf=120 tf=0.2nS cje=0.2pF cjc=0.2pF ccs=0.2pF)
.model qp pnp (is=0.6e-15 bf=60 tf=0.2nS cje=0.5pF cjc=0.3pF ccs=0.2pF)
.model ds d(is=3e-12 tt=0.05nS eg=0.72V vj=0.58)
.model swa vswitch (von=0v voff=2.5V)
.model swb vswitch (von=2.5 voff=0V)
.ends
```

Comparators

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELANTEC Part Number	Description	Typ Prop Delay (5 mV over-drive)	Typ Open Loop Gain (V/V)	Input Common Mode Range		Typ Input Bias Current	Max Supply Current		Temp Range	Packages
				(V_{CC} = ±15V)	(V_{CC} = ±5V)		Output Active	Output 3-State		
EL2018C	Fast, High Voltage Comparator with Latch 3-State Output Monolithic	20 ns From Input to Output	40,000 (92 dB)	±12V Min	±3V Typ	±100 nA	+11/−18 mA	+7/−6.5 mA	0°C to +75°C	8-Pin P-DIP 8-Pin TO-99
EL2019C	Fast, High Voltage Comparator with Master Slave Flip-Flop, 3-State Output, Monolithic	6 ns Setup, 20 ns From Clock to Output	V_{uncert} 30 μV (Typ.)	±12V Min	±3V Typ	±100 nA	+12/−18 mA	+7/−8 mA	0°C to +75°C	8-Pin P-DIP 8-Pin TO-99

EL2018C

Fast, High Voltage Comparator with Transparent Latch

Features

- Fast response time—20 ns
- Wide input differential voltage range—24V to ±15V supplies
- Precision input stage—V_{OS} = 1 mV
- Low input bias current—I_B = 100 nA
- Low input offset current—I_{OS} = 30 nA
- ±4.5V to ±18V supplies
- 3-State TTL and CMOS compatible output
- No supply current glitch during switching
- High voltage gain—40 V/mV
- 50% power reduction in shutdown mode
- Input and latch remain active in shutdown mode
- P/N compatible with industry standard comparators

Applications

- Analog to digital converters
- ATE pin receiver
- Precision crystal oscillators
- Zero crossing detector
- Window detector
- Pulse width modulation generator
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2018CN	0°C to +75°C	P-DIP	MDP0031

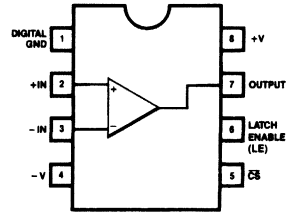
General Description

The EL2018 represents a quantum leap forward in comparator speed, accuracy and functionality. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures the part maintains speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and latch remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see QRA1: *Elantec's Processing-Monolithic Products.*

Connection Diagram

8-Pin Plastic DIP



2018-2

Top View

EL2018C
Fast, High Voltage Comparator with Transparent Latch

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	I_O	Continuous Output Current	25 mA
V_{IN}	Input Voltage	$+V_S$ to $-V_S$	T_A	Operating Temperature Range	0°C to +75°C
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies	T_J	Operating Junction Temperature Plastic DIP Package	150°C
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA	T_{ST}	Storage Temperature	−65°C to +150°C
I_{INS}	Input Current (Pins 5 or 6)	±5 mA		Lead Temperature (Soldering, 10 seconds)	300°C
P_D	Maximum Power Dissipation (Note 4—See Curves)	1.25W			
I_{OP}	Peak Output Current	50 mA			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage (Note 1) V_{CM} = 0V, V_O = 1.4V	25°C		1.0	3	I	mV
		T_{MIN}, T_{MAX}			5	III	mV
I_B	Input Bias Current V_{CM} = 0V, Pin 2 or 3	25°C		100	300	I	nA
		T_{MIN}, T_{MAX}			500	III	nA
I_{OS}	Input Offset Current V_{CM} = 0V	25°C		30	150	I	nA
		T_{MIN}, T_{MAX}			250	III	nA
CMRR	Common Mode Rejection Ratio (Note 2)	25°C	85	105		I	dB
		T_{MIN}, T_{MAX}	80			III	dB
PSRR	Power Supply Rejection Ratio (Note 3)	25°C	85	100		I	dB
		T_{MIN}, T_{MAX}	77			III	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	V
		T_{MIN}, T_{MAX}	±12			III	V
A_V	Voltage Gain V_{OUT} = 0.8V to 2.0V	25°C	15	40		I	V/mV
		T_{MIN}, T_{MAX}	10			III	V/mV
V_{OL}	Output Voltage Logic Low I_{OL} = 0 mA to 8 mA	25°C	−0.05	0.15	0.4	I	V
		T_{MIN}, T_{MAX}	−0.1		0.4	III	V

DC Electrical Characteristics V_S = ±15V unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level	Units
V_{oh}	Output Voltage Logic High V_S = ±15V	25°C	3.5	4.0	4.65	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	3.5		4.65	III	V
	V_S = ±5V	25°C	2.4			I	V
	V_S = ±5V	T_{MIN}	2.4			III	V
	V_S = ±5V	T_{MAX}	2.4			III	V
V_{odis1}	V_{OUT} Range, Disabled, I_{OL} = −1 mA V_S = ±15V	25°C	4.65			I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	4.65			II	V
	V_S = ±5V	25°C		3.5		V	V
V_{odis2}	V_{OUT} Range, Disabled, I_{OL} = 1 mA V_S = ±5V to ±15V	ALL	−0.3	−1		II	V
V_{inh}	LE or $\overline{CS}$ Inputs Logic High Input Voltage	25°C	2.0			I	V
		T_{MIN}, T_{MAX}	2.2			III	V
V_{inl}	LE or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	V
		T_{MIN}, T_{MAX}			0.8	III	V
I_{in}	LE or $\overline{CS}$ Inputs Logic Input Current V_{IN} = 0V to 5V	25°C			±200	I	µA
		T_{MIN}, T_{MAX}			±300	III	µA
I_{s+en}	Positive Supply Current Enabled	25°C		8.4	10	I	mA
		T_{MIN}, T_{MAX}			11	III	mA
I_{s+dis}	Positive Supply Current Disabled	25°C		4.7	6	I	mA
		T_{MIN}, T_{MAX}			7	III	mA
I_{s-en}	Negative Supply Current Enabled	25°C		13.0	17	I	mA
		T_{MIN}, T_{MAX}			18	III	mA
I_{s-dis}	Negative Supply Current Disabled	25°C		5.0	6.5	I	mA
		T_{MIN}, T_{MAX}			6.5	III	mA

EL2018C
Fast, High Voltage Comparator with Transparent Latch

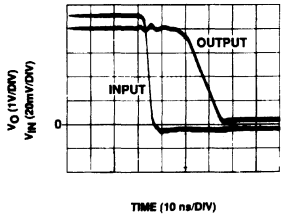
AC Electrical Characteristics $V_S = \pm 15V, T_A = 25°C$

Parameter	Description	Min	Typ	Max	Test Level	Units
T_{pd}	Propagation Delay, 5 mV Overdrive		20	40	III	ns
T_s	Setup Time		6	12	IV	ns
T_h	Hold Time		−2	0	IV	ns
T_{un}	Unlatch Time		23	40	IV	ns
T_{mpw}	Minimum Clock Pulse Width		12		V	ns
T_{en}	Output 3-State Enable Delay		40	70	IV	ns
T_{dis}	Output 3-State Disable Delay		150	300	IV	ns

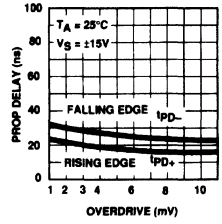
Note 1: $V_{OUT} = 1.4V$.
Note 2: $V_{CM} = 12V$ to $-12V$.
Note 3: $V_S = \pm 5V$ to $\pm 15V$.
Note 4: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

Typical AC Performance Curves

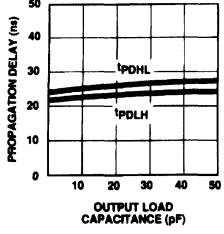
Propagation Delay (−) 5 mV Overdrive



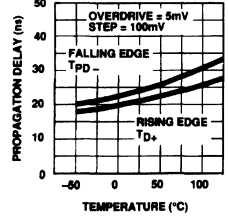
Propagation Delay vs Overdrive



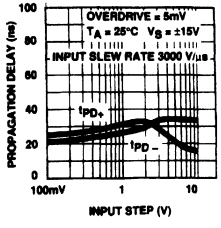
Propagation Delay vs Load Capacitance



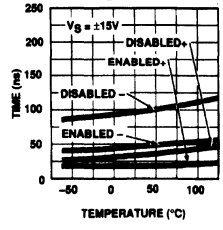
Propagation Delay vs Temperature



Propagation Delay vs Input Step



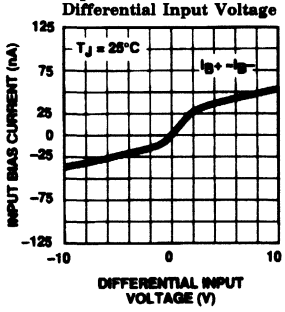
Enabled/Disabled Time vs Temperature



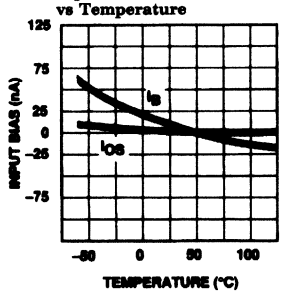
2018-3

Typical AC Performance Curves — Contd.

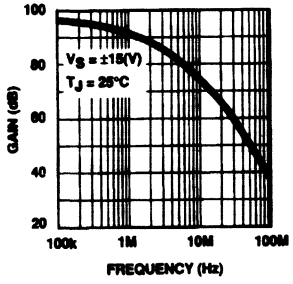
Input Bias Current vs Differential Input Voltage



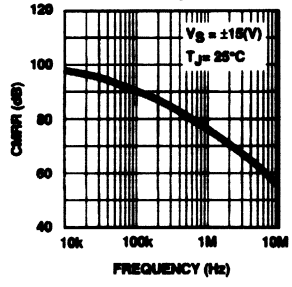
Input Bias Current vs Temperature



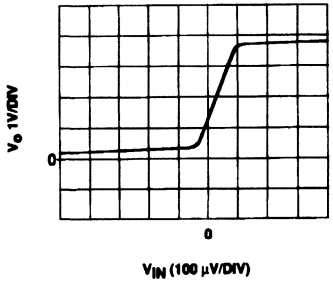
Open-Loop Gain vs Frequency



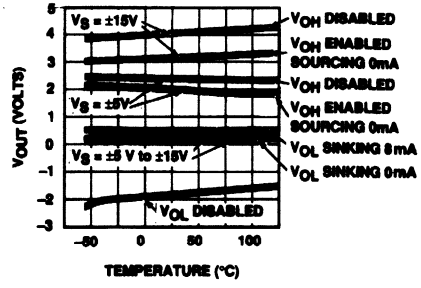
CMRR vs Frequency



V_O/V_I Transfer Characteristic



V_{OUT} vs Temperature



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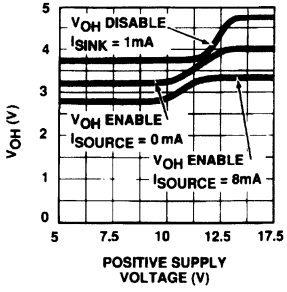
6

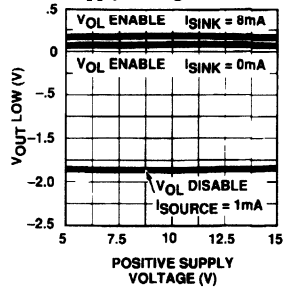
EL2018C
Fast, High Voltage Comparator with Transparent Latch

Typical Performance Curves — Contd.

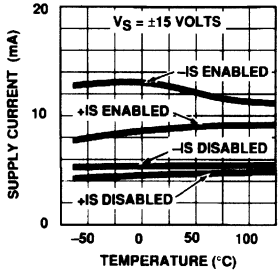
V_{OH} vs Positive Supply Voltage



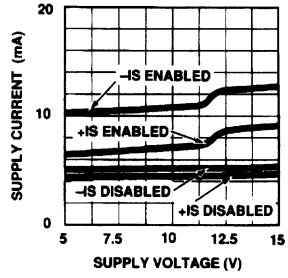
V_{OL} vs Positive Supply Voltage



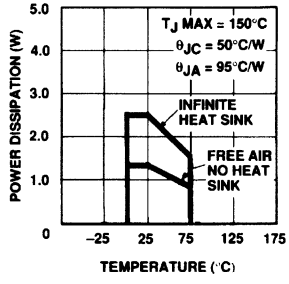
Supply Current vs Temperature



Supply Current vs Supply Voltage



8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



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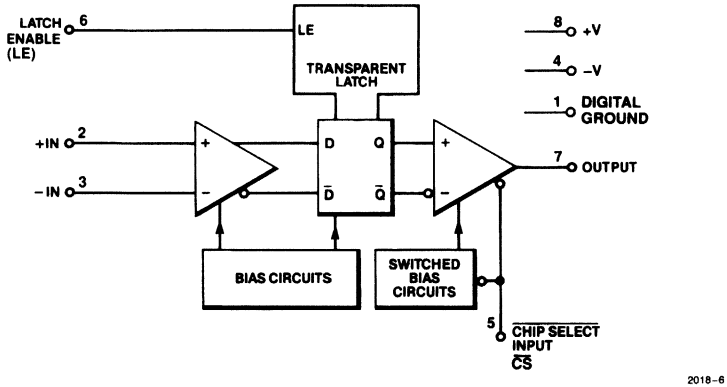
EL2018C

Fast, High Voltage Comparator with Transparent Latch

Block Diagram



Function Table

Inputs (time n−1)				Internal Q	Notes	Output
+IN	−IN	$\overline{CS}$	LE			
+	−	L	L	H	Normal Comparator Operation	H
−	+	L	L	L		L
+	−	H	L	H	Internal Normal Comparator Operation	High Z
−	+	H	L	L	Output Power Down Mode	High Z
X	X	L	H	Qn−1	Data Retained in Latch	Qn−1
X	X	H	H	Qn−1	Data Retained in Latch Power Down Mode	High Z

Application Hints

Device Overview

The EL2018 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Dielectric Isolation Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2018 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.1 μF monolithic ceramic recommended) close to the power supply leads. Good ground plane construction techniques enhance stability, and the lead from pin 1 to ground should be short.

Front End

The EL2018 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V). The transfer function of the EL2018 is linear, and the output is stable when in the linear region.

The large common mode range (±12V minimum) and differental voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

EL2018C
Fast, High Voltage Comparator with Transparent Latch

Application Hints — Contd.

Recovery from Large Overdrives
Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device.

Input Slew Rate
All comparators have input slew rate limitations. The EL2018 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators.

Latch
The EL2018 contains a "transparent" latch. A "transparent" latch acts as an amplifier when the LE input is low and it "latches" and holds the value it had just before the LE transition from low to high.

It is possible to make an oscillation resistant design by putting a short duration "0" on the LE input whenever you wish to make a comparison. This gates the comparator on only for a brief instant, long enough to compare, but not long enough to oscillate. The minimum duration of this pulse is specified by the minimum clock width parameter in the AC electrical tables.

The $\overline{CS}$ input may be left floating and still produce a guaranteed logic "0" input (active). Floating the LE input will normally produce a logic "0" input also, but operation is not guaranteed.

Proper RF technique suggests that these inputs be grounded or pulled to ground if they are not used.

Output Stage
The output stage of the EL2018 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2018 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature
The EL2018 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in a large ATE system where there may be 1000 comparators, but only 10% are in use at any one time.

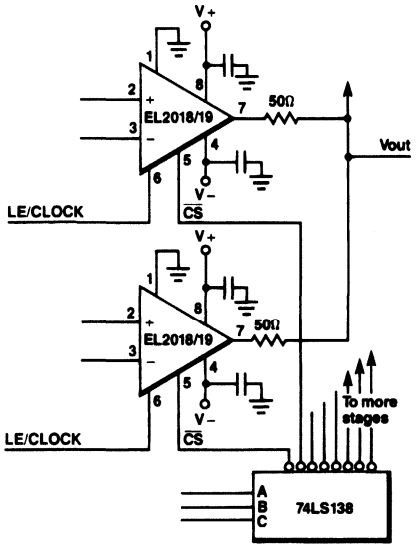
Due to the power saving feature and linear output stage, the EL2018 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2018 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

System Design Considerations
The most common problem users have with high speed comparators is oscillations due to output to input feedback. This can be avoided by using a ground plane, proper supply bypassing, and routing the inputs and outputs away from each other. Since the EL2018 has a gain bandwidth product of about 40 GHz, layout and bypassing are important to a successful system design. A unique alternative to the EL2018 is the EL2019, with its edge triggered master/slave flip flop.

Device Functions
The various operating states of the EL2018 are described in the function table on page 7.

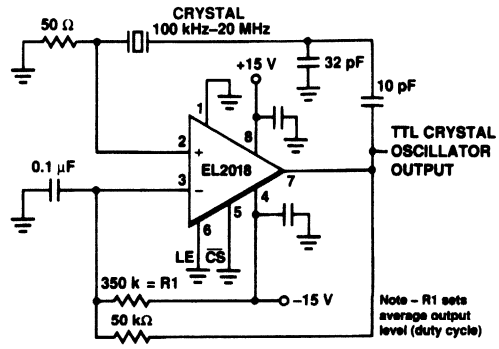
Typical Applications

Using the Power Down/ 3-State Feature



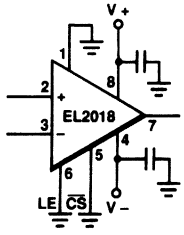
2018-7

Series Resonant Crystal Oscillator



2018-8

Using the EL2018 in the Transparent Mode (Latch Not Used)



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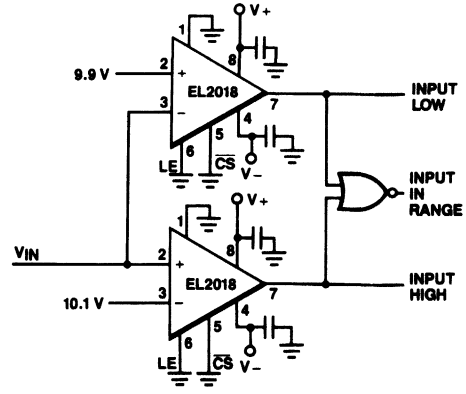
A Wide Input Range Window Comparator

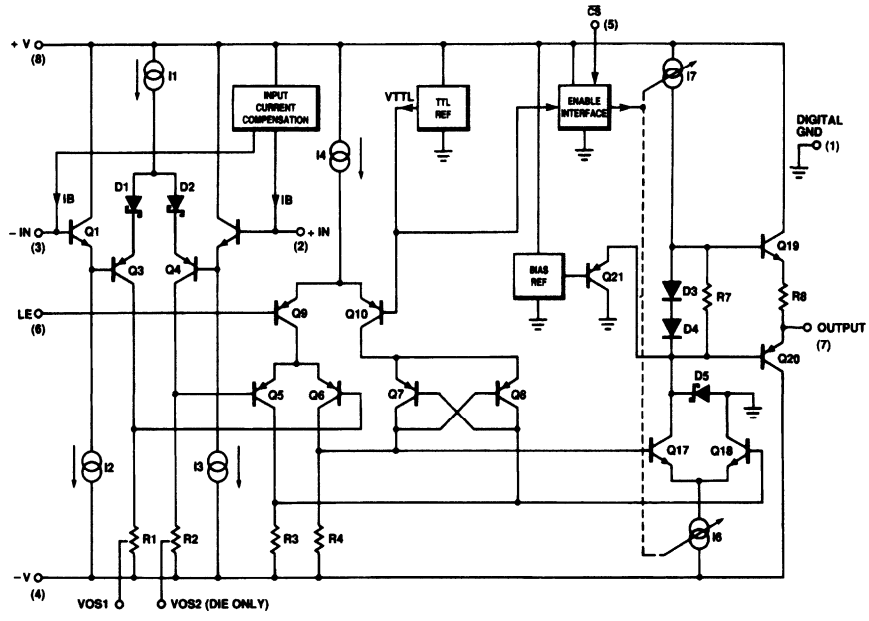


2018-10

V_{IN} Range +12V to −12V
with V_S = ±15V

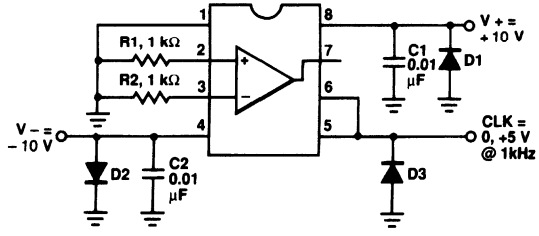
EL2018C
Fast, High Voltage Comparator with Transparent Latch

Equivalent Schematic



2018-11

Burn-In Circuit



2018-12

Pin numbers are for DIP packages.
All packages use the same schematic.

EL2018 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +V
*                   |     |     |     -V
*                   |     |     |     |     LE
*                   |     |     |     |     |     CS
*                   |     |     |     |     |     |     output
*                   |     |     |     |     |     |     |
.subckt M2018       2     3     8     4     6     5     7
*
* Input Stage
*
i1 8 10 700µA
r1 13 4 1K
r2 14 4 1K
q1 8 3 11 qn
q2 8 2 12 qn
q3 13 11 10 qp
q4 14 12 10 qp
i2 11 4 200µA
i3 12 4 200µA
*
* 2nd Stage & Flip Flop
*
*i4 8 24 700µA
i4 8 24 1mA
q9 22 6 24 qp
q10 18 17 24 qp
v1 17 0 2.5V
q5 15 14 22 qp
q6 16 13 22 qp
r3 15 4 1K
r4 16 4 1K
q7 16 15 18 qp
q8 15 16 18 qp
*
* Output Stage
*
i7 8 35 2mA
s1 35 20 5 0 sw
d2 35 8 ds
i6 26 34 5mA
s2 34 4 5 0 sw
d3 34 26 ds
q19 8 20 21 qn 2
q20 4 19 7 qp 2
r8 21 7 60
r7 20 19 4K
q17 19 16 26 qn 5
q18 0 15 26 qn 5
q22 20 20 30 qn 5
```

EL2018C
Fast, High Voltage Comparator with Transparent Latch

EL2018 Macromodel — Contd.

```
q23 19 19 30 qn 8
d1 0 19 ds
q21 0 17 19 qp
*
* Power Supply Current
*
ips 8 4 4mA
*
* Models
*
.model qn npn (is=2e-15 bf=400 tf=0.05nS cje=0.3pF cjc=0.2pF ccs=0.2pF)
.model qp pnp (is=0.6e-15 bf=60 tf=0.3nS cje=0.5pF cjc=0.5pF ccs=0.4pF)
.model ds d(is=2e-12 tt=0.05nS eg=0.62V vj=0.58)
.model sw vswitch (von=0.4V voff=2.5V)
.ends
```

EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Features

- Comparator cannot oscillate
- Fast response—5 ns data to clock setup, 20 ns clock to output
- Wide input differential voltage range—24V on ±15V supplies
- Wide input common mode voltage range—±12V
- Precision input stage—V_{OS} = 1.5 mV
- Low input bias current—100 nA
- Low input offset current—30 nA
- ±4.5V to ±18V supplies
- 3 State TTL compatible output
- No supply current glitch during switching
- 103 dB voltage gain (Low input uncertainty ≈ 30 μV)
- 50% power reduction in shutdown mode
- Input and flip-flop remain active in shutdown mode

Applications

- Analog to digital converters
- ATE pin receiver
- Zero crossing detector
- Window detector
- "Go/no-go" detector

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2019CN	0°C to +75°C	P-DIP	MDP0006

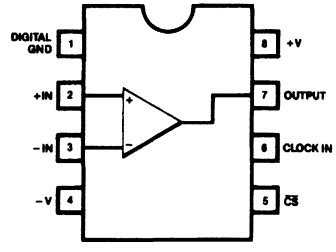
General Description

The EL2019 offers a new feature previously unavailable in a comparator before—a master/slave edge triggered flip-flop. The comparator output will only change output state after a positive going clock edge is applied. Thus the output can't feed back to the input and cause oscillation. Manufactured with Elantec's proprietary Complementary Bipolar process, this device uses fast PNP and NPN transistors in the signal path. A unique circuit design gives the inputs the ability to handle large common mode and differential mode signals, yet retain high speed and excellent accuracy. Careful design of the front end insures speed and accuracy when operating with a mix of small and large signals. The three-state output stage is designed to be TTL compatible for any power supply combination, yet it draws a constant current and does not generate current glitches. When the output is disabled, the supply current consumption drops by 50%, but the input stage and master slave flip-flop remain active.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, see QRA1: *Elantec's Processing-Monolithic Products.*

Connection Diagrams

8-Pin Plastic DIP



Top View

EL2019C

Fast, High Voltage Comparator with Master Slave Flip-Flop

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	I_O	Continuous Output Current	25 mA
V_{IN}	Input Voltage	$+V_S$ to $-V_S$	T_A	Operating Temperature Range	0°C to +75°C
ΔV_{IN}	Differential Input Voltage	Limited only by Power Supplies	T_J	Operating Junction Temperature	150°C
			T_{ST}	Storage Temperature	−65°C to +150°C
I_{IN}	Input Current (Pins 1, 2 or 3)	±10 mA		Lead Temperature	
I_{INS}	Input Current (Pins 5 or 6)	±5 mA		(Soldering, 5 seconds)	300°C
P_D	Maximum Power Dissipation (Note 3 - See Curves)	1.25W			
I_{OP}	Peak Output Current	50 mA			

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, unless otherwise specified

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
V_{OS}	Input Offset Voltage	25°C		1.5	5	I	mV
	V_{CM} = 0V, V_O Transition Point	T_{MIN}, T_{MAX}			7	III	mV
I_B	Input Bias Current	25°C		±100	±300	I	nA
	V_{CM} = 0V, Pin 2 or 3	T_{MIN}, T_{MAX}			±500	III	nA
I_{OS}	Input Offset Current	25°C		30	150	I	nA
	V_{CM} = 0V	T_{MIN}, T_{MAX}			250	III	nA
CMRR	Common Mode Rejection Ratio (Note 1)	25°C	75	90		I	dB
PSRR	Power Supply Rejection Ratio (Note 2)	25°C	75	95		I	dB
V_{CM}	Common Mode Input Range	25°C	±12	±13		I	V
		T_{MIN}, T_{MAX}	±12			III	V
V_{uncer}	Input Uncertainty Range			30		V	μV/RMS
V_{OL}	Output Voltage Logic Low	25°C	−0.05	0.15	0.4	I	V
	I_{OL} = 8 mA and I_{OL} = 0 mA)	T_{MIN}, T_{MAX}	−0.1		0.4	III	V
V_{OH}	Output Voltage Logic High						
	V_S = ±15V	25°C	3.5	4.0	4.65	I	V
	V_S = ±15V	T_{MIN}, T_{MAX}	3.5		4.65	III	V
	V_S = ±5V	25°C	2.4			I	V
	V_S = ±5V	T_{MIN}	2.4			III	V
	V_S = ±5V	T_{MAX}	2.4			III	V

DC Electrical Characteristics $V_S = \pm 15V$, unless otherwise specified — Contd.

Parameter	Description	Temp	Limits			Test Level	Units
			Min	Typ	Max		
V_{ODIS1}	V_{OUT} Range, Disabled, $I_{OL} = -1$ mA						
	$V_S = \pm 15V$	25°C	4.65			I	V
	$V_S = \pm 15V$	T_{MIN}, T_{MAX}	4.65			III	V
	$V_S = \pm 5V$	25°C		3.65		V	V
V_{ODIS2}	V_{OUT} Range, Disabled, $I_{OL} = +1$ mA $V_S = \pm 5V$ to $+15V$	All	−0.3	−1		II	V
V_{INH}	Clock or $\overline{CS}$ Inputs	25°C	2			I	V
	Logic High Input Voltage	T_{MIN}, T_{MAX}	2			III	V
I_{IN}	Clock or $\overline{CS}$ Inputs Logic Input Current $V_{IN} = 0V$ and $V_{IN} = 5V$	25°C			±200	I	μA
		T_{MIN}, T_{MAX}			±300	III	μA
V_{INL}	Clock or $\overline{CS}$ Inputs Logic Low Input Voltage	25°C			0.8	I	V
		T_{MIN}, T_{MAX}			0.8	III	V
I_{S+EN}	Positive Supply Current Enabled	25°C		8.8	11	I	mA
		T_{MIN}, T_{MAX}			12	II	mA
I_{S+DIS}	Positive Supply Current Disabled	25°C		4.9	6	I	mA
		T_{MIN}, T_{MAX}			7	II	mA
I_{S-EN}	Negative Supply Current Enabled	25°C		14.5	17	I	mA
		T_{MIN}, T_{MAX}			18	II	mA
I_{S-DIS}	Negative Supply Current Disabled	25°C		6.4	8.0	I	mA
		T_{MIN}, T_{MAX}			8.0	II	mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = 25°C$

Parameter	Description	Limits			Test Level	Units
		Min	Typ	Max		
T_S	Setup Time 5 mV Overdrive		12	20	II	ns
T_H	Hold Time		−3	0	IV	ns
T_{OPOUT}	Clock to Output Delay		20	25	IV	ns
T_{OPMIN}	Minimum Clock Width		7		V	ns
T_{EN}	Output 3-State Enable Delay		40	70	IV	ns
T_{DIS}	Output 3-State Disable Delay		150	300	IV	ns

Note 1: $V_{CM} = +12V$ to $-12V$.

Note 2: $V_S = \pm 5V$ to $\pm 15V$.

Note 3: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the Typical Performance curves for more details.

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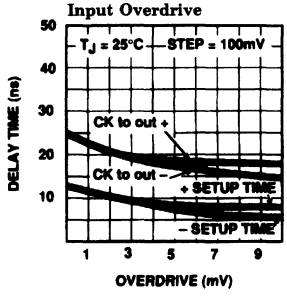
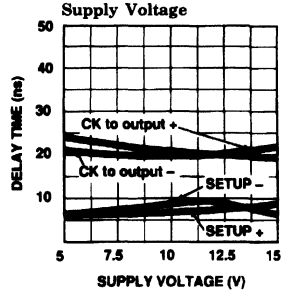
EL2019C
Fast, High Voltage Comparator with Master Slave Flip-Flop

Typical AC Performance Curves

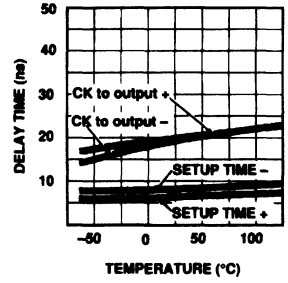
Delay Time vs
Input Overdrive



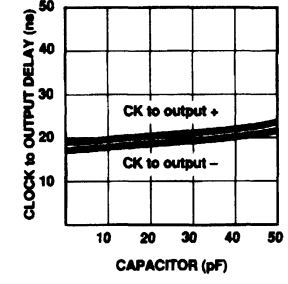
Delay Time vs
Supply Voltage



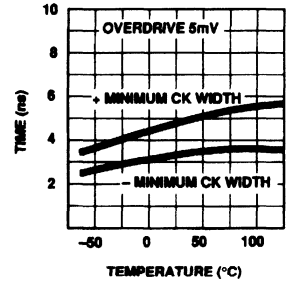
Delay Time vs
Temperature



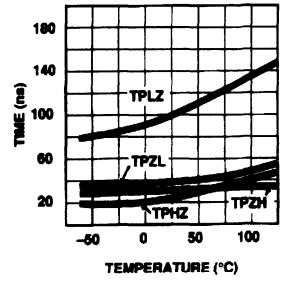
Clock to Output Delay
vs Load Capacitor



Minimum Clock Width
vs Temperature



Enabled/Disabled Times
vs Temperature



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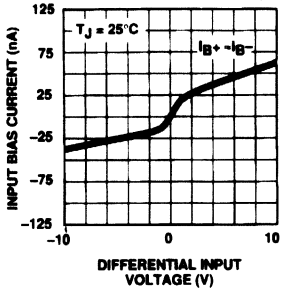
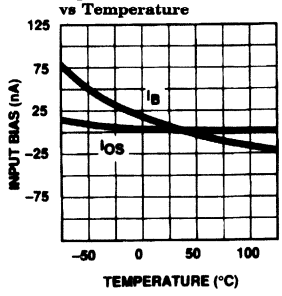
Typical AC Performance Curves — Contd.

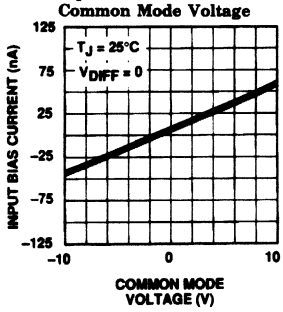
Input Bias Current vs Differential Input Voltage



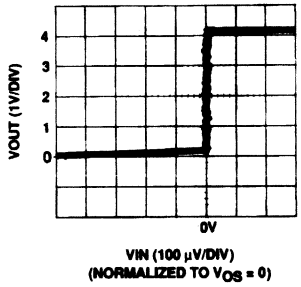
Input Bias Current vs Temperature



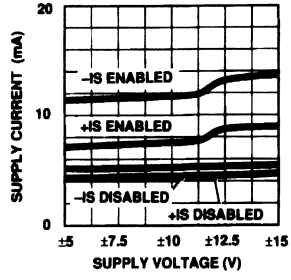
Input Bias Current vs Common Mode Voltage



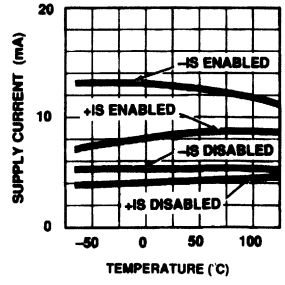
V_O/V_I Transfer Characteristics



Supply Current vs Supply Voltage



Supply Current vs Temperature



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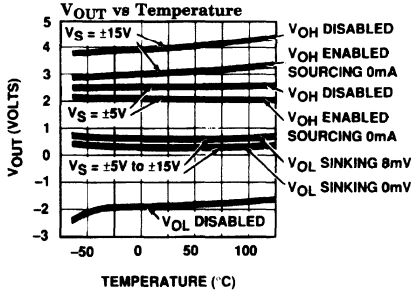
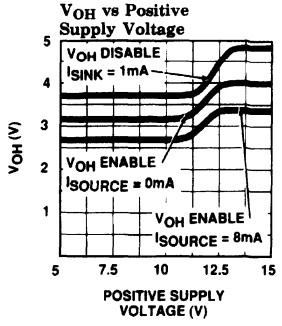
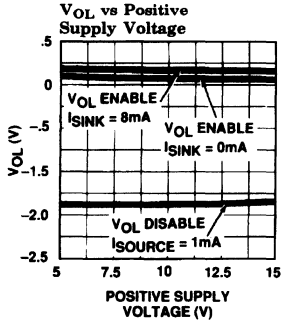
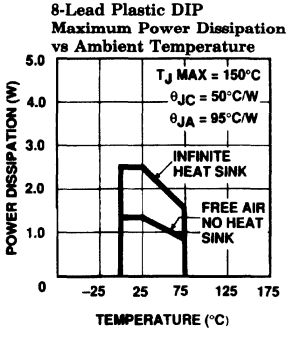
EL2019C
Fast, High Voltage Comparator with Master Slave Flip-Flop

Typical AC Performance Curves — Contd.









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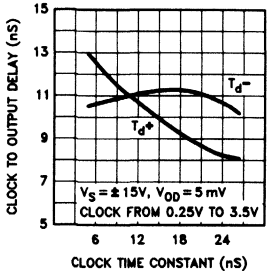
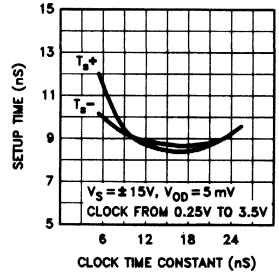
Typical AC Performance Curves — Contd.

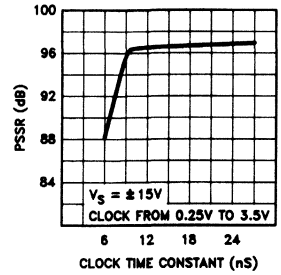
Clock to Output Delay vs Clock Time Constant



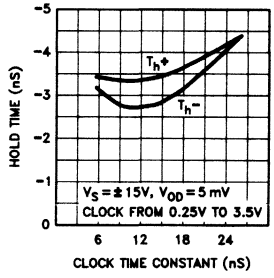
Set-up Time vs Clock Time Constant



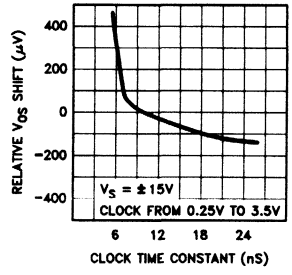
PSRR vs Clock Time Constant



Hold Time vs Clock Time Constant



Relative V_{OS} Shift vs Clock Time Constant



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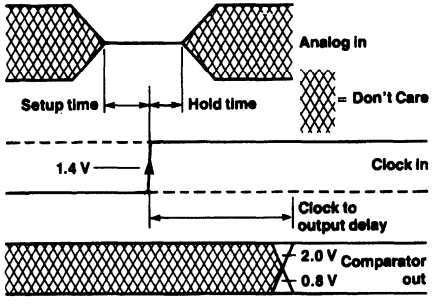
EL2019C
Fast, High Voltage Comparator with Master Slave Flip-Flop

Timing Diagram



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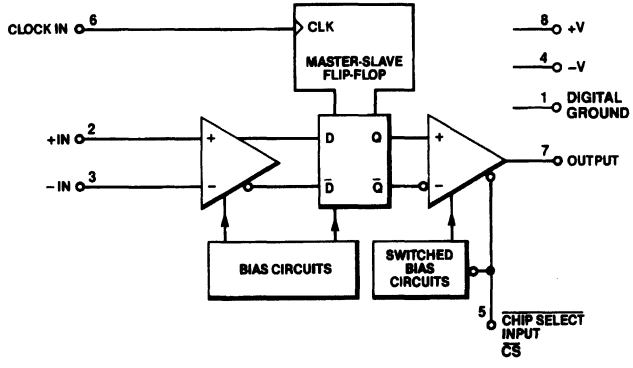
Note: Since the hold time is negative the input is a don't care at the clock time. This ensures that clock noise will not affect the measurement.

Block Diagram



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Function Table

Inputs (Time n−1)				Internal Q (Time n)	Notes	Output (Time n)
+IN	−IN	$\overline{CS}$	CLK			
+	−	L	↓	H	Normal Comparator Operation	H
−	+	L	↓	L	With "D" Flip-Flop	L
+	−	H	↓	H	Normal Comparator Operation	High Z
−	+	H	↓	L	With "D" Flip-Flop; Power Down Mode	High Z
X	X	L	H	Qn−1	Data Retained in Flip-Flop	Qn−1
X	X	L	L	Qn−1	Data Retained in Flip-Flop	Qn−1
X	X	L	↓	Qn−1	Data Retained in Flip-Flop	Qn−1
X	X	H	H	Qn−1	Data Retained in Flip-Flop, Output Power Down Mode	High Z
X	X	H	L	Qn−1	Data Retained in Flip-Flop, Output Power Down Mode	High Z
X	X	H	↓	Qn−1	Data Retained in Flip-Flop, Output Power Down Mode	High Z

Application Hints

Device Overview

The EL2019 is the first comparator of its kind. It is capable of 24V differential signals, yet has excellent accuracy, linearity and voltage gain. The EL2019 has an internal master/slave flip-flop between the input and output. It even has a 3-state output feature that reduces the power supply currents 50% when the output is disabled, yet the input stage and latch remain active. This extremely fast and accurate device is built with the proprietary Elantec Complementary Bipolar Process, which is immune to power sequencing and latch up problems.

Power Supplies

The EL2019 will work with ±5V to ±18V supplies or any combination between (Example +12V and −5V). The supplies should be well bypassed with good high frequency capacitors (0.01 μF monolithic ceramic recommended) within ¼ inch of the power supply leads. Good ground plane construction techniques improve stability, and the lead from pin 1 to ground should be short.

Front End

The EL2019 uses schottky diodes to make a "bullet proof" front end with very low input bias currents, even if the two inputs are tied to very large differential voltages (±24V).

The large common mode range (±12V minimum) and differential voltage handling ability (±24V min.) of the device make it useful in ATE applications without the need for an input attenuator with its associated delay.

Recovery from Large Overdrives

Timing accuracy is excellent for all signals within the common mode range of the device (±12V with ±15V supply). When the common mode range is exceeded the input stage will saturate, input bias currents increase and it may take as much as 200 ns for the device to recover to normal operation after the inputs are returned to the common mode range. If signals greater than the common mode range of the device are anticipated, the inputs should be diode clamped to remain within the common mode range of the device, or the supply voltage be raised to encompass the input signal in the common mode range.

Input Slew Rate

All comparators have input slew rate limitations. The EL2019 operates normally with any input slew rate up to 300 V/μs. Input signal slew rates over 300 V/μs induce offset voltages of 5 mV to 20 mV. This induced offset voltage settles out in about 20 ns, 20 times faster than previous high voltage comparators. This shows up as an increased set-up time.

Master Slave Flip-Flop

The built-in Master/Slave Flip-Flop only allows the output to change when a positive edge is received on the clock input. This feature has some major benefits to the user. First, the device cannot oscillate due to feedback from the output to the inputs. Second, the device *must* make a decision when it receives a clock input, and the difference between deciding on a "0" or a "1" is limited only by the input circuit noise, both internal and external to the EL2019. With low impedance sources and a good layout this uncertainty can be less than 30 μV/RMS. Since a 30 μV change on the input can cause a 4V change on the output this works out to an effective gain of 103 dB, more than adequate for a 16-bit analog to digital converter.

The hold time of the EL2019 is worst case 0 ns, and typically −3 ns. This means that the analog signal is sampled typically 3 ns *before* the clock time and, worst case, concurrent with the clock.

The EL2019 is sensitive to a large clock edge rates. More than a 500 V/μs edge rate at the clock input will induce V_{OS} shifts, reduce PSRR, and cause the device to operate incorrectly at low temperatures and low supply voltages. A good method to control the clock edge rate is to place a resistor in series and a capacitor to ground in parallel with the clock input. Generally, any time constant 10 ns or greater will suffice.

Elantec tests the EL2019 with a nominal 20 ns time constant, using a series 330Ω resistor and 61 pF of capacitance to ground (including strays). All clocks are generated by Schottky TTL and have a 0.25V to 3.5V swing.

EL2019C
Fast, High Voltage Comparator with Master Slave Flip-Flop

Application Hints — Contd.

Output Stage

The output stage of the EL2019 is a pair of complementary emitter followers operating as a linear amplifier. This makes the output stage of the EL2019 glitch free, and improves accuracy and stability when operating with small signals.

3-State Output, Power Saving Feature

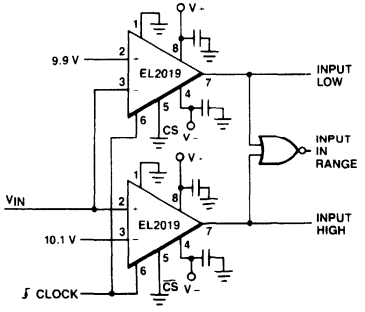
The EL2019 has an output stage which can be put into a high impedance "3-state" mode. When it is in this mode, the input stage and latch remain active, yet the device dissipates only 50% of the power used when the output is active. This has advantages in large ATE systems where there may be 1000 comparators, but only 10% are in use at any one time.

The EL2019 will work properly with the chip select input (pin 5) floating, however, good R.F. technique would be to ground this input if it is not used.

Due to the power saving feature and linear output stage, the EL2019 does not have a standard TTL 3-state output stage. As such one must be careful when using the 3-state feature with devices other than other EL2018's or EL2019's. When operating from ±15V supplies the 3-state feature is compatible with all TTL families, however CMOS families may conflict on high outputs. Since the output stage of the EL2019 turns on faster than it turns off, a 50Ω to 100Ω resistor in series with the output will limit fault currents between devices with minimum impact on logic drive capability.

Typical Applications

A Wide Input Range Window Comparator



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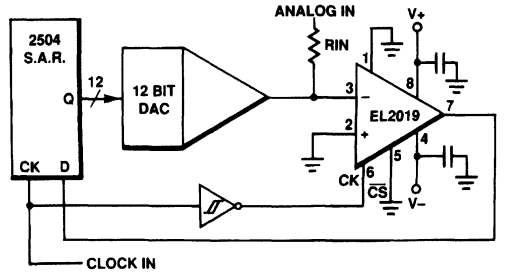
(V_{IN} Range +12V to −12V with V_S = ±15V)

The EL2019 makes an excellent comparator in most analog to digital converters, due to its high gain and fast response. Most 2504 based A to D designs can be modified to use the EL2019 simply by using an inverted clock to the EL2019 as shown below. This results in improved performance due to less jitter of the transition voltages.



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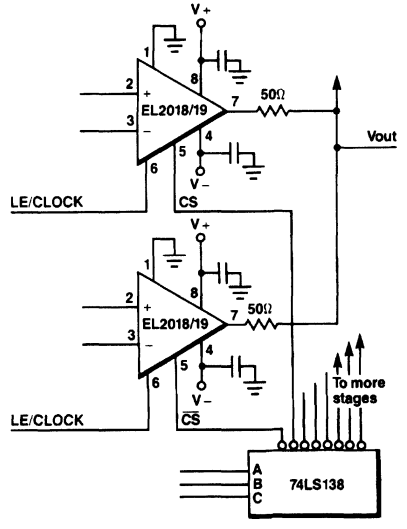
Using the Power Down/ 3-State Feature



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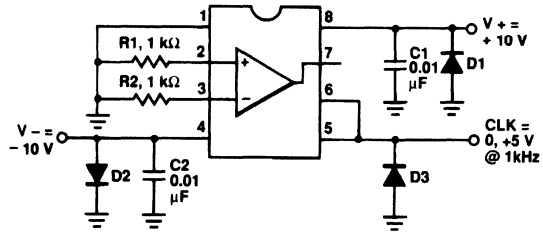
EL2019C
Fast, High Voltage Comparator with Master Slave Flip-Flop

Burn-In Circuit



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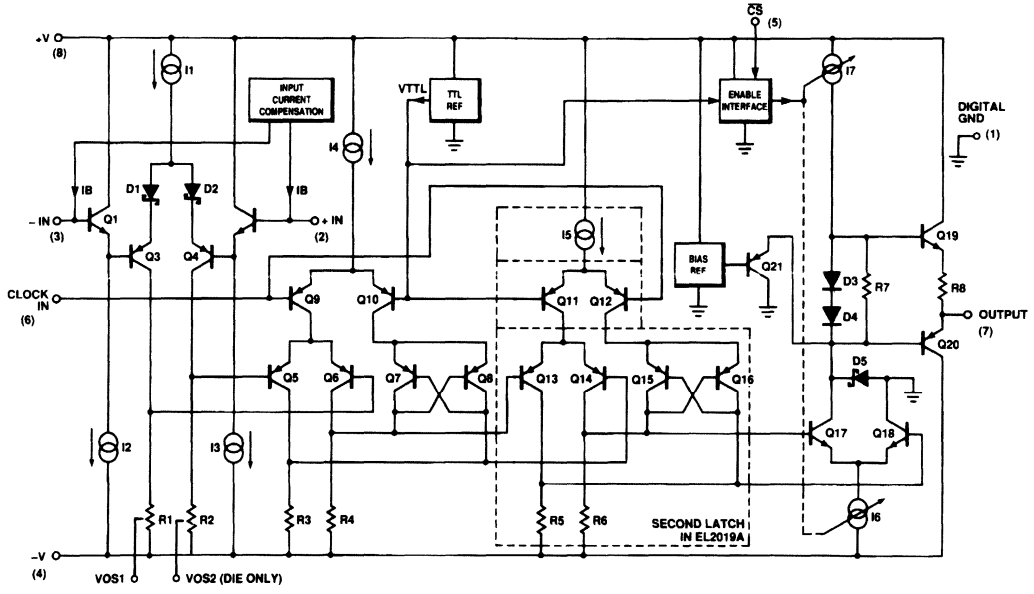
Pin numbers are for DIP packages. All packages use the same schematic.

Equivalent Schematic



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EL2019C
Fast, High Voltage Comparator with Master Slave Flip-Flop

EL2019 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +V
*                   |     |     |     -V
*                   |     |     |     |     Cpin
*                   |     |     |     |     |     CS
*                   |     |     |     |     |     |     output
*                   |     |     |     |     |     |     |
.subckt M2019       2     3     8     4     6     5     7
*
* Input Stage
*
i1 8 10 700µA
r1 13 4 1K
r2 14 4 1K
q1 8 3 11 qn
q2 8 2 12 qn
q3 13 11 10 qp
q4 14 12 10 qp
i2 11 4 200µA
i3 12 4 200µA
*
* 2nd Stage & Flip Flop
*
*i4 8 24 700µA
i4 8 24 1mA
q9 22 6 24 qp
q10 18 17 24 qp
v1 17 0 2.5V
q5 15 14 22 qp
q6 16 13 22 qp
r3 15 4 1K
r4 16 4 1K
q7 16 15 18 qp
q8 15 16 18 qp
i5 8 40 500µA
q11 41 17 40 qp
q12 42 6 40 qp
q13 43 16 41 qp
q14 44 15 41 qp
q15 44 43 42 qp
q16 43 44 42 qp
r5 43 4 1K
r6 44 4 1K
*
* Output Stage
*
i7 8 35 2mA
s1 35 20 5 0 sw
d2 35 8 ds
i6 26 34 5mA
```

EL2019 Macromodel — Contd.

```
s2 34 4 5 0 sw
d3 34 26 ds
q19 8 20 21 qn 2
q20 4 19 7 qp 2
r8 21 7 60
r7 20 19 4K
q17 19 44 26 qn 5
q18 0 43 26 qn 5
q22 20 20 30 qn 5
q23 19 19 30 qn 8
d1 0 19 ds
q21 0 17 19 qp
*
* Power Supply Current
*
ips 8 4 4mA
*
* Models
*
.model qn npn (is = 2e - 15 bf = 400 tf = 0.05nS cje = 0.3pF cjc = 0.2pF ccs = 0.2pF)
.model qp pnp (is = 0.6e - 15 bf = 60 tf = 0.3nS cje = 0.5pF cjc = 0.5pF ccs = 0.4pF)
.model ds d(is = 2e - 12 tt = 0.05nS eg = 0.62V vj = 0.58)
.model sw vswitch (von = 0.4V voff = 2.5V)
.ends
```

Disk Drive VCM Drivers

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Elantec Disk Drive Servo Amplifiers

Elantec Part Number	Description	Continuous Output Current Drive	Voltage Swing Across Load	Power Supply Voltage Range	Operating Mode	Packages
EL2037AC	Monolithic Voice Coil Driver with Auto Head Park— 5¼" Drives	25 mA Min (Drive for External Transistors)	11.25V Typ (±12V Supply)	+10V to +13V	Linear Class AB	20-Pin P-DIP 20-Pin SOL
EL3038C	Monolithic Voice Coil Driver with Auto Head Park— Disable Current Sense Amplifier	35 mA NPN Drive 40 mA PNP Drive	11.25V Typ (12V Supply)	+10V to +13.5V	Linear Class AB	20-Pin SOL

EL2037AC
Servo Motor Driver

Features

- No crossover distortion
- Low output offset current
- Maximum output swing
- Programmable park voltage
- Programmable transconductance
- Programmable bandwidth
- Chip enable function
- Drive low cost bipolar transistors
- Single sense resistor
- Minimum external components
- Small surface mount package

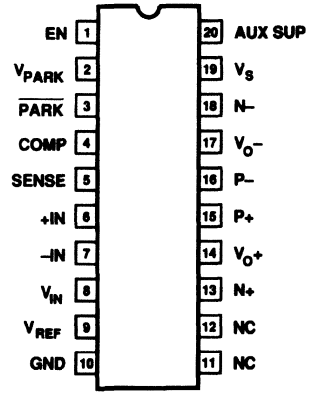
Applications

- Voice coil motor servo systems
- Winchester disk drives
- Optical disk drives
- Super floppy drives
- DC motor control

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2037ACM	−25°C to +85°C	SOL-20	MDP0027

Connection Diagram



2036-1

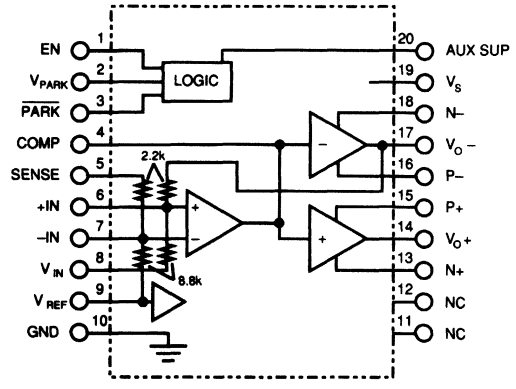
General Description

The EL2037AC is a servo motor driver circuit designed to drive voice coil motors in disk drive applications. These second generation circuits contain more features, have improved accuracy, and are lower in cost compared to earlier generation circuits. The EL2037AC drives an H bridge consisting of four low-cost external bipolar power transistors for maximum output swing. Crossover distortion is eliminated by Class AB biasing of the output devices with a unique patent pending temperature-stable circuit that never needs adjustment.

System accuracy is improved by using one external current sense resistor in series with the motor. Compared to conventional grounded resistor circuits, the EL2037AC has inherent positive to negative gain matching and no gain error due to transistor alpha. All of the critical bias voltages use the same V_{REF} voltage. This reduces the output offset current to less than 5 mA.

In addition to an enable logic input, a "park" logic input has been provided which programs a voltage across the motor to park the head when power is removed. The power for this function comes from a separate supply generated by the back EMF of the spindle motor used as a generator. The EL2037AC requires back EMF of 3.5V minimum.

Block Diagram



2036-2

Manufactured under U.S. Patent No. 4,910,477, 4,878,034, 4,935,704 and 4,963,802.

EL2037AC
Servo Motor Driver

Absolute Maximum Ratings

V_S	Supply Voltage, Pin 19	−0.3V to +18V	T_A	Operating Temperature Range	−25°C to +85°C
V_{AUX}	Auxiliary Supply Voltage, Pin 20	V_S −1V to +18V		Lead Temperature	
V_{LIM}	Short Circuit Limit Sense Voltage	V_S −0.3V to +18V		SOL Package	300°C
V_{IN}	Logic Inputs, Pins 1 and 3	−0.3V to +7V		Vapor Phase (60 seconds)	215°C
	Signal Inputs, Pins 8 and 9	−0.3V to +7V		Infrared (15 seconds)	220°C
I_{IN}	Input Current, Pins 1, 3, 8, and 9	10 mA	T_{ST}	Storage Temperature	−65°C to +150°C
T_J	Junction Temperature	150°C	P_D	Power Dissipation, T_A = 25°C	
				SOL Package	1.50W

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

$T_A = T_J$ = 25°C, V_S = 12V, V_{REF} = 5V, R_s = 0.25Ω, Load = 10Ω. See test circuits

Parameter	Description	Min	Typ	Max	Test Level	Units
Enabled Mode, Pin 1 = H. Pin 3 = H. (Note 1)						
I_{OS}	Output Offset Current	−5	0.6	5	I	mA
G_{M1}	Transconductance, I_{OUT} = ±100 mA	0.95	1	1.05	I	A/V
G_{M2}	Transconductance, I_{OUT} = ±1A	0.93	1	1.07	I	A/V
I_{ST}	Quiescient Supply Current, Total		20		V	mA
I_{Q1}	Quiescient Supply Current, Pin 19		10	14	I	mA
I_{Q2}	Auxiliary Supply Quiescient Current, Pin 20	1	5	7	I	mA
I_{QE}	External Transistor Quiescient Current	2	8	12	I	mA
I_{DN}	NPN Drive Current, Pin 13 or 18	25	35		I	mA
I_{DP}	PNP Drive Current, Pin 15 or 16	25	35		I	mA
I_{IB}	Input Bias Current. $V_{IN} = V_{REF}$ = 2.5V, 6.5V	−250	50	250	I	µA
I_{IA}	Active Input Current. V_{IN} = 0.5V, V_{REF} = 2.5V	−1.5	−1.1		I	mA
I_{IA}	Active Input Current. V_{IN} = 4.5V, V_{REF} = 2.5V		0.4	0.7	I	mA
I_{RB}	Reference Bias Current. $V_{IN} = V_{REF}$ = 2.5V, 6.5V	−250	50	250	I	µA
I_{RA}	Active Reference Current. V_{IN} = 0.5V, V_{REF} = 2.5V	−1.5	−0.9		I	mA
I_{RA}	Active Reference Current. V_{IN} = 4.5V, V_{REF} = 2.5V		0.2	0.5	I	mA
V_S	Supply Voltage Range, Pin 19	11	12	13	IV	V
VRR	Reference Voltage Range, Pin 9	2.5		6.5	I	V
RRR	Reference Voltage Rejection, 2.5V to 6.5V		0.3	1	I	mA/V
PSR	Power Supply Rejection, 11V to 13V		0.3	1	I	mA/V
THD	Total Harmonic Distortion, V_{IN} = 20 mV_{PP}, 1 kHz		0.5	1	I	%

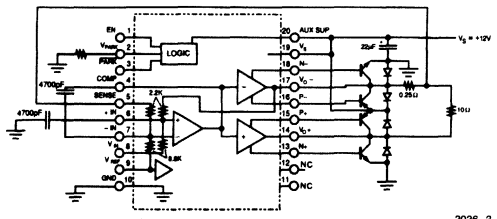
Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = 12V$, $V_{REF} = 5V$, $R_s = 0.25\Omega$, Load = 10Ω. See test circuits — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
Park Mode. Pin 1 = H. Pin 3 = L. Aux Supply (Pin 20) = 6V (Note 1) R_{PARK} = 3k						
V_{P1}	V_{OUT} ($V_O^+ - V_O^-$)	−0.40	−0.50	−0.60	I	V
V_{AR}	Aux Supply Range, EL2037AC ($-0.25V \le V_{OUT} \le -0.65V$)	3.5	6	12	I	V
I_{PD}	NPN Drive. Pin 13	2	3		I	mA
I_{AUX}	Short Circuit Maximum Current (Pin 17 = 0V)		250		V	mA
Disabled Mode. Pin 1 = L. Pin 3 = H. (Note 1)						
I_{OD}	Output Current	−200	10	200	I	µA
R_{OD}	Output Resistance. I_{OUT} ±1 mA	1	3		I	kΩ
I_{SD}	Total Supply Current, Pin 12, 19, and 20 + Transistors		10	14	I	mA
Logic Inputs						
V_{IL}	Low Level Input Voltage for a Valid Low			0.8	I	V
I_{IL}	Low Level Input Current, Logic = 0V	−20	−10	10	I	µA
V_{IH}	High Level Input Voltage for a Valid High	2			I	V
I_{IH}	High Level Input Current, Logic = 5V	−150	10	150	I	µA
Individual Amplifiers						
A_V	Power Amplifier Voltage Gain	10.5	11.5	12.5	I	V/V

Note 1: Logic Level L = 0.8V, Logic Level H = 2.0V

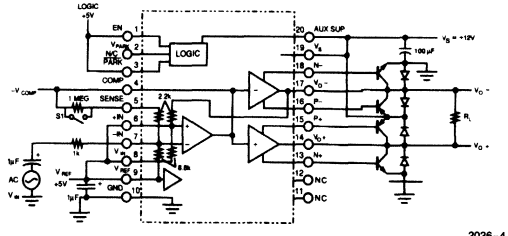
DC and Closed Loop AC Test Circuit



2036-3

NPNs are MJE200.
PNPs are MJE210.
Diodes are 1 Amp IN4000.

Open Loop AC Test Circuit



2036-4

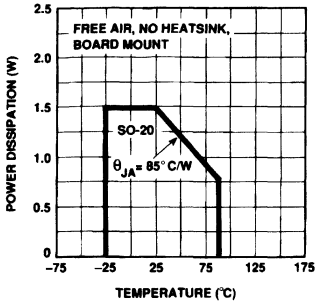
Op Amp Gain—S1 Open, $A_V = \frac{V_{COMP}}{V_{IN}}$

Power Amp Gain—S1 Closed, $A_V = \frac{(V_O+)-(V_O-)}{V_{COMP}}$

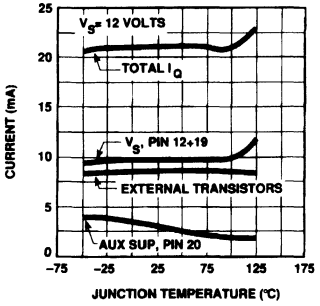
EL2037AC
Servo Motor Driver

Typical Performance Curves

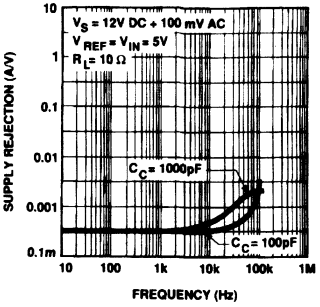
Maximum Power Dissipation vs Ambient Temperature



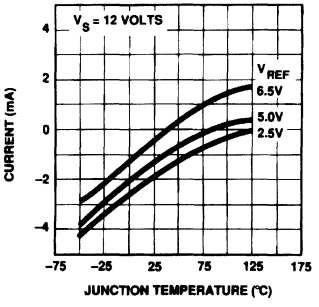
Quiescent Current vs Temperature



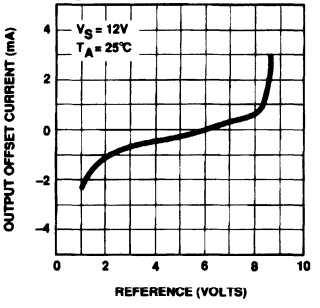
Supply Rejection vs Frequency



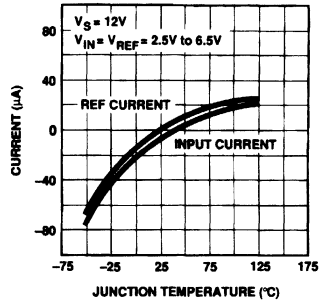
Output Offset Current vs Temperature



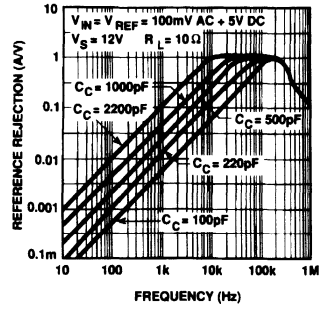
Output Offset Current vs Reference Voltage— Typical Unit



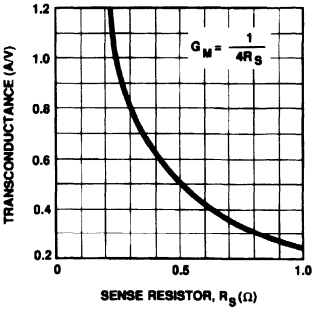
Reference and Input Bias Current vs Temperature



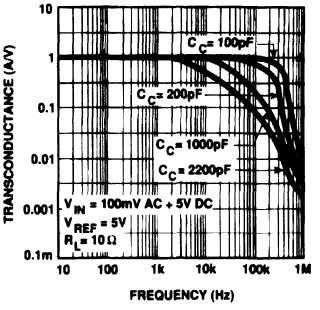
Reference Voltage Rejection vs Frequency



Transconductance vs Sense Resistor



Transconductance vs Frequency



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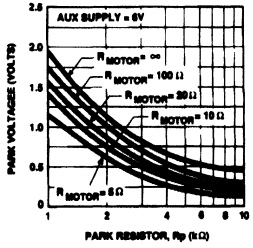
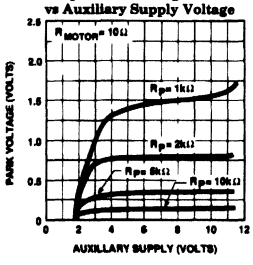
Typical Performance Curves — Contd.

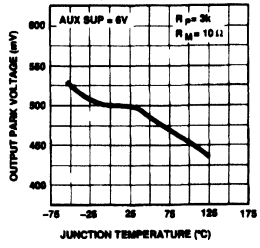
EL2037AC
Output Park Voltage
vs Park Resistor



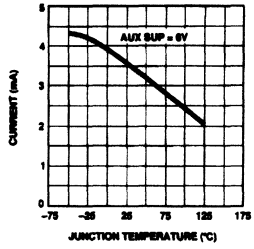
EL2037AC
Output Park Voltage
vs Auxiliary Supply Voltage



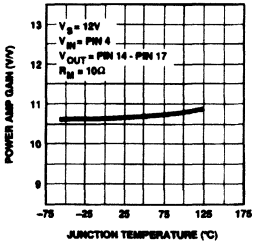
EL2037AC
Output Park Voltage
vs Temperature



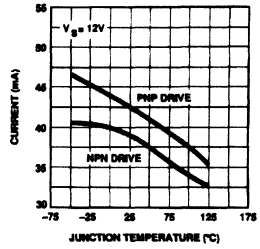
NPN Base Drive During
Park vs Temperature



Power Amplifier Gain
vs Temperature



Power Amplifier Drive
Current vs Temperature



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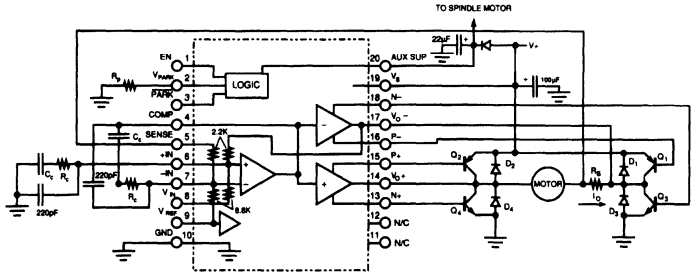
7

EL2037AC
Servo Motor Driver

Typical Application



2036-7

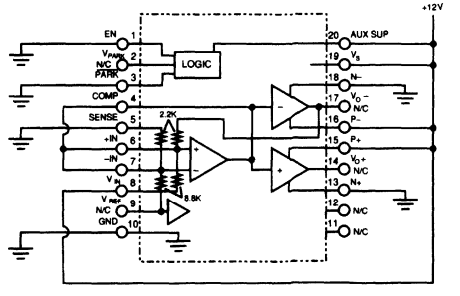
External Components

Parameter	Description	Min	Typ	Max	Units	Typical ± % Tolerance
R_P	Sets the Motor Voltage During PARK Mode, EL2036AC	0.5k	1.5k	Open	Ω	5
R_P	Sets the Motor Voltage During PARK Mode, EL2037AC	1k	3k	Open	Ω	5
R_s	Current Sense Resistor	0.1	0.25	1	Ω	2
C_c	Loop Compensation. Sets dominant pole	100	2000	0.1 μF	pF	5
R_c	Loop Compensation. Makes a Zero, Equal to Motor Pole	0	10	200	kΩ	5
C_d	Short Circuit Delay Capacitor	0.05	1	100	μF	10
D1–4	Catch diodes, 1 amp	1N4000				
Q1, 2 Q3, 4	PNP Power Transistors. Min H_{FE} = 40 NPN Power Transistors. Min H_{FE} = 40 $R_P \approx$ 1.4k/Park motor voltage for EL2037C C_d = Delay/250k R_s = 1/(4*DC transimpedance)	MJE210 or D45H11 MJE200 or D44H11				

Truth Table

Enable (Pin 1)	Park (Pin 3)	Output
>2.0V	>2.0V	Normal Operation
<0.8V	>2.0V	Disabled
X	<0.8V	Parking Mode
X	X	Disabled for Delay

Burn-In Circuit



2036-8

Circuit Description

The EL2037AC is a transconductance amplifier especially well-suited to driving voice coil motors in disk drives. The EL2037AC consists of four main blocks. These four functions are a low offset voltage operational amplifier, a single-ended input to differential output power amplifier, a logic circuit and a park circuit.

The operational amplifier and power amplifier together with four well-matched internal resistors make the basic transconductance amplifier. The logic circuit enables the amplifiers and the park circuit.

The Operational Amplifier

The operational amplifier is a low offset design with modest gain and excellent common mode rejection over a wide range that includes ground. This ensures proper operation when the motor voltage exceeds the supply or ground and is clamped by the catch diodes. The operational amplifier is internally compensated for stable operation at all times. The gain bandwidth product is 2 MHz and the phase margin is 60° at unity gain. The operational amplifier has internal clamps to limit its output swing to about ±2V of the reference voltage. The clamps are not shown in the simplified schematic and their only function is to prevent overcharging of the compensation capacitor during transients. The operational amplifier output is disabled by the logic circuit when either pin 1 or pin 3 is low.

Op Amp Open Loop
Gain and Phase vs Frequency

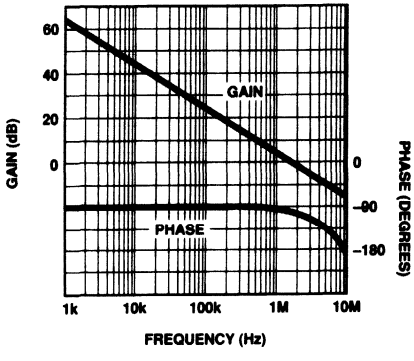


Figure 1

The Power Amplifier

The power amplifiers of the EL2037AC are made of two identical stages that take a single-ended input and drive the motor differentially. The reference is buffered and the outputs of both stages are biased from the buffered reference voltage to reduce output offset current. Each stage has feedback for linearity and gain accuracy. One stage operates noninverting and the other inverting, resulting in a total gain of 11. The feedback is more complicated than shown in the simplified schematic, to ensure accurate gain even when one amplifier saturates before the other. The bandwidth of the power amplifier is about 500 kHz as shown below.

External power transistors deliver the power to the motor to optimize the output swing capability and eliminate power dissipation concerns. A unique biasing circuit eliminates low-level crossover distortion by biasing the transistors on at a few mA. The amplifier outputs are disabled when either pin 1 or pin 3 is low.

Power Amplifier Gain and
Phase vs Frequency

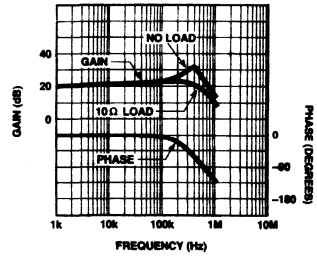


Figure 2

EL2037AC
Servo Motor Driver

The Logic Circuit

The logic circuit operates from a separate supply called the auxiliary supply. In a typical disk drive application, the auxiliary supply is usually within a diode drop of the normal supply, except when the normal supply is interrupted. Then the auxiliary supply is generated from the back EMF of the spindle motor. By having two supplies, the logic circuit can operate for a while after the main power has been removed.

There are two external inputs to the logic circuit, and one internal. The external inputs are enable and park-bar; the internal input is from the short circuit protection. The external inputs are TTL compatible and can be driven by CMOS gates. The internal short circuit protection input overrides the two external inputs. The park-bar input overrides the enable input when it is low. Note that when left open, the external inputs generate a logic low. Therefore, if the logic inputs are removed, the EL2037AC goes into park mode.

The Park Circuit

When the park-bar logic input is high, the park circuit is disabled and has no effect on the motor. When the park-bar logic input is low, the amplifiers are disabled and the park circuit is activated. Like the logic circuit, the park circuit uses the auxiliary supply, not the main supply. The park circuit sets the base of Q65 (the transistor whose emitter is pin 2) to about 2V. The value of the external resistor from pin 2 to ground, R_P, determines the current in the collector of the Q65 transistor. That current is mirrored and generates a voltage as it flows through two diodes, an internal resistor and a saturated transistor, Q68. The voltage is applied to the base of a darlington that drives $V_{OUT}-$, pin 17. At the same time, a current is sent to the base of the opposite output NPN transistor, pin 13. This saturates the external output NPN transistor. The voltage across the motor is now independent of the auxiliary supply voltage at pin 20 and is an inverse function of the resistor R_P.

Applications Information

Transconductance

The DC transconductance of the EL2037AC is set by one resistor, R_s, that senses the motor current. The input voltage is the difference between the voltage on pin 8 and 9. When pin 8 is more positive than pin 9, the input is said to be positive. When the input is positive, the voltage on pin 14 is more positive than pin 17 and the motor current is said to be positive. The DC transconductance is given by the simple equation:

$$G_{MO} = \frac{1}{4R_s} = \frac{I_O}{V_{IN}-V_{REF}}$$

For a transconductance of 1 Amp per volt, the sense resistor, R_s, should equal 0.25Ω. Because the sense resistor is very small, care should be taken to insure that the PC board trace resistance does not increase its value. The connections from pin 5 and 17 are the "sense" connections while the motor and transistor collectors are the "force" connections. Therefore, the connections from pin 5 and pin 17 should go directly to the sense resistor.

Source Impedance

The input and reference source impedances should be low to prevent gain and offset errors. The input current is determined by the internal feedback resistors and the input and output voltages. The worst case current flows when the reference is low and the input is lower and therefore the V_O- output is high. This condition is tested and the input and reference currents are guaranteed to be less than 1.5 mA. Therefore, the input and reference should be able to sink and source

Applications Information — Contd.

1.5 mA. For the typical case where the transconductance is 1 Amp per volt, a source impedance of less than 10Ω will generate less than 2.5 mA of additional output offset current and less than 1.5% gain error. Obviously, if the output of an operational amplifier drives the EL2037AC there will be no errors due to source impedance. Be careful with some single supply operational amplifiers (324 and 358 types). They require output loading to ground to eliminate their high output impedance and crossover distortion.

Transistors

The EL2037AC will drive almost any pair of complementary transistors. The output transistor drive is guaranteed to be 25 mA. The required maximum output current divided by 25 mA gives the minimum H_{FE} required. For 1 Amp output current, the minimum H_{FE} is 40.

The important specifications for the output devices are:

BV_{CEO}	Minimum 15V
H_{FE}	Minimum 40 at 1 Amp
f_t	40 MHz or more
$V_{CE}(SAT)$	As low as possible

The MJE200 and MJE210 series are excellent with minimum H_{FE} of 45 and saturation voltages of only 300 mV at 1 Amp. The D44H11 and D45H11 series have even lower saturation voltages and a higher H_{FE} of 60. Both types are available in surface mount from Motorola, SGS and others.

Motor Characterization

The formulas for the compensation of the EL2037AC are based on the electrical characteristics of the motor. For most high-performance voice coil motors, the effective impedance is a function of frequency that can not be modeled over a large frequency range with a simple resistor and inductor. Fortunately, for the compensation equations to work, it is only necessary to model the motor at the bandwidth frequency.

The easiest way to determine the resistance and inductance of a motor is to use an RLC meter that reads the inductance and resistance at the bandwidth frequency. If such a meter is not available, a network analyzer and a current probe will give the impedance versus frequency. From the magnitude and phase at the bandwidth frequency, the real and imaginary impedance can be calculated (and the imaginary part converted to inductance). Some network analyzers will even give the real and imaginary impedances directly.

The setup below was used to generate the following curve of impedance versus frequency on a real motor. At 10 kHz the impedance is 13Ω at 52°. This is 8Ω real and 10.25Ω reactive. Notice that the DC resistance is much less than the impedance at 10 kHz. The equivalent inductance is 163 μH.

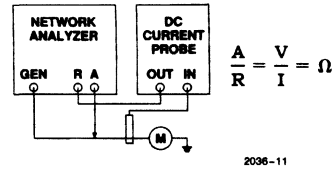


Figure 3. Motor Characterization Setup

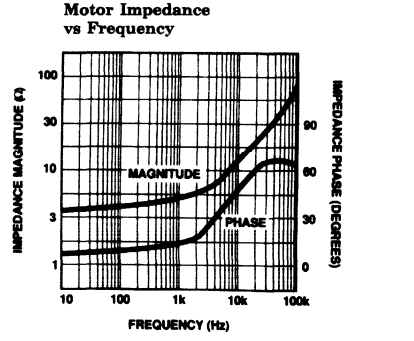


Figure 4

Compensation

The compensation components, C_c and R_c, are calculated to give the desired transconductance bandwidth. The equivalent motor resistance and inductance, R_m and L_m, the value of the sense resistor, R_s, and the bandwidth, BW, are used to compute C_c and R_c. The EL2037AC requires two identical networks for compensation. Each network is a series connection of a resistor, R_c, and a capacitor, C_c. The matching of the components is not critical, standard five percent tolerance is suf-

EL2037AC
Servo Motor Driver

Applications Information — Contd.

ficient. The derivation of the following equations is in the AC Response Section.

$$C_c = \frac{4\,R_s}{800\,(R_m + R_s)\,2\pi\,BW}$$

$$R_c = \frac{L_m}{(R_m + R_s)\,C_c}$$

To compensate the motor described in the previous section for a 10 kHz bandwidth and a transconductance of 1 Amp per volt we substitute

$R_s = 0.25$ $\quad L_m = 160\ \mu H$
$R_m = 8\Omega$ $\quad BW = 10$ kHz

into the above equations.

$$C_c = \frac{4\,(0.25)}{800(8+0.25)(2)(3.14)(10\text{ kHz})} = 2400\text{ pF}$$

use 2200 pF

$$R_c = \frac{160\text{ mH}}{(8+0.25)(2200\text{ pF})} = 8800$$

use 10k.

Two 220 pF capacitors between pin 4 and pin 7, and between pin 6 and Ground (as shown in the Typical Application drawing on page 6) smooth fast rising input signals to ensure that the operational amplifier will not slew rate limit. Both capacitors can be eliminated if the slew rate of the input signal does not exceed 0.5 V/μs.

Park Function

The EL2037AC will force a constant voltage across the motor when pin 3, park-bar, is open or low. The output voltage is negative; pin 14 if forced to about zero volts and pin 17 to the constant voltage determined by the resistor R_P from pin 2 to ground. This voltage drive produces a constant velocity that is used to park the heads. The power to drive the motor is supplied from an auxiliary supply (Aux Sup) on pin 20. Usually this auxiliary supply is the normal supply reduced by a diode drop. The spindle motor also is tied to the auxiliary supply. Once the normal supply drops, the spindle motor back EMF acts as a generator and holds the voltage up long enough for the drive to park the heads. An external bypass capacitor is needed on pin 20 to filter the ripple. To determine the value of the resistor required from pin 2 to ground use the curve of Output Park Voltage versus Park Resistor (page 5).

AC Response

The AC response of the EL2037AC is set by the motor electrical time constant and the compensation impedance Z(s). The actual circuit is quite difficult to analyze due to the differential techniques used to improve accuracy. To simplify the analysis, a single-ended system can be modeled with a summer, a forward path, the motor electrical elements and a feedback path. The forward path has a gain that includes the compensation components, and the feedback includes the current sense resistor, R_S. In this way we can solve for the response in terms of the actual EL2037AC external component values.

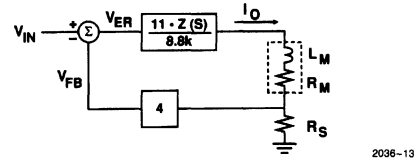


Figure 5. The Servo Motor Loop Equivalent Circuit

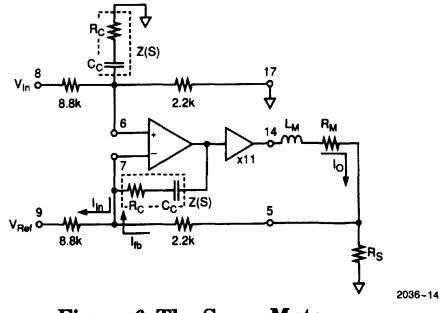


Figure 6. The Servo Motor Control Equivalent Circuit

AC Response — Contd.

The forward path gain of this circuit is the output current divided by the input voltage without any feedback.

$$A = \frac{I_o}{V_{IN}} = \frac{11Z(s)}{8.8K\,(sL_m + R_m + R_s)}$$

The feedback path is the feedback voltage divided by the output current.

$$b = \frac{V_{FB}}{I_O} = 4\,R_s$$

The closed loop response is therefore:

$$A_{CL} = \frac{A}{1 + A\beta} = \frac{\frac{1}{\beta}}{1 + \frac{1}{A\beta}}$$

$$= \frac{\frac{1}{4\,R_s}}{1 + \frac{800}{4\,R_s}\left(\frac{s\,L_m}{R_m + R_s} + 1\right)\left(\frac{R_m + R_s}{Z(s)}\right)}$$

The compensation network $Z(s)$ is usually a series resistor and capacitor, R_c and C_c. That is to say

$$Z(s) = R_c + \frac{1}{s\,C_c} = \frac{s\,R_c\,C_c + 1}{s\,C_c}$$

Substituting this into the closed loop equation gives

$$A_{CL} = \frac{\frac{1}{4\,R_s}}{1 + \frac{800}{4\,R_s}\left(\frac{s\,L_m}{R_m + R_s} + 1\right)\frac{(R_m + R_s)\,s\,C_c}{(s\,R_c\,C_c + 1)}}$$

There are many ways to analyze this for the desired response. Bode plots, Nyquist plots and root locus techniques can all be used to determine the values of R_c and C_c for a particular motor. The simplest way to obtain the values of R_c and C_c is to make the zero due to them equal to the motor pole.

$$R_c\,C_c = \frac{L_m}{R_m + R_s}$$

Substituting this constraint into the closed loop equation results in a single pole system. The equation is:

$$A_{CL} = \frac{\frac{1}{4\,R_s}}{\frac{800}{4\,R_s}(R_m + R_s)\,s\,C_c + 1}$$

The closed loop −3 dB bandwidth (BW) is where the magnitude of the real and imaginary parts of the denominator are equal. We therefore can say, in terms of bandwidth in Hertz, that

$$\frac{800}{4\,R_s}(R_m + R_s)\,2\pi \bullet BW \bullet C_c = 1$$

Solving these for C_c and R_c gives:

$$C_c = \frac{4\,R_s}{800\,(R_m + R_s)\,2\pi\,BW}$$

$$R_c = \frac{L_m}{(R_m + R_s)\,C_c}$$

Simplified Schematic

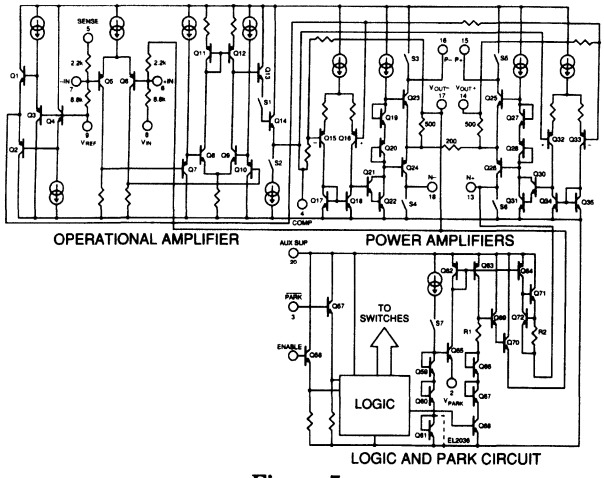


Figure 7

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL3038C
2 Amp Precision Servo Motor Drivers

Features

- No crossover distortion
- Low output offset current
- Maximum output swing
- Programmable park voltage
- Programmable transconductance
- Programmable bandwidth
- Chip enable function
- Drive low cost bipolar transistors
- Single sense resistor
- Minimum external components
- Current sensing amplifier

Applications

- Voice coil motor servo systems
- Winchester disk drives
- Optical disk drives
- Super floppy drives
- DC motor control

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL3038CM	0°C to +75°C	SOL-20	MDP0027

General Description

This IC is a servo motor driver circuit designed to drive voice coil motors in disk drive application. It is designed to drive an H bridge consisting of four low-cost external bipolar transistors for maximum output swing. The EL3038C achieves a new level drive capability. With typical output current drive of 45 mA they are suitable for very low resistance voice coils. Crossover distortion is eliminated by Class AB biasing of the output devices with a unique temperature stable circuit which never needs adjustment.

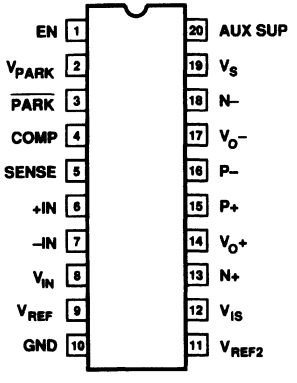
System accuracy is maximized by using only 1 external sense resistor in series with the motor. Compared to conventional grounded resistor circuits they have inherent positive to negative gain matching and no gain error due to transistor alpha. All three critical bias voltages in the main loop use the same V_{REF} voltage. This reduces the output offset current to less than 5 mA.

The EL3038C has an internal low power supply voltage detection which automatically initiates parking of the heads when V_{AUX} falls below about 7.5V. The power for this function comes from a separate supply generated by the back EMF of the spindle motor used as a generator. The EL3038C requires only 2.5V back EMF. Parking can also be commanded by a logic low on the PARK-BAR pin.

The EL3038C has a low power consumption disabled state controlled by the logic input pin ENABLE.

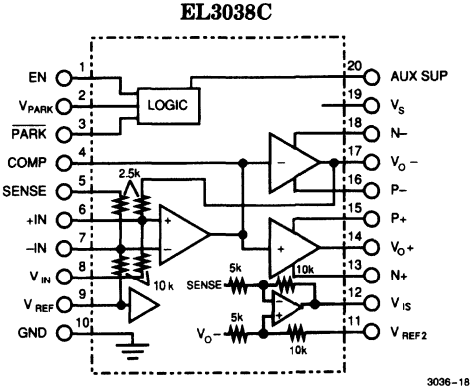
The EL3038C has a motor current sensing amplifier for use in the system level servo loop. The amplifier multiplies the voltage across the sense resistor by 2 and references it to a reference voltage independent of the main loop reference voltage.

Connection Diagram



3036-3

Block Diagram



3036-18

Manufactured under U.S. Patent Nos. 4,910,477, 4,878,034, 4,935,704 and 4,963,802.

Absolute Maximum Ratings

V_S	Supply Voltage, Pin 19	−0.3V to +15V	T_A	Operating Temperature Range	−25°C to +85°C
V_{AUX}	Auxiliary Supply Voltage, Pin 20	V_S −1V to +15V		Lead Temperature	
V_{LIM}	Short Circuit Limit Sense Voltage	V_S −0.3V to +15V		SOL Package	300°
V_{IN}	Logic Inputs, Pins 1 and 3	−0.3V to +15V		Vapor Phase (60 seconds)	215°C
	Signal Inputs, Pins 8 and 9	−0.3V to +15V		Infrared (15 seconds)	220°C
I_{IN}	Input Current, Pins 1, 3, 8, and 9	10 mA	T_{ST}	Storage Temperature	−65°C to +150°C
T_J	Junction Temperature	150°C	P_D	Power Dissipation, T_A = 25°C	
				DIP Package	1.80W
				SOL Package	1.50W

Important Note

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level **Test Procedure**

I 100% production tested and QA sample tested per QA test plan QCX0002.

II 100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.

III QA sample tested per QA test plan QCX0002.

IV Parameter is guaranteed (but not tested) by Design and Characterization Data.

V Parameter is typical value at T_A = 25°C for information purpose only.

Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = 12V$, $V_{REF} = 5V$, $R_s = 0.25\Omega$, Load = 10Ω. See test circuits

Parameter	Description	Min	Typ	Max	Test Level	Units
Enabled Mode, Pin 1 = H. Pin 3 = H. (Note 1)						
I_{OS}	Output Offset Current	−5	0.6	5	I	mA
G_{M1}	Transconductance, I_{OUT} = ±100 mA	0.95	1	1.05	I	A/V
G_{M2}	Transconductance, I_{OUT} = ±1A	0.93	1	1.07	I	A/V
I_{ST}	Quiescient Supply Current, Total		20		V	mA
I_{Q1}	Quiescient Supply Current, Pin 12 + 19		9	12	I	mA
I_{Q2}	Auxiliary Supply Quiescient Current, Pin 20	4	5	7	I	mA
I_{QE}	External Transistor Quiescient Current	1	8	12	I	mA
I_{DN}	NPN Drive Current, Pin 13 or 18	35	45		I	mA
I_{DP}	PNP Drive Current, Pin 15 or 16	40	55		I	mA
I_{IB}	Input Bias Current. $V_{IN} = V_{REF}$ = 2.5V, 6.5V	−250	50	250	I	µA
I_{IA}	Active Input Current. V_{IN} = 0.5V, V_{REF} = 2.5V	−1.5			I	mA
I_{IA}	Active Input Current. V_{IN} = 4.5V, V_{REF} = 2.5V		0.4	0.7	I	mA
I_{RB}	Reference Bias Current. $V_{IN} = V_{REF}$ = 2.5V, 6.5V	−250	100	250	I	µA
I_{RA}	Active Reference Current. V_{IN} = 0.5V, V_{REF} = 2.5V	−1.0	−0.5		I	mA
I_{RA}	Active Reference Current. V_{IN} = 4.5V, V_{REF} = 2.5V	−1.5	−0.9	0.5	I	mA
V_S	Supply Voltage Range, Pin 19	11	12	13	IV	V
VRR	Reference Voltage Range, Pin 9	2.5		6.5	I	V
RRR	Reference Voltage Rejection, 2.5V to 6.5V	−1	−0.3	1	I	mA/V
PSR	Power Supply Rejection, 11V to 13V	−1	0.3	1	I	mA/V
THD	Total Harmonic Distortion, V_{IN} = 20 mV_{PP}, 1 kHz		0.5	1	I	%

EL3038C
2 Amp Precision Servo Motor Drivers

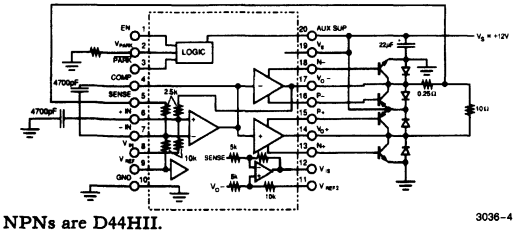
Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = 12V$, $V_{REF} = 5V$, $R_s = 0.25\Omega$, Load = 10Ω. See test circuits — Contd.

Parameter	Description	Min	Typ	Max	Test Level	Units
Park Mode. Pin 1 = H. Pin 3 = L. Aux Supply (Pin 20) = 6V (Note 1) R_{PARK} = 1.5k						
V_{P1}	V_{OUT} ($V_O^+ - V_O^-$) R_{PARK} = 1.5k	−0.30	−0.45	−0.55	I	V
V_{P1}	V_{OUT} ($V_O^+ - V_O^-$) R_{PARK} = 3k	−0.40	−0.50	−0.60	I	V
V_{AR}	Aux Supply Range (−0.25V ≤ V_{OUT} ≤ −0.75V)	2.5	6	12	I	V
I_{PD}	NPN Drive. Pin 13	2	3		I	mA
I_{AUX}	Short Circuit Maximum Current (Pin 17 = 0V)		250		V	mA
Disabled Mode. Pin 1 = L. Pin 3 = H. (Note 1)						
I_{OD}	Output Current	−100	10	+100	I	µA
R_{OD}	Output Resistance. I_{OUT} ±1 mA	2	4		I	kΩ
I_{SD}	Total Supply Current, Pin 12, 19, and 20 + Transistors		6	10	I	mA
Motor Current Sense Amplifier						
A_{VIS}	Voltage Gain	1.85		2.15	I	V/V
V_{VIS}	Output Voltage Range	1		9	I	V
V_{OS}	Output Offset Voltage, V_O- = Sense = V_{REF}	−10		+10	I	mV
Logic Inputs						
V_{IL}	Low Level Input Voltage for a Valid Low			0.8	I	V
I_{IL}	Low Level Input Current, Logic = 0V	−30	−10	0	I	µA
V_{IH}	High Level Input Voltage for a Valid High	2			I	V
I_{IH}	High Level Input Current, Logic = 5V	0	10	150	I	µA
Individual Amplifiers						
A_V	Power Amplifier Voltage Gain	10.5	11.5	12.5	I	V/V

Note 1: Logic Level L = 0.8V, Logic Level H = 2.0V

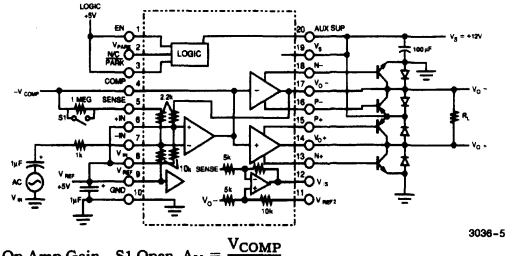
DC and Closed Loop AC Test Circuit



3036-4

NPNs are D44HII.
PNPs are D45HII.
Diodes are 1 Amp IN4000.

Open Loop AC Test Circuit



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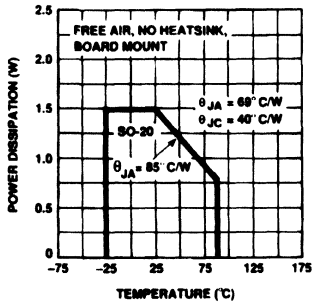
Op Amp Gain—S1 Open, $A_V = \frac{V_{COMP}}{V_{IN}}$

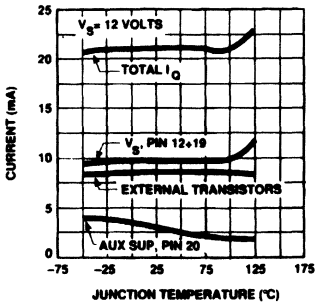
Power Amp Gain—S1 Closed, $A_V = \frac{(V_{O+})-(V_{O-})}{V_{COMP}}$

Typical Performance Curves

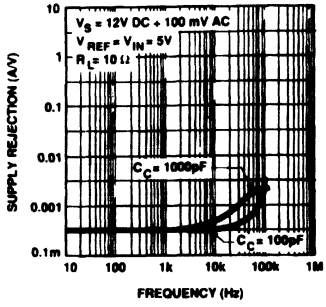
Maximum Power Dissipation vs Ambient Temperature



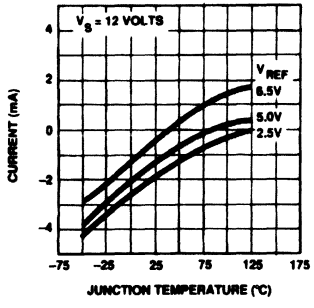
Quiescent Current vs Temperature



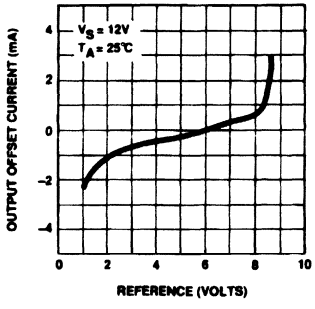
Supply Rejection vs Frequency



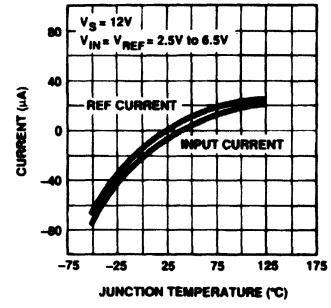
Output Offset Current vs Temperature



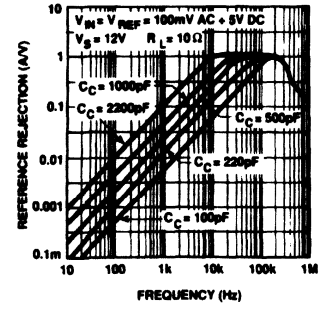
Output Offset Current vs Reference Voltage— Typical Unit



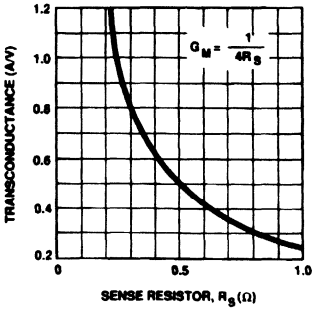
Reference and Input Bias Current vs Temperature



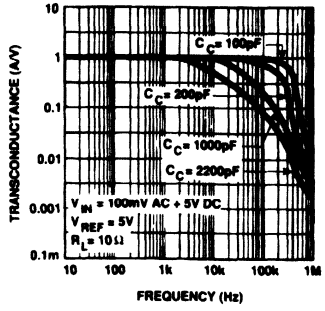
Reference Voltage Rejection vs Frequency



Transconductance vs Sense Resistor



Transconductance vs Frequency



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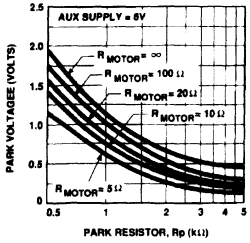
7

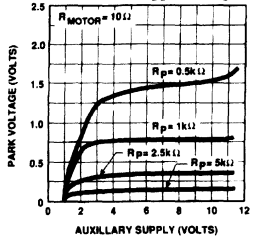
EL3038C
2 Amp Precision Servo Motor Drivers

Typical Performance Curves — Contd.

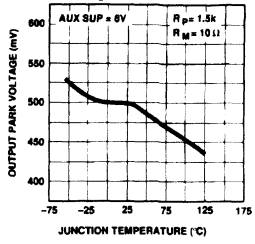
Output Park Voltage vs Park Resistor



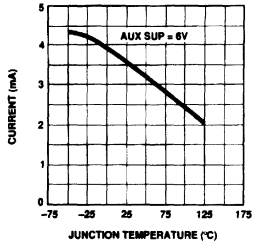
Output Park Voltage vs Auxiliary Supply Voltage



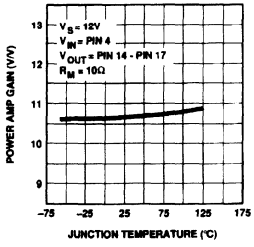
Output Park Voltage vs Temperature



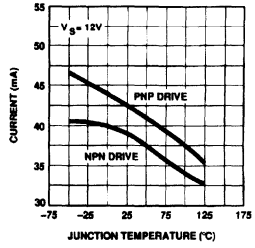
NPN Base Drive During Park vs Temperature



Power Amplifier Gain vs Temperature

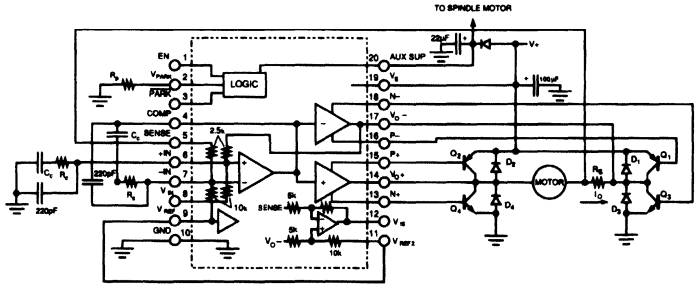


Power Amplifier Drive Current vs Temperature



3036-7

Typical Application



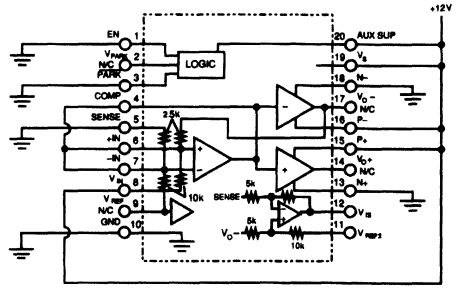
External Components

Parameter	Description	Min	Typ	Max	Units	Typical ± % Tolerance
R_P	Sets the Motor Voltage During PARK Mode	0.5k	1.5k	Open	Ω	5
R_s	Current Sense Resistor	0.1	0.25	1	Ω	2
C_C	Loop Compensation. Sets dominant pole	100	2000	0.1 μF	pF	5
R_C	Loop Compensation. Makes a Zero, Equal to Motor Pole	0	10	200	kΩ	5
D1–4	Catch diodes, 1 amp	1N4000				
Q1, 2	PNP Power Transistors. Min H_{FE} = 60	MJE210 or D45H11				
Q3, 4	NPN Power Transistors. Min H_{FE} = 60	MJE200 or D44H11				
	R_1 = 0.425/Trip current					
	C_d = Delay/250k					
	R_s = 1/(4*DC transimpedance)					

Truth Table

Enable (Pin 1)	Park (Pin 3)	Output
>2.0V	>2.0V	Normal Operation
<0.8V	>2.0V	Disabled
X	<0.8V	Parking Mode
X	X	Disabled for Delay

Burn-In Circuit



EL3038C
2 Amp Precision Servo Motor Drivers

Circuit Description

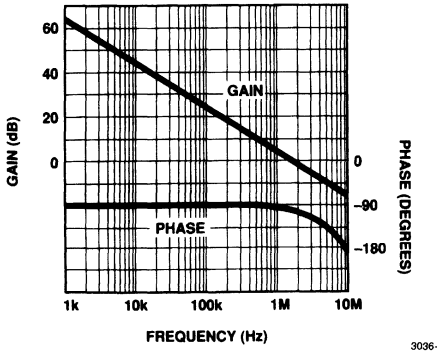
Common Functions

There are 4 circuit blocks common to the EL3038. They are a low offset voltage operational amplifier, a single-ended input to differential output power amplifier, a logic circuit, and a parking circuit. The operational amplifier and power amplifier together with four well-matched internal resistors make the basic transconductance amplifier. The logic circuit enables or disables the amplifiers or the park circuit. The park circuit provides a constant voltage across the motor.

The Operational Amplifier

The operational amplifier is a low offset design with modest gain and excellent common mode rejection over a wide range that includes ground. This ensures proper operation when the motor voltage exceeds the supply or ground and is clamped by the catch diodes. The operational amplifier is internally compensated for stable operation at all times. The gain bandwidth product is 2 MHz and the phase margin is 60° at unity gain. The operational amplifier has internal clamps to limit its output swing to about ±2V of the reference voltage. The clamps are not shown in the simplified schematic and their only function is to prevent overcharging of the compensation capacitor during transients. The operational amplifier output is disabled by the logic circuit when either pin 1 or pin 3 is low.

Op Amp Open Loop
Gain and Phase vs Frequency



3036-10

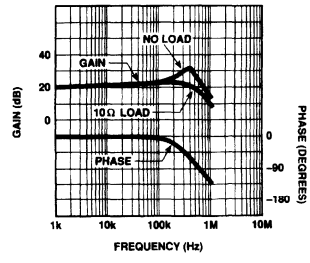
Figure 1

The Power Amplifier

The power amplifiers of the EL3038C are made of two identical stages that take a single-ended input and drive the motor differentially. The outputs of both stages are biased from the buffered reference voltage to reduce output offset current. Each stage has feedback for linearity and gain accuracy. One stage operates noninverting and the other inverting, resulting in a total gain of 11. The feedback is more complicated than shown in the simplified schematic, to ensure accurate gain even when one amplifier saturates before the other. The bandwidth of the power amplifier is about 500 kHz as shown below.

External power transistors deliver the power to the motor to optimize the output swing capability and eliminate power dissipation concerns. A unique biasing circuit eliminates low-level crossover distortion by biasing the transistors on at a few mA. The amplifier outputs are disabled when either pin 1 or pin 3 is low.

Power Amplifier Gain and
Phase vs Frequency



3036-11

Figure 2

The Logic Circuit

The logic circuit operates from a separate supply called the auxiliary supply. In a typical disk drive application, the auxiliary supply is usually within a diode drop of the normal supply, except when the normal supply is interrupted. Then the auxiliary supply is generated from the back EMF of the spindle motor. By having two supplies, the logic circuit can operate for a while after the main power has been removed.

Circuit Description — Contd.

The EL3038C has two external inputs and one common internal input to the logic circuit. The external inputs are Park-Bar and Enable. The common internal input is from the low supply voltage sensor. The external inputs are TTL compatible and can be driven from CMOS sources. The park-bar input and the low supply sensor input override the Enable input. When Park-Bar is high and the supply voltage is above approximately 8V the Enable input turns the main amplifiers on or off.

Park Circuit

When the Park-Bar logic input is high and the voltage on V_S is above about 8V the park circuit is disabled and has no effect on the motor. If either condition is reversed, the main amplifiers are disabled and the park circuit is activated. Like the logic circuit, the park circuit uses the auxillary supply, not the main supply. The park circuit sets the voltage at ParkR (Pin 2) to about 0.75V. The value of the external resistor from ParkR to GND sets the voltage at V_O- (pin 17) according to the graph in the Typical Performance section. At the same time current is provided at N+ (pin 13) to saturate the external NPN transistor on the opposite side of the motor.

Current Sense Circuit

The EL3038C has a copy of the main low offset voltage operational amplifier wired with 4 well-matched resistors to amplify the voltage across the motor current sense resistor by 2. Its output appears at the pin V_{IS}. The resistors are wired to center the amplified voltage around the user supplied voltage at pin V_{REF2}. This amplifier is active whenever the main transconductance amplifiers are active.

Applications Information

Transconductance

The DC transconductance is set by one resistor, R_s, that senses the motor current. The input voltage is the difference between the voltage on pin 8 and 9. When pin 8 is more positive than pin 9, the input is said to be positive. When the input is positive, the voltage on pin 14 is more positive than pin 17 and the motor current is said to be positive. The DC transconductance is given by the simple equation:

$$G_{MO} = \frac{1}{4R_s} = \frac{I_O}{V_{IN}-V_{REF}}$$

For a transconductance of 1 Amp per volt, the sense resistor, R_s, should equal 0.25Ω. Because the sense resistor is very small, care should be taken to insure that the PC board trace resistance does not increase its value. The connections from pin 5 and 17 are the "sense" connections while

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EL3038C
2 Amp Precision Servo Motor Drivers

Applications Information — Contd.

the motor and transistor collectors are the "force" connections. Therefore, the connections from pin 5 and pin 17 should go directly to the sense resistor.

Source Impedance

The input and reference source impedances should be low to prevent gain and offset errors. The input current is determined by the internal feedback resistors and the input and output voltages. The worst case current flows when the reference is low and the input is lower and therefore the V_O- output is high. This condition is tested and the input and reference currents are guaranteed to be less than 1.5 mA. Therefore, the input and reference should be able to sink and source 1.5 mA. For the typical case where the transconductance is 1 Amp per volt, a source impedance of less than 10Ω will generate less than 2.5 mA of additional output offset current and less than 1.5% gain error. Obviously, if the output of an operational amplifier drives the IC, there will be no errors due to source impedance. Be careful with some single supply operational amplifiers (324 and 358 types). They require output loading to ground to eliminate their high output impedance and crossover distortion.

Transistors

The IC will drive almost any pair of complementary transistors. The output transistor drive is guaranteed to be more than 40 mA for the PNPs and 35 mA for the NPNs. The required maximum output current divided by the available base drive gives the minimum H_{FE} required. For 2 Amp output current, the minimum H_{FE} is 60.

The important specifications for the output devices are:

BV_{CEO}	Minimum 15V
H_{FE}	Minimum 60 at 2 Amp
f_t	40 MHz or more
$V_{CE}(SAT)$	As low as possible

The MJE200 and MJE210 series are excellent with minimum H_{FE} of 45 and saturation voltages of only 300 mV at 1 Amp. The D44H11 and D45H11 series have even lower saturation voltages and a higher H_{FE} of 60. Both types are available in surface mount from Motorola, SGS and others.

Motor Characterization

The formulas for motor compensation are based on the electrical characteristics of the motor. For most high-performance voice coil motors, the effective impedance is a function of frequency that can not be modeled over a large frequency range with a simple resistor and inductor. Fortunately, for the compensation equations to work, it is only necessary to model the motor at the bandwidth frequency.

The easiest way to determine the resistance and inductance of a motor is to use an RLC meter that reads the inductance and resistance at the bandwidth frequency. If such a meter is not available, a network analyzer and a current probe will give the impedance versus frequency. From the magnitude and phase at the bandwidth frequency, the real and imaginary impedance can be calculated (and the imaginary part converted to inductance). Some network analyzers will even give the real and imaginary impedances directly.

The setup below was used to generate the following curve of impedance versus frequency on a real motor. At 10 kHz the impedance is 13Ω at 52°. This is 8Ω real and 10.25Ω reactive. Notice that the DC resistance is much less than the impedance at 10 kHz. The equivalent inductance is 163 μH.

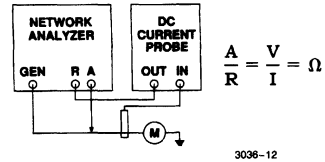

Figure 3. Motor Characterization Setup

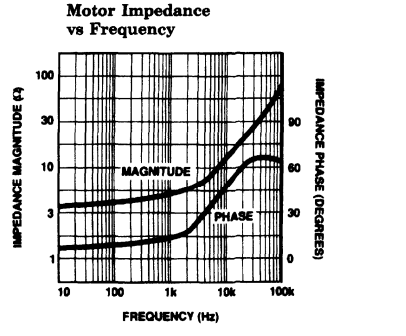

Figure 4

Applications Information — Contd.

Compensation

The compensation components, C_c and R_c, are calculated to give the desired transconductance bandwidth. The equivalent motor resistance and inductance, R_m and L_m, the value of the sense resistor, R_s, and the bandwidth, BW, are used to compute C_c and R_c. Two identical networks are required for compensation. Each network is a series connection of a resistor, R_c, and a capacitor, C_c. The matching of the components is not critical, standard five percent tolerance is sufficient. The derivation of the following equations is in the AC Response Section.

$$C_c = \frac{4\,R_s}{870\,(R_m + R_s)\,2\pi\,BW}$$

$$R_c = \frac{L_m}{(R_m + R_s)\,C_c}$$

To compensate the motor described in the previous section for a 10 kHz bandwidth and a transconductance of 1 Amp per volt we substitute

$R_s = 0.25 \quad L_m = 160\ \mu H$
$R_m = 8\Omega \quad BW = 10\ kHz$

into the above equations.

$$C_c = \frac{4\,(0.25)}{870(8+0.25)(2)(3.14)(10\ kHz)} = 2200\ pF$$

$$R_c = \frac{160\ \mu H}{(8+0.25)(2200\ pF)} = 8800$$

use 10k.

Two 220 pF capacitors between pin 4 and pin 7, and between pin 6 and Ground (as shown in the Typical Application drawing on page 6) smooth fast rising input signals to ensure that the operational amplifier will not slew rate limit. Both capacitors can be eliminated if the slew rate of the input signal does not exceed 0.5 V/μs.

Park Function

The EL3038C will force a constant voltage across the motor when pin 3, park-bar, is open or low. The output voltage is negative; pin 14 if forced to about zero volts and pin 17 to the constant voltage determined by the resistor R_P from pin 2 to ground. This voltage drive produces a constant velocity that is used to park the heads. The power to drive the motor is supplied from an auxiliary supply (Aux Sup) on pin 20. Usually this auxiliary supply is the normal supply reduced by a diode drop. The spindle motor also is tied to the auxiliary supply. Once the normal supply drops, the spindle motor back EMF acts as a generator and holds the voltage up long enough for the drive to park the heads. An external bypass capacitor is needed on pin 20 to filter the ripple. To determine the value of the resistor required from pin 2 to ground use the curve of Output Park Voltage versus Park Resistor (page 5).

Motor Current Sensing

Many servo systems require a voltage representing the actual motor current. The V_{IS} signal (Pin 12) provides this. Internally there is an OpAmp configured to amplify the voltage across the motor current sense resistor by 2 and reference it to reference voltage V_{REF2} at pin 11. For example if the motor current were -1A, the sense resistor 0.25Ω and the V_{REF2} 2.5V the voltage at V_{IS} will be 2.5V + ($-1 \times 0.25 \times 2$) or 2.0V. The internal OpAmp is a copy of the OpAmp used in the main motor current amplifier and has the same characteristics of low offset and good gain. But its output swing is limited to +1V to +8V (V_S = 12V). Consequently with some combinations of reference voltage and motor current sense resistor the signal at V_{IS} will be clipped. The OpAmp and gain setting resistors are guaranteed to have a offset voltage less than 10 mV. So in a typical application the ultimate accuracy of the V_{IS} signal is $\pm$10 mA.

AC Response

The AC response is set by the motor electrical time constant and the compensation impedance Z(s). The actual circuit is quite difficult to analyze due to the differential techniques used to improve accuracy. To simplify the analysis, a single-ended system can be modeled with a summer, a forward path, the motor electrical elements and a feedback path. The forward path has a gain that includes the compensation components, and the feedback includes the current sense resistor, R_S. In this way we can solve for the response in terms of the actual external component values.

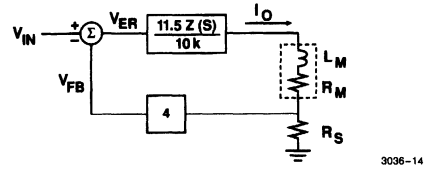

Figure 5. The Servo Motor Loop Equivalent Circuit

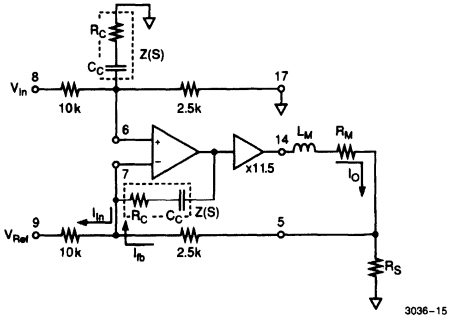

Figure 6. The Servo Motor Control Equivalent Circuit

The forward path gain of this circuit is the output current divided by the input voltage without any feedback.

$$A = \frac{I_o}{V_{IN}} = \frac{11.5Z(s)}{10K\,(sL_m + R_m + R_s)}$$

The feedback path is the feedback voltage divided by the output current.

$$b = \frac{V_{FB}}{I_O} = 4\,R_s$$

The closed loop response is therefore:

$$A_{CL} = \frac{A}{1 + A\beta} = \frac{\frac{1}{\beta}}{1 + \frac{1}{A\beta}}$$

$$= \frac{\frac{1}{4\,R_s}}{1 + \frac{870}{4\,R_s}\left(\frac{s\,L_m}{R_m + R_s} + 1\right)\left(\frac{R_m + R_s}{Z(s)}\right)}$$

The compensation network Z(s) is usually a series resistor and capacitor, R_c and C_c. That is to say

$$Z(s) = R_c + \frac{1}{s\,C_c} = \frac{s\,R_c\,C_c + 1}{s\,C_c}$$

Substituting this into the closed loop equation gives

$$A_{CL} = \frac{\frac{1}{4\,R_s}}{1 + \frac{870}{4\,R_s}\left(\frac{s\,L_m}{R_m + R_s} + 1\right)\frac{(R_m + R_s)\,s\,C_c}{(s\,R_c\,C_c + 1)}}$$

There are many ways to analyze this for the desired response. Bode plots, Nyquist plots and root locus techniques can all be used to determine the values of R_c and C_c for a particular motor. The simplest way to obtain the values of R_c and C_c is to make the zero due to them equal to the motor pole.

$$R_c\,C_c = \frac{L_m}{R_m + R_s}$$

Substituting this constraint into the closed loop equation results in a single pole system. The equation is:

$$A_{CL} = \frac{\frac{1}{4\,R_s}}{\frac{870}{4\,R_s}(R_m + R_s)\,s\,C_c + 1}$$

The closed loop −3 dB bandwidth (BW) is where the magnitude of the real and imaginary parts of the denominator are equal. We therefore can say, in terms of bandwidth in Hertz, that

$$\frac{870}{4\,R_s}(R_m + R_s)\,2\pi \bullet BW \bullet C_c = 1$$

Solving these for C_c and R_c gives:

$$C_c = \frac{4\,R_s}{870\,(R_m + R_s)\,2\pi\,BW}$$

$$R_c = \frac{L_m}{(R_m + R_s)\,C_c}$$

Arrays

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Elantec Transistor Arrays

ELANTEC Part Number	Description	Test Temp	V_{be} Match		H_{fe} Match		Min H_{fe}		BV_{ceo} BV_{cbo} Over Temp (Min)	Packages
			25°	Over Temp	25°C	Over Temp	25°C	Over Temp		
EP2015C	Monolithic, D.I. Matched Quad PNP Transistor Array	−25°C to +85°C	5 mV	N/A	10%	N/A	75	N/A	40V	14-Pin Plastic DIP 14-Pin CerDIP
EP2015AC	Monolithic, D.I. Precision Matched Quad PNP Transistor Array	0°C to +75°C	1 mV	2 mV	10%	20%	150	60	40V	14-Pin Plastic DIP
EN2016C	Monolithic, D.I. Matched Quad NPN Transistor Array	−25°C to +85°C	5 mV	N/A	10%	N/A	75	N/A	40V	14-Pin Plastic DIP

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EP2015C/EP2015AC
Fast Quad PNP Array

Features

- Four independent fast PNP's
- 350 MHz f_t
- Tight V_{BE} matching—1 mV
- Tight H_{fe} matching—5%
- One chip construction with dielectric isolation
- Excellent thermal tracking
- High H_{fe}—150 minimum
- 40V minimum BV_{ceo}
- Each transistor similar to 2N3906
- Pin compatible with TPQ3906 and MPQ3906

Applications

- Current sources
- Current mirrors
- Log amplifiers
- Multipliers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EP2015CN	0°C to +75°C	P-DIP	MDP0031
EP2015ACN	0°C to +75°C	P-DIP	MDP0031
EP2015CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EP2015 family are quad monolithic vertical PNP transistor arrays which offer excellent parametric matching and high speed performance. The 350 MHz f_t provides A.C. performance similar to 2N3906 class devices. Manufactured on Elantec's Complementary Bipolar process, these transistors are electrically isolated from each other by a layer of oxide. The resulting low collector to substrate capacitance allows very high speed performance with minimal crosstalk. In addition, complete D.C. isolation is achieved. Substrate biasing is not required for normal operation, however for optimum high speed performance the substrate should be grounded. One-chip construction insures excellent parameter matching and tracking over temperature.

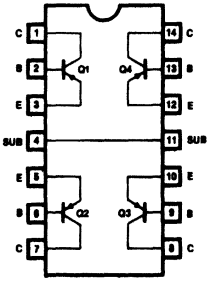
The low cost EP2015C is specified at 25°C. The EP2015AC is more tightly specified and guaranteed over the commercial temperature range of 0°C to +75°C. The EP2015C and EP2015AC are available in 14-pin plastic dual-in-line packages.

For information on a complementary NPN transistor array, see Elantec's EN2016 family data sheet.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, request our brochure, QRA1: *Elantec's Processing—Monolithic Products.*

Connection Diagrams

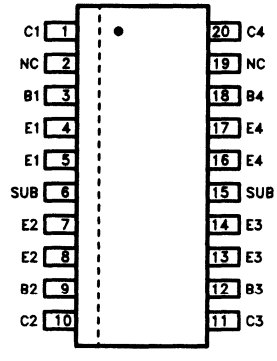
DIP Package



2016-1

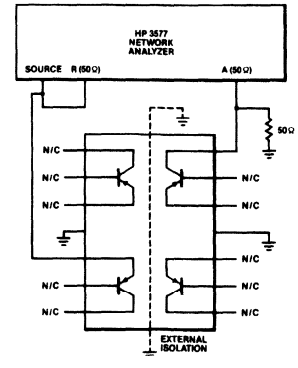
Top View

20-Lead SOL



2015-13

Isolation Characteristics Test Circuit



2015-2

EP2015C/EP2015AC
Fast Quad PNP Array

Absolute Maximum Ratings

P_D	Power Dissipation	
	Each Transistor	500 mW (T_A = 25°C)
	Total Package	1.25W (T_A = 25°C)
T_A	Operating Temperature Range	−0°C to +75°C
T_J	Maximum Junction Temperature	150°C
T_{ST}	Storage Temperature	−65°C to +150°C
	Lead Temperature	
	SOL Package	
	Vapor Phase (60 seconds)	215°C
	Infrared (15 seconds)	220°C
	(Soldering, <10 seconds)	300°C
V_{CB}	Max	40V
V_{EB}	Max	5V
V_{CE}	Max	40V
I_C	Max	50 mA
I_B	Max	10 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

Parameter	Description	Test Conditions	EP2015C				Units
			Min	Typ	Max	Test Level	
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA, T_A = 25°C			5	I	mV
		$T_{MIN} < T_A < T_{MAX}$					mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA, T_A = 25°C			10	I	%
		$T_{MIN} < T_A < T_{MAX}$					%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1 mA, T_A = 25°C			10	I	%
		$T_{MIN} < T_A < T_{MAX}$					%
ΔH_{fe3}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA, T_A = 25°C			10	I	%
		$T_{MIN} < T_A < T_{MAX}$					%
H_{fe1}	(Note 3)	V_{CE} = 1V, I_C = 0.1 mA, T_A = 25°C	75			I	
		$T_{MIN} < T_A < T_{MAX}$					
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA, T_A = 25°C	75			I	
		$T_{MIN} < T_A < T_{MAX}$					

Electrical Characteristics — Contd.

Parameter	Description	Test Conditions	EP2015				Units
			Min	Typ	Max	Test Level	
H_{fe3}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	75			I	
		$T_{MIN} < T_A < T_{MAX}$					
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$					V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{ceo}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_C = 0 mA T_A = 25°C	5			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$					nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$					nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA, < I_C < 2 mA T_A = 25°C		1		V	Ω

Parameter	Description	Test Conditions	EP2015AC				Units
			Min	Typ	Max	Test Level	
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA T_A = 25°C			1	I	mV
		$T_{MIN} < T_A < T_{MAX}$			2	III	mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 0.1 mA T_A = 25°C			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	III	%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1 mA T_A = 25°C			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	III	%
ΔH_{fe3}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C			5	I	%
		$T_{MIN} < T_A < T_{MAX}$			10	III	%

EP2015C/EP2015AC
Fast Quad PNP Array

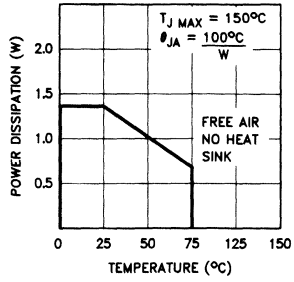
Electrical Characteristics — Contd.

Parameter	Description	Test Conditions	EP2015A				Units
			Min	Typ	Max	Test Level	
H_{fe1}	(Note 3)	V_{CE} = 1V, I_C = 0.1 mA T_A = 25°C	150			I	
		$T_{MIN} < T_A < T_{MAX}$	60			III	
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA T_A = 25°C	150			I	
		$T_{MIN} < T_A < T_{MAX}$	60			III	
H_{fe3}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	100			I	
		$T_{MIN} < T_A < T_{MAX}$	40			III	
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$			1.10	III	V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$			0.30	III	V
BV_{ceo}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			I	V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$	40			III	V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_C = 0 mA T_A = 25°C	5			I	V
		$T_{MIN} < T_A < T_{MAX}$	5			III	V
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	II	nA
		$T_{MIN} < T_A < T_{MAX}$			50	III	nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$			50	III	nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA < I_C < 2 mA T_A = 25°C		1		V	Ω

Note 1: ΔV_{BE} and ΔH_{fe} are measured between each of six possible pairs of transistors.
Note 2: ΔH_{fe} is calculated based on the difference divided by the larger of the two readings.
Note 3: Applies to all four transistors.
Note 4: Estimated from log conformity.

Typical Performance Curves

20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



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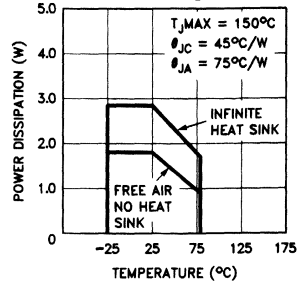
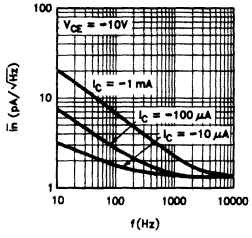
14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature

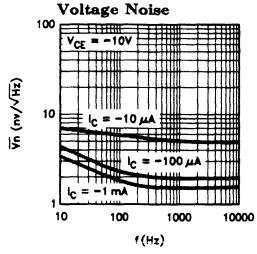


2015-12

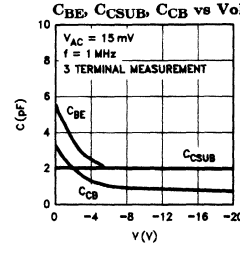
Current Noise



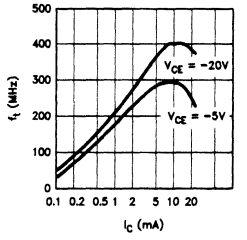
Voltage Noise



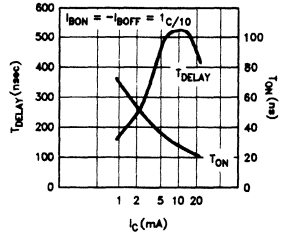
C_{BE}, C_{CSUB}, C_{CB} vs Voltage



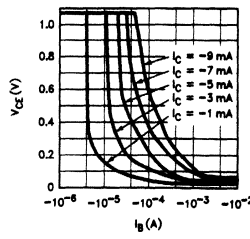
f_t vs I_C



T_{DELAY} and T_{ON} vs I_C



$V_{CE\,SAT}$ vs I_B



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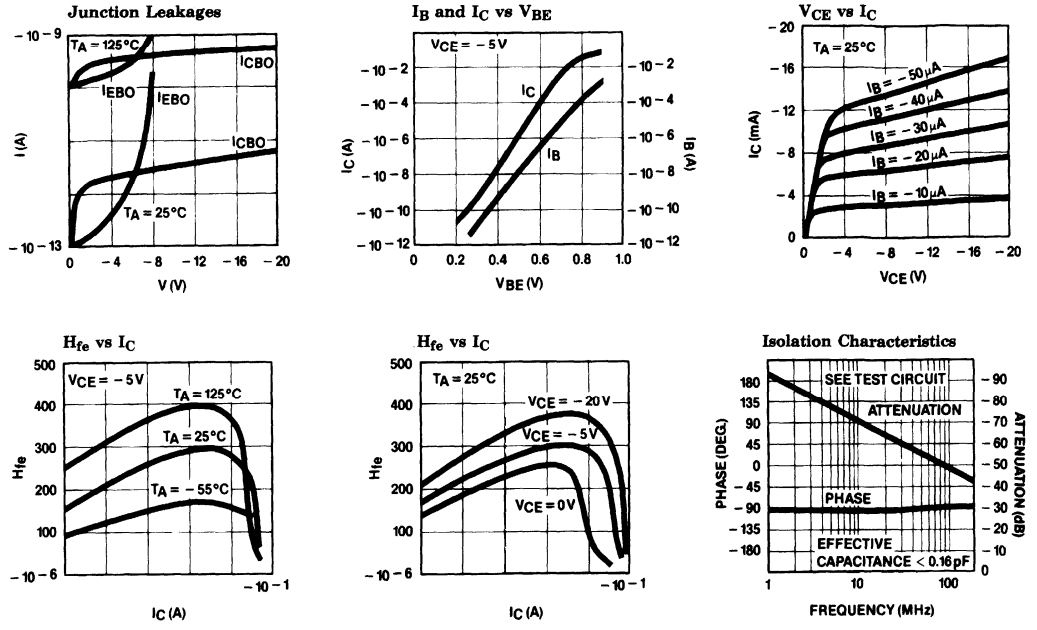
EP2015C/EP2015AC
Fast Quad PNP Array

Typical Performance Curves — Contd.



2015-5

EP2015 PSPICE® Model

IS = 8E − 15 BF = 300 VA = 47 IK = 0.03
XTB = 1.3 BR = 4.5 TF = 0.3N TR = 280N
RB = 230 RC = 170 ISE = 1E − 15 NE = 1.24
CCS = 2P MS = 0 CJC = 3.7P PC = 0.5 MC = 0.45
CJE = 5.4P PE = 0.6 ME = 0.33 PTF = 15

Note that for the above model the maximum "soft" saturation collector RC is used. For "hard" saturation modeling set RC ≈ 9.

PSPICE® is a registered trademark of MicroSim Corporation.

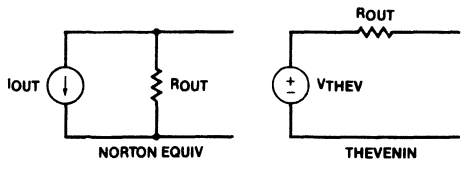
Matched NPN transistors have allowed system designers to make NPN current sinks. Now for the first time Elantec's fast matched PNP transistors are available. These make excellent, fast, matched current sources. The advantages of using current sources as active loads, instead of pullup resistors include:

- Faster, linear pull up (Not exponential)
- High output resistance (This increases voltage gain in many applications)

Current Sources and Current Mirrors

Current sinks and current mirrors have long been a tool available to the designer of monolithic ICs.

The Norton and Thevenin equivalent circuits of a current source are:



2015-6

And $V_{THEV} = I_{OUT} \times R_{OUT}$

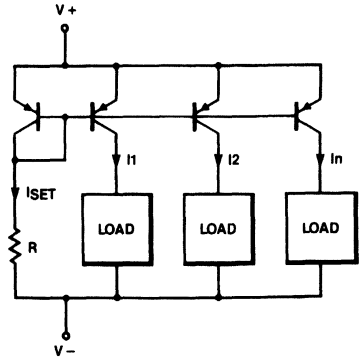
Four examples of current mirrors are shown, along with some of the advantages and limitations of each topology. For a more thorough discussion see "Analysis and Design of Analog Integrated Circuits" by Grey & Meyer (Wiley 1984), pages 233–247.

All current sources are only as good as the transistors that make them. If the transistors' V_{BE} match is 5 mV the output current would have a 20% error.

All current sources shown can be improved by putting a resistor in series with the topmost emitters. A 250 mV drop across these resistors reduces a 5 mV V_{BE} mismatch to a 2% current error. This has the added benefit of increasing output resistance. Elantec can guarantee a 1 mV V_{BE} match so resistors may not be necessary.

Basic Current Source

The Basic Current Mirror is simple and works well at low currents. Its limitations are low output resistance and it is not as fast as the Wilson.



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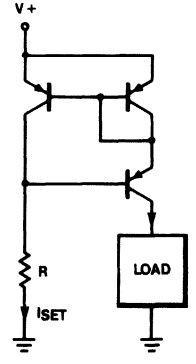
$$I_{SET} \approx \frac{((V+) - (V-)) - V_{BE}}{R}$$

$$I1 = I2 = In = \frac{\beta I1}{\beta + n + 1}$$

$$R_{OUT} = \frac{V_A}{I_{OUT}} = \frac{\text{EARLY VOLTAGE}}{I_{OUT}} = r_o$$

PNP Wilson Current Mirror

The Wilson is the best Current Mirror for high frequency applications, and it has plenty of output resistance.



$$I_{OUT} \approx I_{REF}\left(1 - \frac{2}{\beta^2 + 2\beta + 2}\right)$$

$$R_{OUT} \approx \frac{\beta r_o}{2}$$

$$V_{THEV} \approx \frac{\beta V_A}{2}$$

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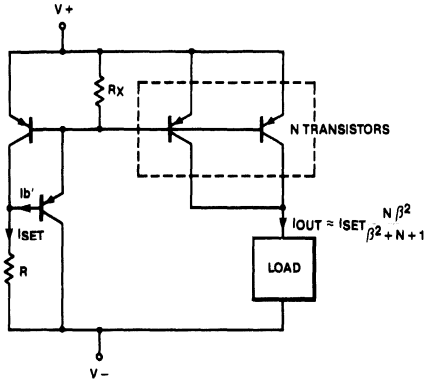
EP2015C/EP2015AC
Fast Quad PNP Array

Precision Current Source

The Precision Current Source has excellent current match since the error reduction is proportional to β^2. It is slow to turn off since it has no base turn off current. The turn off speed can be increased by using R_X, at the expense of reduced accuracy.



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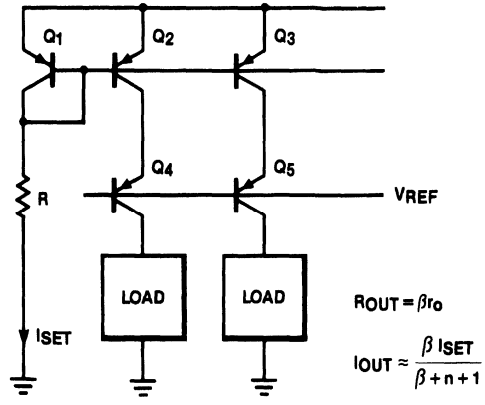
$$I_{SET} \approx \frac{((V+) - (V-)) - 2(V_{BE})}{R}$$

$$I_{OUT} \approx I_{SET} \frac{N\beta^2}{\beta^2 + N + 1}$$

$$R_{OUT} = \frac{V_A}{I_{OUT}}$$

Cascode Current Source

The Cascode Current Source is a basic current mirror with a common base transistor in the collector. This makes V_{CE} relatively constant for the mirror transistors and greatly increases the output resistance. This has good high frequency characteristics. Note that Q4 and Q5 can be in a package separate from Q1, Q2 and Q3.



2015-10

EP2015 Macromodel

```
* Connections:      q1c
*                   |    q1b
*                   |    |    q1e
*                   |    |    |    q2c
*                   |    |    |    |    q2b
*                   |    |    |    |    |    q2e
*                   |    |    |    |    |    |    q3c
*                   |    |    |    |    |    |    |    q3b
*                   |    |    |    |    |    |    |    |    q3e
*                   |    |    |    |    |    |    |    |    |    q4c
*                   |    |    |    |    |    |    |    |    |    |    q4b
*                   |    |    |    |    |    |    |    |    |    |    |    q4e
*                   |    |    |    |    |    |    |    |    |    |    |    |
.subckt em2015       1    2    3    7    6    5    8    9    10   14   13   12
* Models
.model ep2015 pnp (is=8e-15 bf=300 va=47 ikf=30mA xtb=1.3 br=4.5 tf=0.3nS
+tr=280nS rb=230 rc=170 ise=1e-15 ne=1.24 ccs=2pF cjc=3.7pF pc=0.5
+mc=0.45 cje=5.4pF pe=0.6 me=0.33 ptf=15)
* Transistors
q1 1 2 3 ep2015
q2 7 6 5 ep2015
q3 8 9 10 ep2015
q4 14 13 12 ep2015
.ends
```

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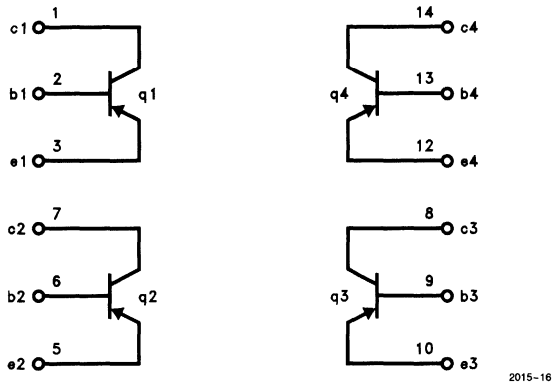
EP2015C/EP2015AC
Fast Quad PNP Array

EP2015 Macromodel — Contd.



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élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EN2016C
Fast Quad NPN Array

Features

- Four independent fast NPN's
- 350 MHz f_t
- Tight V_{be} matching—1 mV
- Tight H_{fe} matching—5%
- One chip construction with dielectric isolation
- Excellent thermal tracking
- High H_{fe}—150 minimum
- 40V minimum BV_{ceo}
- Each transistor similar to 2N3904
- Pin compatible with TPQ3904 and MPQ3904

Applications

- Current sources
- Current mirrors
- Log amplifiers
- Multipliers

Ordering Information

Part No.	Temp. Range	Package	Outline #
EN2016CN	0°C to +75°C	P-DIP	MDP0031
EN2016CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EN2016 family are quad monolithic vertical NPN transistor arrays which offer excellent parametric matching and high speed performance. The 350 MHz f_t provides AC performance similar to 2N3904 class devices. Manufactured on Elantec's Complementary Bipolar process, these transistors are electrically isolated from each other by a layer of oxide. The resulting low collector to substrate capacitance allows very high speed performance with minimal crosstalk. In addition, complete DC isolation is achieved. Substrate biasing is not required for normal operation, however for optimum high speed performance the substrate should be grounded. One-chip construction insures excellent parameter matching and tracking over temperature.

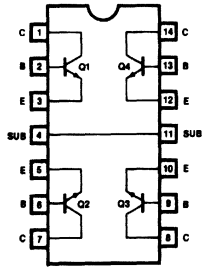
The low cost EN2016C is specified at 25°C. The EN2016C is available in either 14-pin plastic dual-in-line or 20-lead small outline packages.

For information on a complementary PNP transistor array, see Elantec's EP2015 family data sheet.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. For information on Elantec's processing, request our brochure: QRA1: *Elantec's Processing—Monolithic Products.*

Connection Diagrams

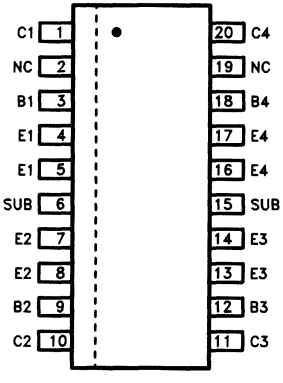
14-Lead DIP



2016-1

Top View

20-Lead SOL



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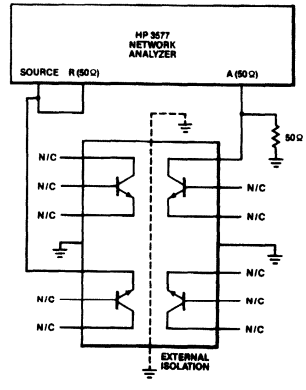
Top View

Isolation Characteristics Test Circuit



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EN2016C
Fast Quad NPN Array

Absolute Maximum Ratings

P_D	Power Dissipation	
	Each Transistor	500 mW (T_A = 25°C)
	Total Package	1.25W (T_A = 25°C)
T_A	Operating Temperature Range	0°C to +75°C
T_{ST}	Storage Temperature	−65°C to +150°C
T_J	Maximum Junction Temperature	150°C

Lead Temperature	
SOL Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
(Soldering, < 10 seconds)	300°C
V_{cb} MAX	40V
V_{eb} MAX	5V
V_{ce} MAX	40V
I_c MAX	50 mA
I_b MAX	10 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics

Parameter	Description	Test Conditions	EN2016C				Units
			Min	Typ	Max	Test Level	
ΔV_{BE}	(Note 1)	V_{CE} = 4V, I_C = 1 mA, T_A = 25°C			5	I	mV
		$T_{MIN} < T_A < T_{MAX}$					mV
ΔH_{fe1}	(Notes 1, 2)	V_{CE} = 1V, I_C = 1.0 mA, T_A = 25°C			10	I	%
		$T_{MIN} < T_A < T_{MAX}$					%
ΔH_{fe2}	(Notes 1, 2)	V_{CE} = 1V, I_C = 10 mA, T_A = 25°C			10	I	%
		$T_{MIN} < T_A < T_{MAX}$					%
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 1.0 mA, T_A = 25°C	75			I	
		$T_{MIN} < T_A < T_{MAX}$					

Electrical Characteristics — Contd.

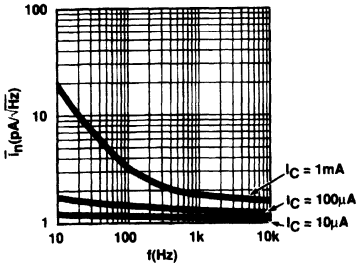
Parameter	Description	Test Conditions	EN2016C				Units
			Min	Typ	Max	Test Level	
H_{fe2}	(Note 3)	V_{CE} = 1V, I_C = 10 mA T_A = 25°C	75			I	
		$T_{MIN} < T_A < T_{MAX}$					
V_{BEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.90	I	V
		$T_{MIN} < T_A < T_{MAX}$					V
V_{CEsat}	(Note 3)	I_C = 10 mA, I_B = 1 mA T_A = 25°C			0.20	I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{ceo}	(Note 3)	I_C = 1 mA, I_B = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{cbo}	(Note 3)	I_C = 10 μA, I_E = 0 mA T_A = 25°C	40			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
BV_{ebo}	(Note 3)	I_B = 10 μA, I_C = 0 mA T_A = 25°C	5			I	V
		$T_{MIN} < T_A < T_{MAX}$					V
I_{cbo}	(Note 3)	V_{CB} = 30V, I_E = 0 mA T_A = 25°C			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$					nA
I_{ebo}	(Note 3)	V_{CE} = 4V, I_C = 0 mA T_A = 25°C			50	I	nA
		$T_{MIN} < T_A < T_{MAX}$					nA
f_t	(Note 3)	V_{CE} = 20V, I_C = 10 mA T_A = 25°C		350		V	MHz
r_{BE}	(Notes 3, 4)	10 μA < I_C < 2 mA T_A = 25°C		1		V	Ω

Note 1: ΔV_{BE} and ΔH_{fe} are measured between each of six possible pairs of transistors.
Note 2: ΔH_{fe} is calculated based on the difference divided by the larger of the two readings.
Note 3: Applies to all four transistors.
Note 4: Estimated from log conformity.

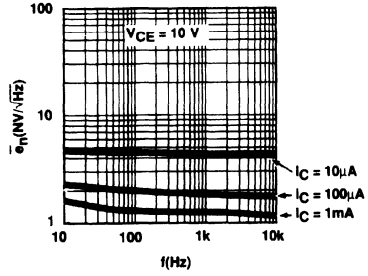
EN2016C
Fast Quad NPN Array

Typical Performance Curves

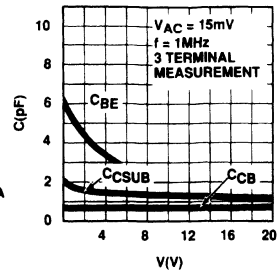
Current Noise



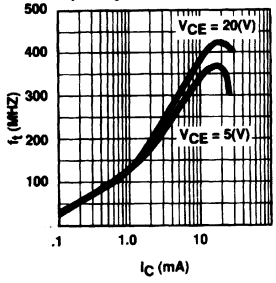
Voltage Noise



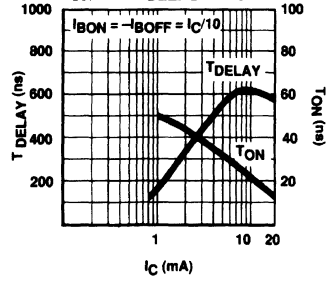
C_{BE}, C_{CSUB}, C_{CB} vs Voltage



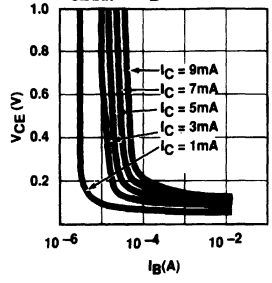
f_t vs I_C



T_{ON} and T_{DELAY} vs I_C

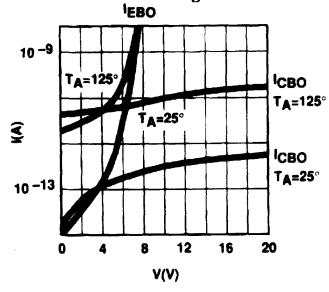


$V_{CE\,Sat}$ vs I_B

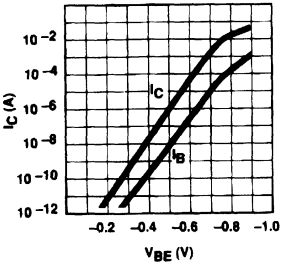


2016-4

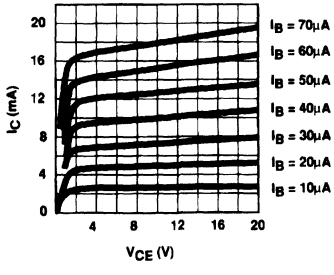
Junction Leakages



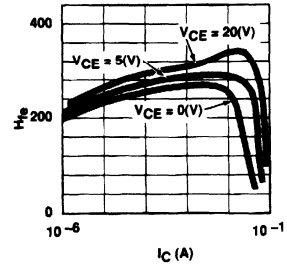
I_B and I_C vs V_{BE}



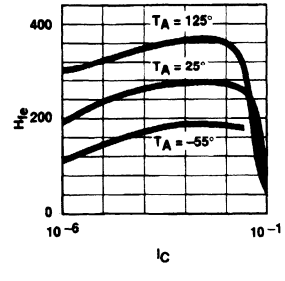
V_{CE} vs I_C



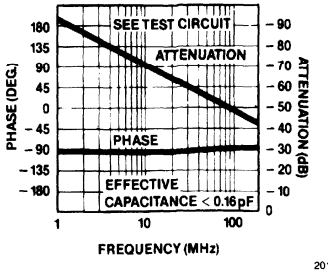
H_{fe} vs I_C



H_{fe} vs I_C



Isolation Characteristics



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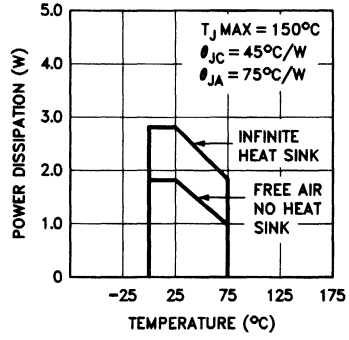
Typical Performance Curves — Contd.

14-Lead Plastic DIP
Maximum Power Dissipation
vs Ambient Temperature



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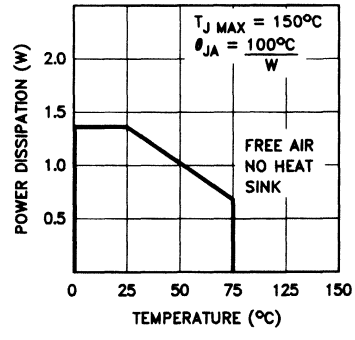
20-Lead SOL
Maximum Power Dissipation
vs Ambient Temperature



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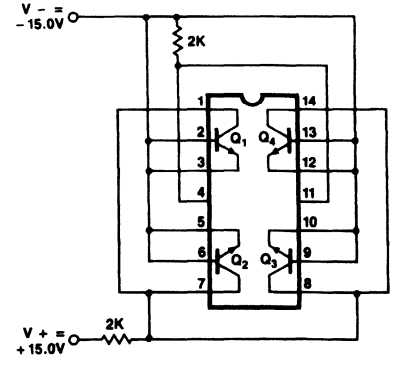
Note that for the above model the maximum "soft" saturation collector RC is used. For hard saturation set RC = 8.
PSPICE® is a registered trademark of Microsim Corporation.

EN2016 PSPICE® Model

NPN IS = 4E − 15 BF = 250 VA = 80 IK = 0.12
XTB = 1.1 BR = 10 TF = 0.35N TR = 80N
RB = 200 RC = 150 ISE = 3E − 14 NE = 2
CCS = 0.7P MS = 0 CJC = 2.4P XCJC = 0.3
PC = 0.32 MC = 0.19 CJE = 6P PE = 0.63
ME = 0.30 PTF = 15

Burn-In Circuit

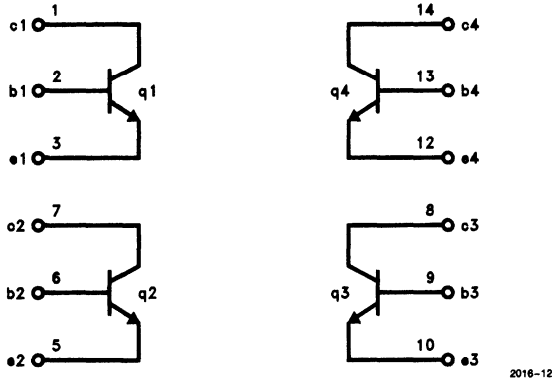


2016-8

EN2016C
Fast Quad NPN Array

EN2016 Macromodel

```
* Connections:      q1c
*                   |   q1b
*                   |   |   q1e
*                   |   |   |   q2c
*                   |   |   |   |   q2b
*                   |   |   |   |   |   q2e
*                   |   |   |   |   |   |   q3c
*                   |   |   |   |   |   |   |   q3b
*                   |   |   |   |   |   |   |   |   q3e
*                   |   |   |   |   |   |   |   |   |   q4c
*                   |   |   |   |   |   |   |   |   |   |   q4b
*                   |   |   |   |   |   |   |   |   |   |   |   q4e
*                   |   |   |   |   |   |   |   |   |   |   |   |
.subckt em2016      1   2   3   7   6   5   8   9   10  14  13  12
* Models
.model en2016 npn (is=4e-15 bf=250 va=80 ikf=120mA xtb=1.1 br=10 tf=0.35nS
+tr=80nS rb=200 rc=150 ise=3e-14 ne=2 ccs=0.7pF cjc=2.4pF xcjc=0.3 pc=0.32
+mc=0.19 cje=6pF pe=0.63 me=0.30 ptf=15)
* Transistors
q1 1 2 3 en2016
q2 7 6 5 en2016
q3 8 9 10 en2016
q4 14 13 12 en2016
.ends
```



Hybrid ICs

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

AMPLIFIERS

*Listed in order of decreasing bandwidth

ELANTEC Part Number	Description	Temp. Range	Min. A_{VOL} Over Temp.	Max. Offset Voltage		Max. Bias Current°C		*Gain Bandwidth Product Typical @A_V = xx (or f_{3dB})	Min. Slew Rate 25 Comp for A_v = xx)	Continuous Output Current	Max I_{CC} (Full Temp.)	Packages
				25°C	Over Temp.	25°C	Over Temp.					
EL2006C/ 883 or DESC	Much Improved ELH0032 Hybrid, FET Input ELH0032 Pinout	−25°C to +85°C −55°C to +125°C	74 dB	3 mV	5.5 mV	100 pA	10 nA	500 MHz (A_V = 20)	350 V/μs (A_V = 1)	±100 mA Min.	23 mA	12-Pin TO-8
ELH0032/ 883 or DESC	Hybrid, see also EL2006 Industry Standard Pinout FET Input	−55°C to +125°C	45 dB	5 mV	10 mV	1 nA	50 nA	360 MHz (A_V = 20)	350 V/μs (A_V = 1)	Power Limited ±100 mA Min.	23 mA	12-Pin TO-3
ELH0101/ 883 or DESC	Hybrid, Industry Standard Pinout Power Op-Amp	−55° to +125°C	100 dB	3 mV	7 mV	300 nA	60 nA	4 MHz (A_V = 1)	7.5V/μs (A_V = 1)	±2.1A Min	35 mA	8-Pin TO-3
ELH0021 883 or DESC	Hybrid, Industry Standard Pinout Power Op-Amp	−55°C to +125°C	100 dB	3 mV	5 mV	300 nA	1 μA	1 MHz (A_V = 1)	1.5V/μs (A_V = 1)	±1.1A Min.	4 mA	8-Pin TO-3
ELH0041/ 883 or DESC	Hybrid, Industry Standard Pinout Power Op-Amp	−55°C to +125°C	100 dB	3 mV	5 mV	300 nA	1 μA	1 MHz (A_V = 1)	1.5V/μs (A_V = 1)	±200 mA Typ.	4 mA	12-Pin TO-8

Note: Some specifications in table are for the best version available.
Consult individual data sheets for product details.

BUFFERS
*Listed in order of decreasing bandwidth

ELANTEC Part Number	Description	Full Temp Warmed Up Input Current (Input Impedance)	Continuous Output Current Drive (Peak Output Current)	Typical −3 dB* Bandwidth (Risetime)	Typical Slew Rate	Max Supply Current	Packages
EL2004C/ 883 or DESC	350 MHz FET INPUT BUFFER, Improved ELH0033, Hybrid	10 nA Max (100 MΩ Min)	±90 mA Min (±250 mA)	350 MHz (1 ns)	2500V/μs	24 mA	12-Pin TO-8
ELA2005C/ 883 or DESC	Precision FET INPUT BUFFER, Improved ELH0033, Hybrid	5 nA Max (10,000 MΩ Min)	±90 mA Min (±250 mA)	140 MHz (2.5 ns)	1500V/μs	24 mA	12-Pin TO-8
ELH0033/ 883 or DESC	Hybrid, FET Input "Industry Standard" Pinout, See Also EL2004, EL2005	2.5 nA Max (10,000 MΩ Min)	±100 mA Min (±250 mA)	100 MHz (2.9 ns Typ)	1500V/μs	24 mA	12-Pin To-8
ELH0002/ 883 or DESC	Hybrid "Industry Standard" Pinout, See Also EL2003	±10 μA Max (180 kΩ Min)	±100 mA Min (±400 mA)	30 MHz (12 ns)	200V/μs	10 mA	8-Pin TO-5

Note: Some specifications in table are for the best version available.
Consult individual data sheets for product details.

DESC/SMD Drawings

Elantec is an active participant in the DESC/SMD Drawing standardization program. This is a program administered by the Defense Electronics Supply Center (DESC) in Dayton, Ohio. Under this program, a MIL-STD-1772 certified manufacturer, such as Elantec, may supply hybrid devices to many customers using one government controlled specification instead of having each customer create his own Source Control Drawing (SCD). Elantec treats these devices as standard parts, i.e., they are built to be inventoried at both Elantec and our distributors in anticipation of customer orders rather than being built to order. This practice lowers costs, shortens lead times, and improves quality.

At publication time, this is the list of devices for which Elantec is an approved supplier:

DESC/SMD Drawing Number	Generic Part Number
7801301X	ELH0002H/883B
8001301ZA	ELH0032G/883B
8001401ZA	ELH0033G/883B
8508701ZA	ELH0041G/883B
8508801YA	ELH0021K/883B
8508901YA	ELH0101AK/883B
8508902YA	ELH0101K/883B

Features

- Slew rate—2500 V/μs
- Rise time—1 ns
- Bandwidth—350 MHz
- ELH0033—pin compatible
- ±5 to ±15V operation
- 100 mA output current
- MIL-STD-883B Rev. C devices manufactured in U.S.A.

Applications

- Coaxial cable driver
- Fast op amp booster
- Flash converter driver
- Video line driver
- High-speed sample and hold
- Pulse transformer driver
- A.T.E. pin driver

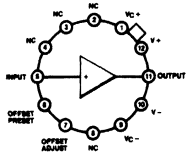
Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2004CG	−25°C to +85°C	TO-8	MDP0002
EL2004G	−55°C to +125°C	TO-8	MDP0002
EL2004L	−55°C to +125°C	52-Pad LCC	MDP0013
EL2004L/MIL	−55°C to +125°C	52-Pad LCC	MDP0013

5962-89659 is the SMD version of this device.

Connection Diagram

Case is Electrically Isolated



2004-1

Top View

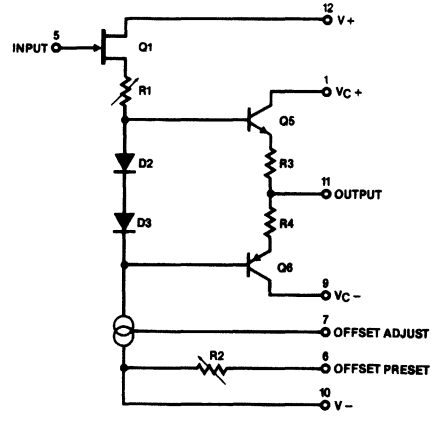
General Description

The EL2004 is a very high-speed, FET input buffer/line driver designed for unity gain applications at both high current (up to 100 mA) and at frequencies up to 350 MHz. The 2500 V/μs slew rate and wide bandwidth ensures the stability of the circuit when the EL2004 is used inside op amp feedback loops.

Applications for the EL2004 include line drivers, video buffers, wideband instrumentation, and high-speed drivers for inductive and capacitive loads. The performance of the EL2004 makes it an ideal buffer for video applications including input buffers for flash A/D converters, and output buffers for video DACs. Its excellent phase linearity is particularly advantageous in digital signal processing applications.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



2004-3

EL2004/EL2004C
350 MHz FET Buffer

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	40V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	40V		EL2004	−55°C to +125°C
P_D	Power Dissipation (See curves)	1.5W		EL2004C	−25°C to +85°C
I_{OC}	Continuous Output Current	±100 mA	T_J	Operating Junction Temperature	175°C
I_{OP}	Peak Output Current	±250 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

±15V DC Electrical Characteristics

V_S = ±15V, $T_{MIN} < T_A < T_{MAX}$, V_{IN} = 0V, R_L = 1 kΩ unless otherwise specified (Note 1)

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \le 100$ kΩ, T_J = 25°C		5	10	I		12	20	I	mV
		$R_S \le 100$ kΩ			15	I			25	III	mV
A_V	Voltage Gain	V_{IN} = ±10V	0.97	0.98	1.0	I	0.96	0.98	1.0	II	V/V
		R_L = 100Ω, V_{IN} = ±10V	0.92	0.95	0.98	I	0.90	0.95	0.98	II	V/V
R_{IN}	Input Impedance	T_J = 25°C, V_{IN} = ±1V	10^8	10^{11}		I	10^8	10^{11}		I	Ω
R_{OUT}	Output Impedance	V_{IN} = ±1 V_{DC}, ΔR_L = 100Ω to Infinity		4	8	I		4	10	II	Ω
V_O	Output Voltage Swing	V_{IN} = ±14V	±12	±13		I	±12	±13		II	V
		V_{IN} = ±10.5V, R_L = 100Ω T_A = 25°C	±9	±9.8		I	±9	±9.8		I	V
I_{IN}	Input Current	T_J = 25°C (Note 2)			0.25	I			2.0	I	nA
		T_A = 25°C (Note 3)			2.5	IV			20	IV	nA
		$T_J = T_A = T_{MAX}$			10	I			50	III	nA
		V_{IN} = −10V		20		V		20		V	nA
I_S	Supply Current			20	24	I		20	24	II	mA

±5V DC Electrical Characteristics

V_S = ±5V, $T_{MIN} < T_A < T_{MAX}$, V_{IN} = 0V, R_L = 50Ω unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \leq 100\,k\Omega$, T_J = 25°C		10	30	I		10	30	I	mV
		$R_S \leq 100\,k\Omega$			35	I			35	III	mV
A_V	Voltage Gain	V_{IN} = ±1V, R_L = 1 kΩ	0.90	0.95	1.0	I	0.90	0.95	1.0	II	V/V
		V_{IN} = ±1V	0.80	0.88	0.95	I	0.80	0.88	0.95	II	V/V
R_{IN}	Input Impedance	T_J = 25°C, V_{IN} = ±1V	10^8	10^{11}		I	10^{10}	10^{11}		I	Ω
R_{OUT}	Output Impedance	V_{IN} = ±1 V_{DC}, ΔR_L = 50Ω to Infinity		4	8	I		4	10	II	Ω
V_O	Output Voltage Swing	V_{IN} = ±4V	±2.0	±2.9		I	±2.0	±2.9		III	V
I_{IN}	Input Current	T_J = 25°C (Note 2)			250	I			500	I	pA
		T_A = 25°C (Note 3)			2.5	IV			5	IV	nA
		$T_J = T_A = T_{MAX}$			10	I			20	III	nA
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V, R_L = 1 kΩ		60		V		60		V	dB
I_S	Supply Current	R_L = 1 kΩ		17.5	20	I		17.5	20	II	mA

Note 1: When operating at elevated temperatures the power dissipation of the EL2004 must be limited to the values shown in the typical performance curve "Maximum Power Dissipation vs Temperature". Junction to case thermal resistance is 31°C/W when dissipation is spread among the transistors in a normal AC steady-state condition. In special conditions where heat is concentrated in one output device, junction temperature should be calculated using a thermal resistance of 70°C/W.

Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures will exceed the value at T_J = 25°C. When supply voltages are ±15V, no-load operating junction temperatures may rise 40°C to 60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_{IN} will change significantly during warm-up. Refer to I_{IN} vs Temperature graph for expected values.

Note 3: Measured in still air seven minutes after application of power. See graph of Input Current During Warm-up for further information.

Note 4: Bandwidth is calculated from the rise time. The EL2004 has a single pole gain and phase response up to the −3 dB frequency.

Note 5: Slew rate is measured between V_{OUT} = +2.5V and −2.5V for this test.

Note 6: Slew rate is measured between V_{OUT} = +1V and −1V for this test. Pulse repetition rate is <50 MHz.

±15V AC Electrical Characteristics

V_S = ±15V, R_L = 1 kΩ, R_S = 50Ω, T_J = 25°C unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
BW	Bandwidth	(Note 4)	200	350		I	200	350		I	MHz
		R_L = 50Ω	140	200		I	140	200		I	MHz
t_s	Settling Time to 1%	ΔV_{IN} = 1V, t_r = 3 ns		6		V		6		V	ns
C_{in}	Input Capacitance			3		V		3		V	pF

9

EL2004/EL2004C
350 MHz FET Buffer

±15V AC Electrical Characteristics

V_S = ±15V, R_L = 1 kΩ, R_S = 50Ω, T_J = 25°C unless otherwise specified — Contd.

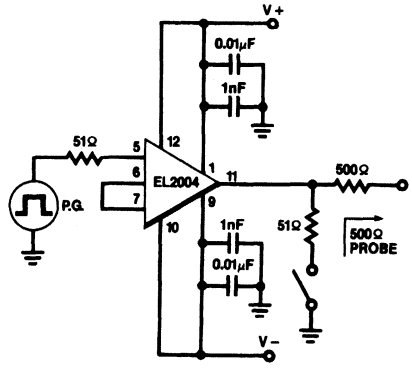
Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	V_{IN} = ±5V (Note 5)	2000	2500		I	2000	2500		I	V/μs
		C_L = 100 pF, V_{IN} = ±5V (Note 5)		1200		V		1200		V	V/μs
t_r	Rise Time Note: See Test Figure	ΔV_{IN} ∿ 0.6V		1.0	1.7	I		1.0	1.7	I	ns
		ΔV_{IN} ∿ 0.6V, R_L = 50Ω		1.7	2.5	I		1.7	2.5	I	ns
t_p	Propagation Delay Note: See Test Figure	ΔV_{IN} ∿ 0.6V		1.0	2.0	I		1.0	2.0	I	ns
R_{OUT}	Output Impedance	f = 1 MHz, V_{IN} = 1 V_{RMS} ΔR_L = 100Ω to Infinity		4		V		4		V	Ω
+PSRR	Power Supply Rejection Ratio	ΔV_S+ = ±1.5 V_{peak} f = 1 kHz		40		V		40		V	dB
−PSRR	Power Supply Rejection Ratio	ΔV_S− = ±1.5 V_{peak} f = 1 kHz		40		V		40		V	dB

±5V AC Electrical Characteristics

V_S = ±5V, R_L = 50Ω, R_S = 50Ω, T_J = 25°C unless otherwise specified

Parameter	Description	Test Conditions	EL2004				EL2004C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
BW	Bandwidth	R_L = 1 kΩ	175	220		I	175	220		I	MHz
		(Note 4)	125	150		IV	125	150		IV	MHz
t_s	Settling Time to 1%	ΔV_{IN} = 1V, t_r = 3 ns		8		V		8		V	ns
C_{in}	Input Capacitance			3		V		3		V	pF
SR	Slew Rate	V_{IN} = ±2V (Note 6)	900	1200		I	900	1200		I	V/μs
		C_L = 100 pF, V_{IN} = ±2V R_L = 1 kΩ (Note 6)		500		V		500		V	V/μs
t_r	Rise Time Note: See Test Figure	R_L = 1 kΩ, ΔV_{IN} ∿ 0.6V		1.6	2.0	I		1.6	2.0	I	ns
		R_L = 50Ω, ΔV_{IN} ∿ 0.6V		2.3	2.8	IV		2.3	2.8	IV	ns
t_p	Propagation Delay Note: See Test Figure	R_L = 1 kΩ, ΔV_{IN} ∿ 0.6V		1.2	2.4	I		1.2	2.4	I	ns
R_{OUT}	Output Impedance	f = 1 MHz, V_{IN} = 1 V_{RMS} ΔR_L = 100Ω to Infinity		4		V		4		V	Ω
+PSRR	Power Supply Rejection Ratio	ΔV_S− = ±0.5 V_{peak} f = 1 kHz		30		V		30		V	dB
−PSRR	Power Supply Rejection Ratio	ΔV_S+ = ±0.5 V_{peak} f = 1 kHz		30		V		30		V	dB

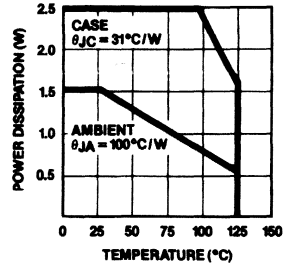
AC Test Circuit



2004-4

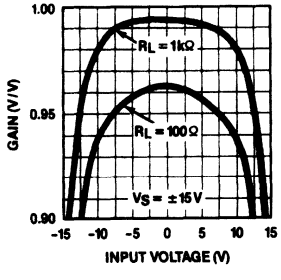
Typical Performance Curves

TO-8
Maximum Power
Dissipation

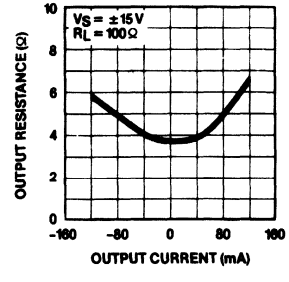


2004-5

Gain vs Input Voltage



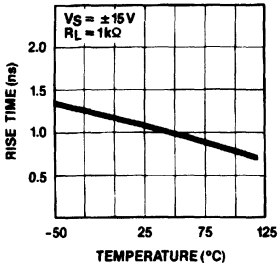
Output Resistance vs
Output Current



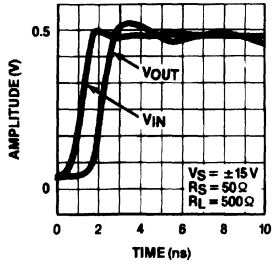
2004-7

Typical Performance Curves — Contd.

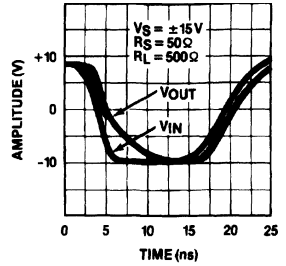
Rise Time vs Temperature



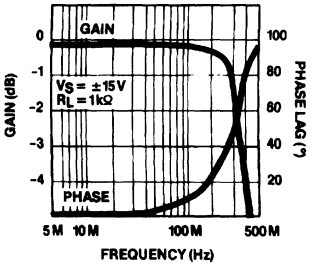
Small Signal Pulse Response



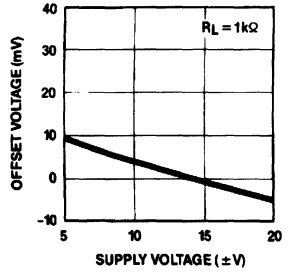
Large Signal Pulse Response



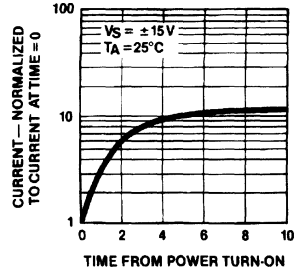
Frequency Response



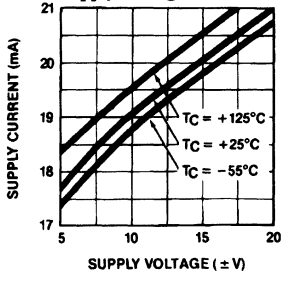
Offset Voltage vs Supply Voltage



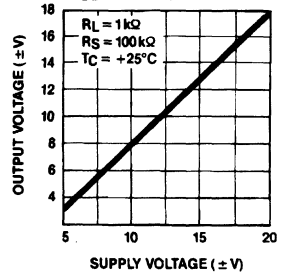
Normalized Input Bias Current During Warm-up



Supply Current vs Supply Voltage



Output Voltage vs Supply Voltage



2004-8

Applications Information

The EL2004 is one member of a family of high performance buffers manufactured by Elantec. The 2004 is optimized for speed while others offer choices of input DC parameters or output drive or cost. The following table illustrates those members available at the time of this printing. Consult the factory for the latest capabilities in this developing line.

Elantec's Buffer Family

Part #	Slew Rate V/μs	Bandwidth MHz	Input Current (Warm)	Peak I_{OUT} mA	Rise Time ns
ELH0002	200	50	6 μA	400	7
ELH0033	1500	100	2.5 nA	250	2.9
EL2004	2500	350	2.5 nA	250	1.0
EL2005	1500	140	0.1 nA	250	2.5

Recommended Layout Precautions

The very high-speed performance of the EL2004 can only be realized by taking certain precautions in circuit layout and power supply decoupling. Low inductance ceramic chip or disc power supply decoupling capacitors of 0.1 μF or more should be connected with the shortest practical lead lengths between the device supply leads and a ground plane. In addition, it can be helpful to parallel these with 4.7 μF electrolytics (Tantalum preferred). Failure to follow these precautions can result in oscillation.

Circuit Operation

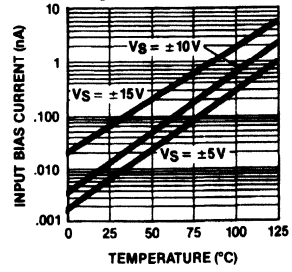
The EL2004 is effectively an ideal unity gain amplifier with almost infinite input impedance and about 6Ω output impedance.

Input Characteristics

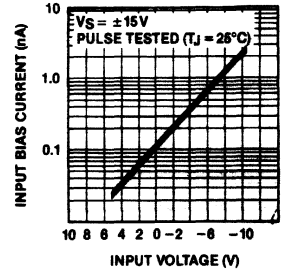
The input impedance of a junction FET is a strong function of temperature and input voltage. Nominal input resistance of EL2004 is 10^{12} at 25°C junction, but as I_B doubles every 11°C in the JFET, the input resistance falls. During warm-up, self-heating raises the junction temperature up to 60°C or more (without heatsink) so operating I_B will be much higher than the data sheet 25°C specification.

Another factor which can increase bias current is input voltage. If the input voltage is more than 20V below the positive supply, the input current rises exponentially. (See Curve.)

Input Bias Current vs Temperature



Input Bias Current vs Input Voltage



2004-9

In applications such as sample and hold circuits where it is important to maintain low input bias current over input voltage range, the EL2005 High Accuracy Fast Buffer is recommended.

The input capacitance of EL2004 comprises the FET device gate-to-source capacitance (which is a function of input voltage) and stray capacitance to the case. Effective input capacitance can be minimized by connecting the case to the output since it is electrically isolated. Or, for reduced radiation, the case may be grounded. The AC characteristics specified in this data sheet were obtained with the case floating.

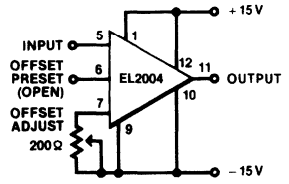
Offset Voltage Adjustment

The EL2004's offset voltages have been actively laser trimmed at ±15V supplies to meet specified limits when the offset adjust pin is shorted to the offset preset pin. If external offset null is required, the offset adjust pin should be connected to a 200Ω trim pot connected to the negative supply.

EL2004/EL2004C
350 MHz FET Buffer

Circuit Operation — Contd.

Offset Zero Adjust



2004-10

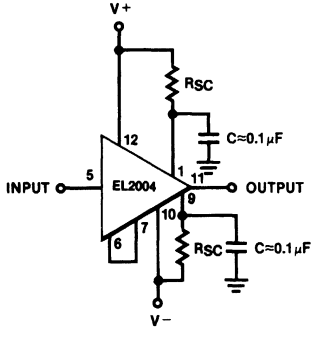
Capacitive Loading

The EL2004 is designed to drive capacitive loads up to several thousand picofarads without oscillation. However, peak current resulting from charging currents on fast edges should be limited below the absolute maximum peak current rating of 250 mA. In some cases it may be necessary to employ one of the current limit schemes shown below.

Short Circuit Protection

Dynamic response of the EL2004 was preserved by excluding current limit circuits which are not needed in most applications. However, in situations where operating conditions are not controlled, short circuit protection can be added by inserting resistors between the output device collectors and supplies as illustrated.

Using Resistor Current Limiting



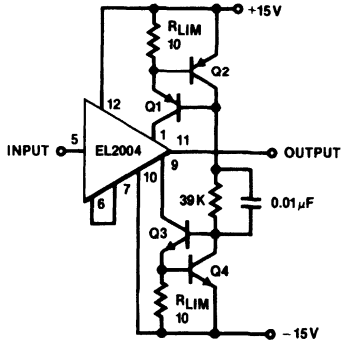
2004-11

Suitable resistor values can be calculated as follows:

$$R_{SC} = \frac{V+}{I_{SC}} = \frac{V-}{I_{SC}}$$

where $I_{SC} \leq 100$ mA for EL2004.

Current Limiting Using Current Sources



2004-12

The inclusion of limiting resistors in the collectors of the output devices will reduce the output voltage swing and speed. Decoupling V_C+ and V_C- pins with capacitors to ground will retain full output swing for transient pulses.

An alternate active current limit technique that retains full DC output swing is shown above. Here the current sources are saturated during normal operation thus applying full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as the current source reaches its limit.

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{100\ mA} = 6\Omega$$

Power Supplies

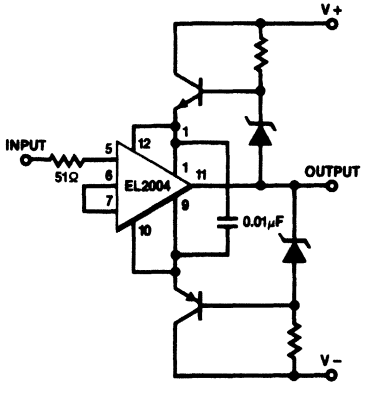
The EL2004 has been characterized for both ±15 and ±5V dual supply operation, but other combinations can also be useful. For example, in many video applications it is only necessary for the output to swing ±2V or less, but speed and distortion are important. In this situation, the input stage can be operated at the full ±15V supply while the output collectors are returned to ±5V. The speed and distortion will be almost as good as if the whole circuit was operating at ±15V, but the dissipation is substantially reduced and higher load currents can be safely accommodated.

Circuit Operation — Contd.

Increasing Operating Voltage and Reducing Thermal Tail

When driving heavy loads, the changing dissipation in the output transistors can sometimes cause temperature gradients in the circuit which cause a shift in offset voltage and the phenomenon known as "thermal tail". Bootstrapping the output as illustrated substantially reduces the power in the output transistors and mitigates the effect.

High Voltage Inputs can be Accommodated with Bootstrapped Supplies



2004-13

Hardware

In order to utilize the full drive capabilities of the EL2004, it should be mounted with a heatsink, particularly for extended temperature operation. Suitable heatsinks include Thermalloy 2240A (33°C/W), Wakefield 215CB (30°C/W) and IERC-UP-TO-848CB (15°C/W).

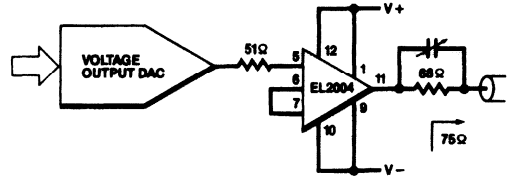
The case is isolated from the circuit and may be connected to system chassis. Sockets are not recommended as they add substantial inductance and capacitance which impair the performance of the device. However, for test purposes they are unavoidable and precautions such as shielding input from output are suggested.

General Application Suggestions

Video DAC Buffer

Many of the available video D to A converters are unable to directly drive 50Ω or 75Ω cables. The EL2004's excellent phase linearity at video frequencies make it an ideal solution. In critical applications or where line termination is not controlled, a matching pad should be used as shown. The capacitor should be adjusted for optimum pulse response. If properly layed out this circuit will not overshoot.

Video DAC Buffer

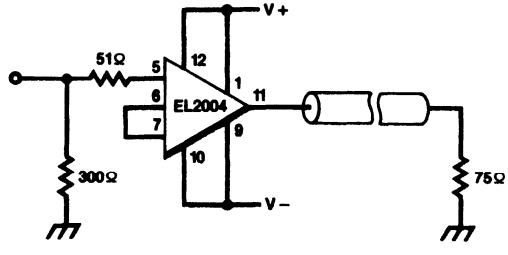


2004-14

Impedance Matching

The EL2004 provides power gain and isolation between source and load when used as an active tap or impedance matching device as illustrated here. In this example, there is no output matching pad between the 2004 and the 75Ω line. Such matching is not needed when the distant end of the cable is properly terminated as there is no reflected signal to worry about and the 2004 isolates the source. This technique allows the full output voltage of the EL2004 to be applied to the load.

Impedance Converter

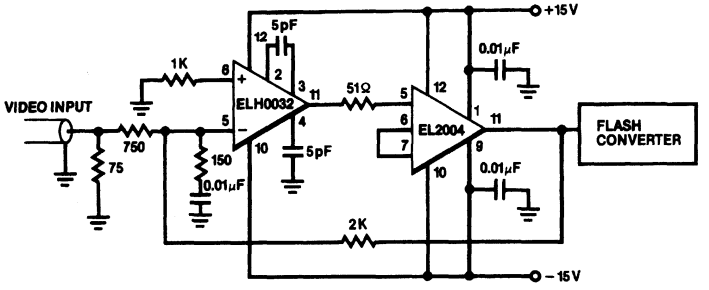


2004-15

9

General Application Suggestions — Contd.

Inverting Amplifier for 20 MHz Flash Converter

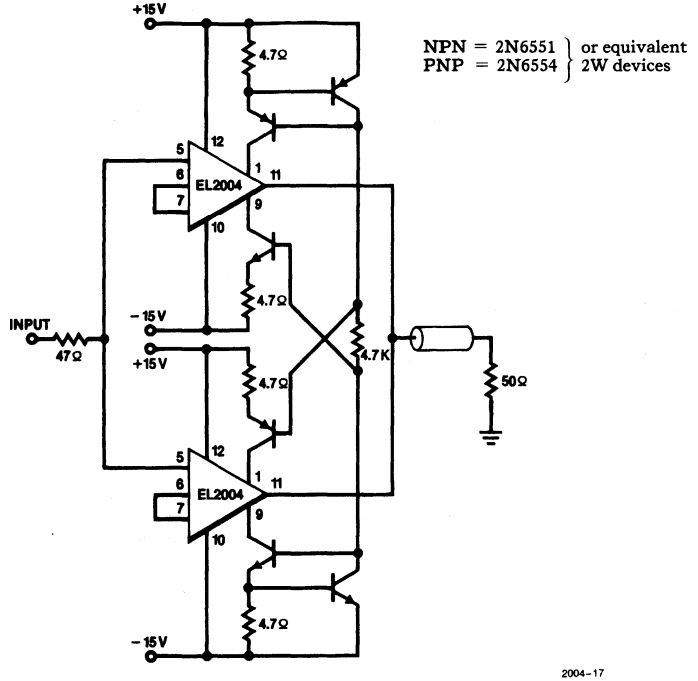


2004-16

Boosting the Output

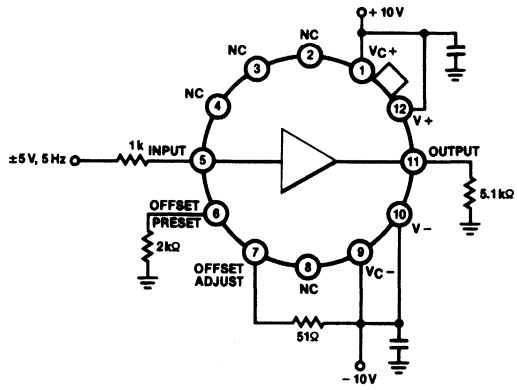
Unlike most integrated cicuits, two or more EL2004's can be paralleled for increased output drive. This capability results from the finite output resistance and low output mismatch of the EL2004. For example, a 50Ω cable driver with ±10V capability can be made by using two EL2004's. A short-circuit protected version is shown below.

50Ω Cable Driver with Short Circuit Protection



2004-17

Burn-In Circuit



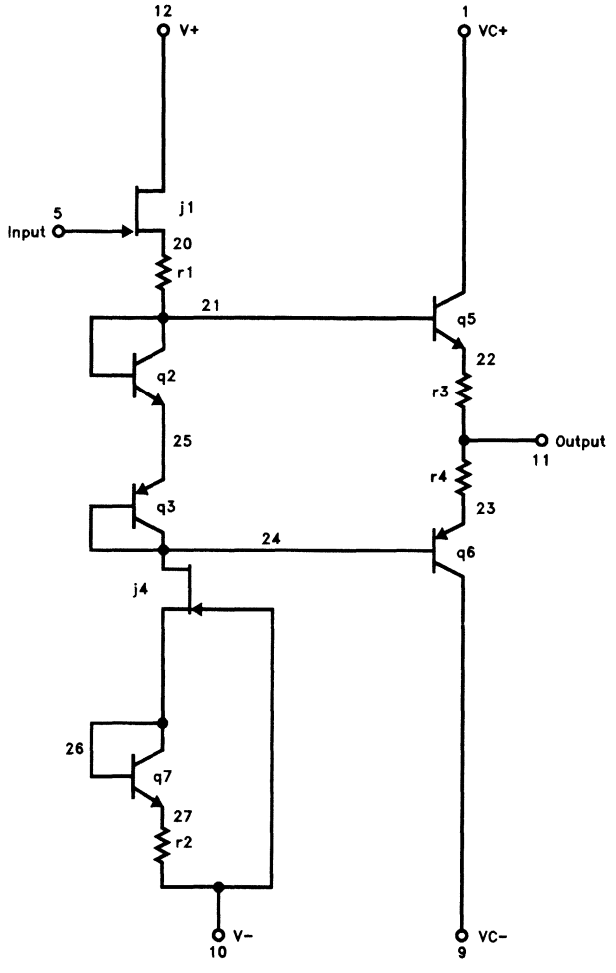
2004-18

Pin numbers are for TO-8 package.
LCC uses the same schematic.

EL2004 Macromodel

```
* Connections:  input
*               |     V+
*               |     |     Vc+
*               |     |     |     V-
*               |     |     |     |     Vc-
*               |     |     |     |     |     output
*               |     |     |     |     |     |
.subckt M2004   5     12    1     10    9     11
* Models
.model qn npn (is=5e-14 bf=150 vaf=100 rc=1 rb=5 re=1 ikf=200mA
+cje=5pF cjc=5pF mje=.42 mjc=.23 tf=.3nS tr=200nS br=5 vtf=0)
.model qp pnp (is=5e-14 bf=150 vaf=100 rc=2 rb=3 re=1 ikf=100mA
+cje=5.7pF cjc=4pF tf=.3nS mje=.32 mjc=.43 tr=170nS br=5 vtf=0)
.model qf njf (vto=-3V beta=4.0e-3 cgd=4pF cgs=10pF lambda=671.0e-6)
* Resistors
r1 20 21 58.33
r2 27 10 58.33
r3 22 11 2
r4 11 23 2
* Transistors
j1 12 5 20 qf
j4 24 10 26 qf
q2 21 21 25 qn
q3 24 24 25 qp
q5 1 21 22 qn
q6 9 24 23 qp
q7 26 26 27 qn
.ends
```

EL2004 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2005/EL2005C
High Accuracy Fast Buffer

Features

- Low input current—50 pA
- Low offset and drift—2 mV/25 μV/°C
- High slew rate—1500 V/μs
- Fast rise and fall time—2.5 ns
- High input resistance—1000 GΩ
- Bandwidth—140 MHz
- Pin compatible with ELH0033
- MIL-STD-883 Revision C devices manufactured in U.S.A.

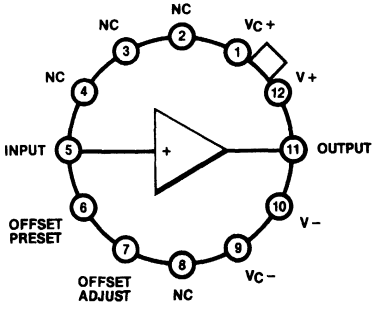
Advantages

- No input loading
- Input current independent of input voltage
- Eliminates offset adjustments
- Drives cables directly

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2005CG	−25°C to +85°C	TO-8	MDP0002
EL2005G	−55°C to +125°C	TO-8	MDP0002
EL2005G/883B	−55°C to +125°C	TO-8	MDP0002

Connection Diagram



Top View

Note: Case is electrically isolated.

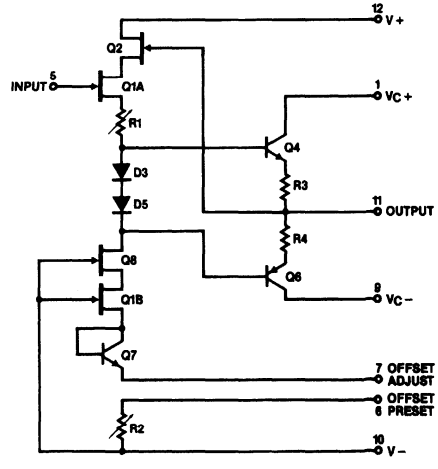
General Description

The EL2005 is a high-speed, FET input buffer similar to ELH0033 and EL2004 but with input specifications significantly improved over the previous types. The input stage employs a cascode configuration to maintain constant input characteristics over the full ±10V input range. The input looks like a 3 pF capacitor to ground in almost all cases since the DC bias current is constant with input voltage. In sample and hold circuits this results in an order of magnitude improvement in hold characteristics. Input offset voltage and offset voltage drift are also improved a factor of two over previous types.

These excellent DC characteristics are complemented by a wide 140 MHz bandwidth while the 1500 V/μs slew rate and excellent phase linearity of the ELH0033 family are preserved allowing direct plug-in replacement for upgraded performance. (For even faster operation see EL2004.)

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage (V+ − V−)	40V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	40V		EL2005	−55°C to +125°C
P_D	Power Dissipation (See curves)	1.5W		EL2005C	−25°C to +85°C
I_{OC}	Continuous Output Current	±100 mA	T_J	Operating Junction Temperature	175°C
I_{OP}	Peak Output Current	±250 mA	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, V_{IN} = 0V, $T_{MIN} \le T_A \le T_{MAX}$

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	$R_S \le 100$ kΩ, T_J = 25°C (Note 1)		2	5	I		3	10	I	mV
		$R_S \le 100$ kΩ			10	I			15	III	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Offset Voltage	R_S = 100Ω		25		V		25		V	μV/°C
PSRR	Supply Rejection	±10V ≤ V_S ≤ ±20V	65	75		I	60	75		II	dB
I_B	Input Bias Current	T_J = 25°C (Notes 1 and 3)		2	50	I		5	100	I	pA
		T_A = 25°C (Notes 2 and 3)		50	500	IV		100	1000	IV	pA
		$T_J = T_A = T_{MAX}$		2	5	I		0.5	5	III	nA
A_V	Voltage Gain	R_S = 100Ω, R_L = 1 kΩ, V_{IN} = ±10V	0.97	0.98	1.0	I	0.96	0.98	1.0	II	V/V
		R_S = 100Ω, R_L = 100Ω, v_{IN} = ±10V	0.88	0.95	0.98	I	0.88	0.95	0.99	II	V/V
R_{IN}	Input Impedance	R_L = 1 kΩ, −10V ≤ V_{IN} ≤ ±10V	2×10^9	10^{12}		I	2×10^9	10^{12}		IV	Ω
		T_J = 25°C (Note 1), R_L = 1 kΩ	10^{10}	10^{12}		I	10^{10}	10^{12}		I	Ω
R_O	Output Impedance	R_L = 1 kΩ, V_{IN} = ±1V		4	8	I		4	9	II	Ω

EL2005/EL2005C
High Accuracy Fast Buffer

DC Electrical Characteristics $V_S = \pm 15V, V_{IN} = 0V, T_{MIN} \leq T_A \leq T_{MAX}$ — Contd.

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	$V_{IN} = \pm 14V$, $R_L = 1 k\Omega$		±12.5		V		±12.5		V	V
		$V_{IN} = \pm 10.5V, R_L = 100\Omega$, $T_A = 25°C$	±9	±9.8		I	±9	±9.8		I	V
I_S	Supply Current	$V_{IN} = 0$ (Note 1)		19	22	I		19	24	II	mA
PD	Power Consumption	$V_{IN} = 0$		570	660	I		570	720	II	mW

AC Electrical Characteristics $T_C = 25°C, V_S = \pm 15V, R_S = 50\Omega, R_L = 1 k\Omega$

Parameter	Description	Test Conditions	EL2005				EL2005C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
SR	Slew Rate	$V_{IN} = \pm 10V, V_{OUT} = \pm 5V$	1000	1500		III	1000	1500		III	V/μs
BW	Bandwidth	$V_{IN} = 1 V_{rms}$		140		V		140		V	MHz
ϕ_{NL}	Phase Non-Linearity	BW = 1 MHz to 20 MHz		2		V		2		V	Degree
t_r	Rise Time	$\Delta V_{IN} = 0.5V$		2.5		V		2.5		V	ns
t_P	Propagation Delay	$\Delta V_{IN} = 0.5V$		1.0		V		1.0		V	ns
HD	Harmonic Distortion	f > 1 kHz		<0.1		V		<0.1		V	%
A_V	Voltage Gain	$R_S = 100\Omega, V_{IN} = 1 V_{rms}$, f = 1 kHz	0.97	0.99	1.0	I	0.96	0.99	1.0	II	V/V
R_O	Output Impedance	$V_{IN} = 1 V_{rms}$, f = 1 kHz		4	8	I		4	9	II	Ω

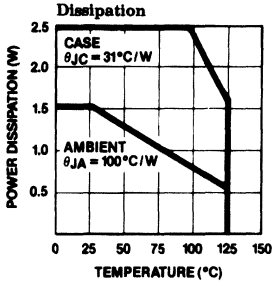
Note 1: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperatures will exceed the value at $T_J = 25°C$. When supply voltages are ±15V, no-load operating junction temperatures may rise 40°C to 60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs Temperature graph for expected values.

Note 2: Measured in still air seven minutes after application of power.

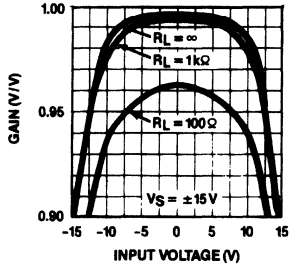
Note 3: Input bias current is guaranteed over the input range of $-10V \leq V_{IN} \leq +10V$.

Typical Performance Curves

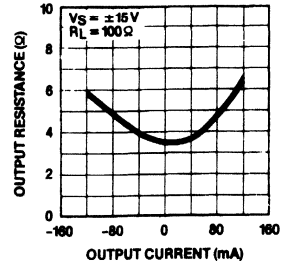
Maximum Power Dissipation



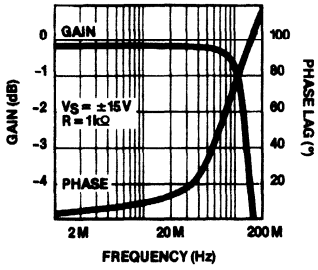
Gain vs Input Voltage



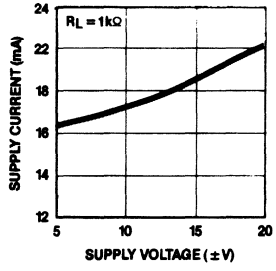
Output Resistance vs Output Current



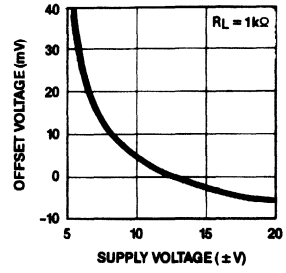
Frequency Response



Supply Current vs Supply Voltage

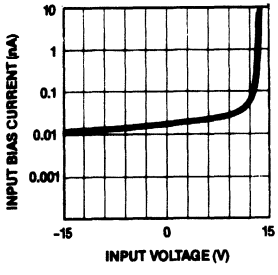


Offset Voltage vs Supply Voltage

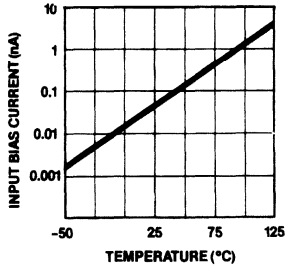


2005-3

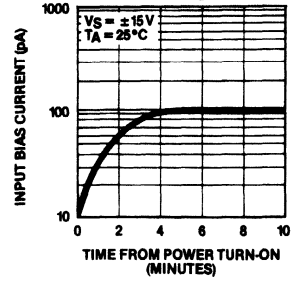
Input Bias Current vs Input Voltage



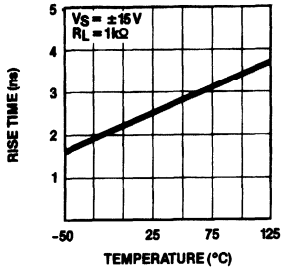
Input Bias Current vs Temperature



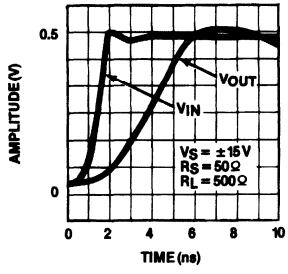
Input Bias Current During Warm-up



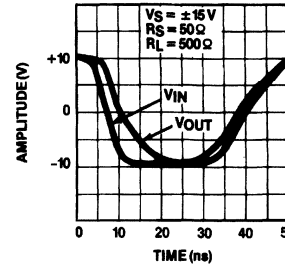
Rise Time vs Temperature



Small Signal Pulse Response



Large Signal Pulse Response

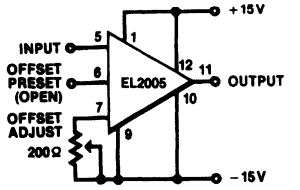


2005-4

EL2005/EL2005C
High Accuracy Fast Buffer

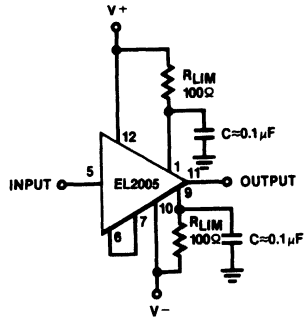
Typical Applications

Offset Zero Adjust



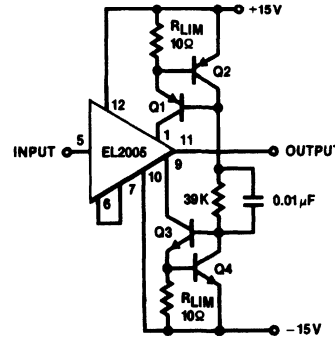
2005-5

Using Resistor Current Limiting



2005-6

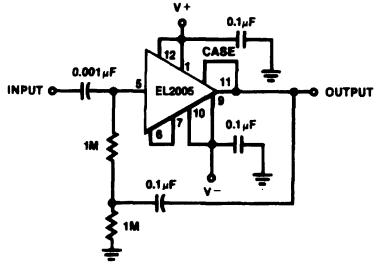
Current Limiting Using Current Sources



2005-7

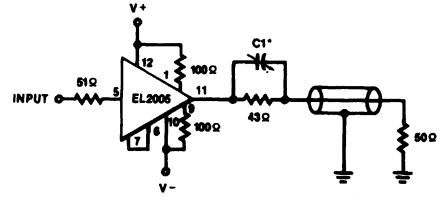
Q1 = Q2 = 2N2905
Q3 = Q4 = 2N2219

High Input Impedance AC Coupled Amplifier



2005-8

Coaxial Cable Driver

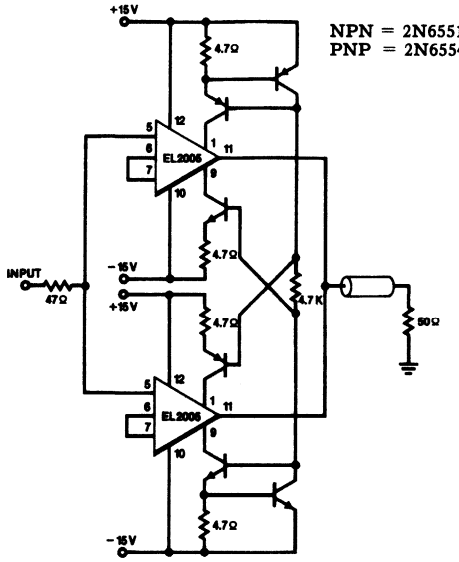


*Select C1 for optimum pulse response

2005-9

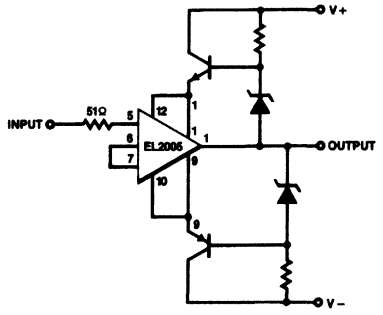
Typical Applications — Contd.

50Ω Cable Driver with Short Circuit Protection



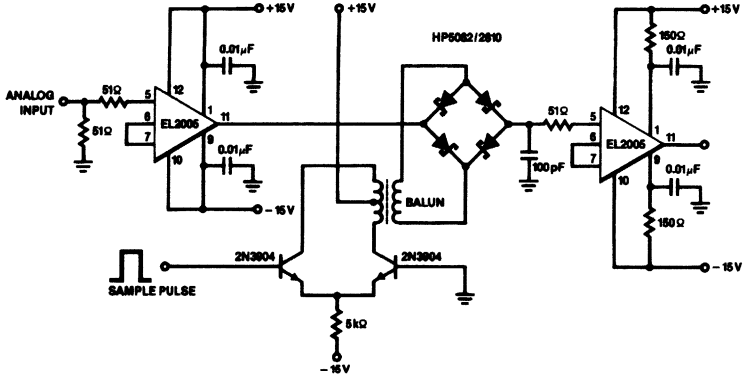
2005-10

Bootstrapped Supplies for High Voltage Applications



2005-11

High-Speed Sample and Hold



2005-12

EL2005/EL2005C
High Accuracy Fast Buffer

Applications Information

Recommended Layout Precautions

RF/video printed circuit board layout rules should be followed when using the EL2005 since it will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively, the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment

The EL2005's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. The pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 200Ω between the offset adjust pin and V− as illustrated on page 9-22.

Operation from Single or Asymmetrical Power Supplies

This device type may be readily used in applications where symmetrical supplies are unavailable or not desirable. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V+ - V-)}{2} = 0.005\,(V+ - V-)$$

where: A_V = No load voltage gain, typically 0.99
$V+$ = Positive supply voltage
$V-$ = Negative supply voltage

For example, with $V+ = +5V$ and $V- = -12V$, ΔV_O would be −35 mV. This may be adjusted to zero as described above.

Short Circuit Protection

In order to optimize transient response and output swing, output current limit has been omitted from the EL2005. Short circuit protection may be added by inserting appropriate value resistors between $V+$ and V_C+ pins and $V-$ and V_C- pins as shown on page 9-22.

Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V+}{I_{SC}} = \frac{V-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for EL2005

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C+ and V_C- pins with capacitors to ground will retain full output swing for transient pulses. An alternate active current limit technique that retains full DC output swing is also shown on page 9-22. In this circuit, the current sources are saturated during normal operation thus applying full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

$$R_{LIM} \cong \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\text{ mA}} = 10\Omega$$

Capacitive Loading

The EL2005 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from (C × dV/dt) should be limited below absolute maximum peak current ratings for the devices.

Thus:

$$\frac{\Delta V_{IN}}{\Delta t} \times C_L \leq I_{OUT} \leq \pm 250\text{ mA}$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below the total package power rating:

$$P_Dpkg \geq P_{DC} + P_{AC}$$

$$P_Dpkg \geq (V+ - V-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

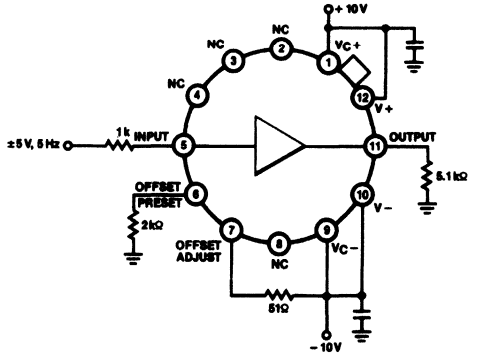
where: $V_{P\text{-}P}$ = Peak-to-peak output voltage swing
f = Frequency
C_L = Load Capacitance

Applications Information — Contd.

Operation within an Op Amp Loop

The EL2005 may be used as a current booster or isolation buffer within a closed loop with op amps such as the ELH0032 and HA2500 and HA2600 series. An isolation resistor of 47Ω should be used between the op amp output and the input of EL2005. The wide bandwidth and high slew rates of the EL2005 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

Burn-In Circuit



2005-13

Hardware

In order to utilize the full drive capabilities of the EL2005, it should be mounted with a heatsink, particularly for extended temperature operation. The case is isolated from the circuit and may be connected to system chassis.

IMPORTANT!

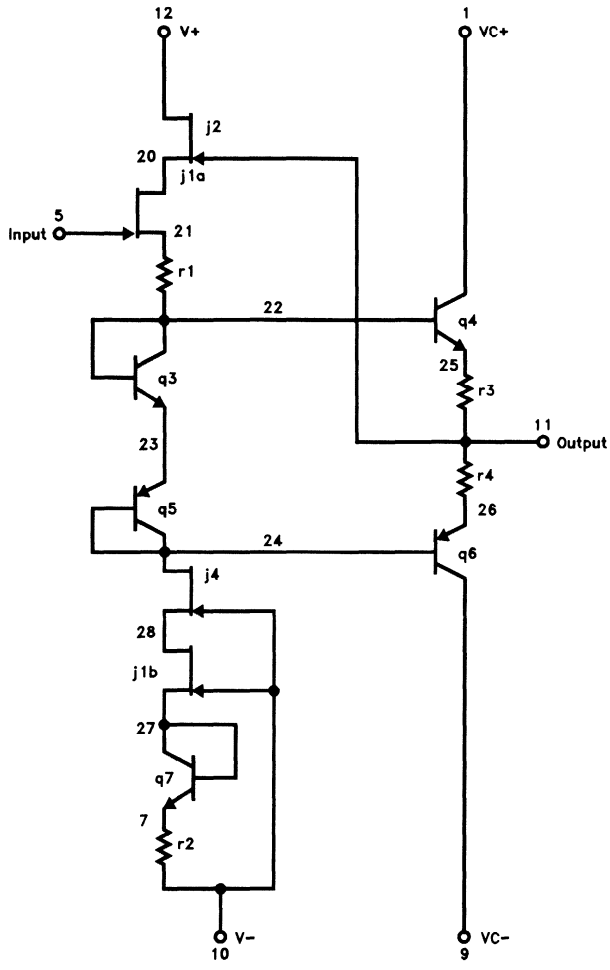
Power supply bypassing is necessary to prevent oscillation with the EL2005 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within ¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1 μF in parallel; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances.

EL2005/EL2005C
High Accuracy Fast Buffer

EL2005 Macromodel

```
* Connections:      input
*                   |      V+
*                   |      |       +Vc+
*                   |      |       |      V-
*                   |      |       |      |      Vc-
*                   |      |       |      |      |      output
*                   |      |       |      |      |      |
.subckt M2005       5      12      1      10     9      11
* Models
.model qn npn (is=5e-14 bf=150 vaf=100 rc=1 rb=5 re=1 ikf=200mA
+cje=5pF cjc=5pF mje=.42 mjc=.23 tf=.3nS tr=200nS br=5 vtf=0)
.model qp pnp (is=5e-14 bf=150 vaf=100 rc=.2 rb=3 re=1 ikf=100mA
+cje=5.7pF cjc=4pF tf=.3nS mje=.32 mjc=.43 tr=170nS br=5 vtf=0)
.model qfa njf (vto=-8V beta=2.344e-3 cgd=10pF cgs=7pF lambda=671e-6)
.model qfb njf(vto=-4V beta=1.06e-3 cgd=3pF cgs=3pF)
* Resistors
r1 21 22 30
r2 7 10 30
r3 25 11 3
r4 11 26 3
* Transistors
j1a 20 5 21 qfb
j1b 28 10 27 qfb
j2 12 11 20 qfa
j4 24 10 28 qfa
q3 22 22 23 qn
q4 1 22 25 qn
q5 24 24 23 qp
q6 9 24 26 qp
q7 27 27 7 qn
.ends
```

EL2005 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2006/EL2006A
High Gain Fast FET Input Op Amp

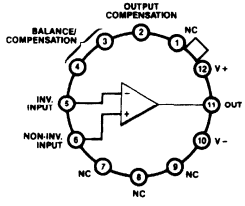
Features

- 90 dB open loop gain
- 450 V/μs slew rate
- 40 MHz bandwidth
- No thermal tail
- 3 mV max input offset voltage
- Offset nulls with single pot
- No compensation required for gains above 50
- Peak output current to 200 mA
- Pin compatible with LH0032
- 80 dB common mode rejection

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
EL2006CG	−25°C to +85°C	TO-8	MDP0002
EL2006G	−55°C to +125°C	TO-8	MDP0002
EL2006G/883B	−55°C to +125°C	TO-8	MDP0002
EL2006ACG	−25°C to +85°C	TO-8	MDP0002
EL2006AG	−55°C to +125°C	TO-8	MDP0002
EL2006AG/883G	−55°C to +125°C	TO-8	MDP0002

Connection Diagrams



Top View

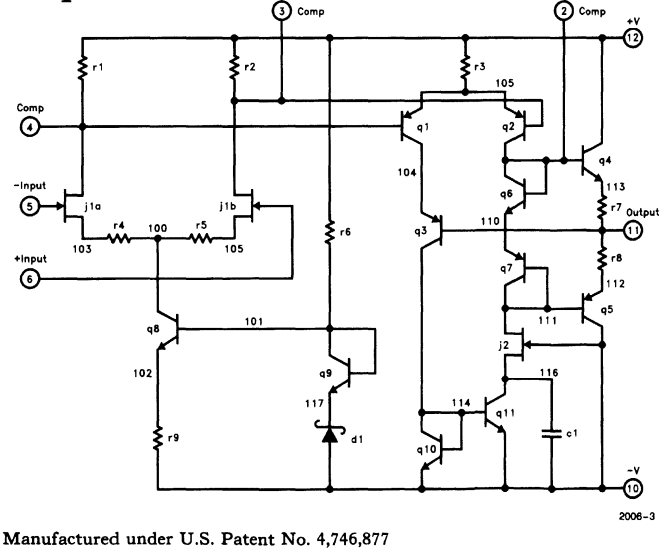
General Description

The EL2006/EL2006A are high slew rate, wide bandwidth, high input impedance, high gain and fully differential input operational amplifiers. They exhibit excellent open loop gain characteristics making them suitable for a broad range of high speed signal processing applications. These patented devices have open loop gains in excess of 86 dB making the EL2006/EL2006A ideal choices for current mode video bandwidth digital to analog converters of 10 bits or higher resolution. The EL2006's FET input structure, high slew rate, and high output drive capability allow use in applications such as buffers for flash converter inputs. In general, the EL2006/EL2006A allow the user to take relatively high closed loop gains without compromising gain accuracy or bandwidth.

The EL2006/EL2006A are pin compatible with the popular industry standard ELH0032/ELH0032A offering comparable bandwidth and slew rate, while offering significant improvements in open loop gain, common mode rejection and power supply rejection.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883 Class B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Simplified Schematic



Manufactured under U.S. Patent No. 4,746,877

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	±15V		EL2006, EL2006A	−55°C to +125°C
	Differential Input Voltage	30V		EL2006C, EL2006AC	−25°C to +85°C
I_{OUT}	Peak Output Current (Note 1)	±200 mA	T_J	Operating Junction Temperature	175°C
P_D	Power Dissipation		T_{ST}	Storage Temperature	−65°C to +150°C
	T_A = 25°C 1.5W, derate 100°C/W to +125°C			Lead Temperature	
	T_C = 25°C 2.2W, derate 70°C/W to +125°C			(Soldering 10 seconds)	300°C

[redacted]

DC Electrical Characteristics V_S = ±15V, $T_{MIN} < T_A < T_{MAX}$

Parameter	Description	Test Conditions	EL2006				EL2006C				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	T_J = 25°C			5	I			5	I	mV
					10	I			10	III	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			15		V		15		V	µV/°C
I_B	Bias Current	T_J = 25°C			100	I			500	I	pA
				1	10	I		1	10	III	nA
I_{OS}	Offset Current	T_J = 25°C			25	I			50	I	pA
				0.2	2.5	I		0.2	2.5	III	nA
V_{CM}	Common Mode Range		±10			I	±10			II	V
CMRR	Common Mode Rejection Ratio	ΔV_{IN} = ±10V	70	80		I	70	80		II	dB
PSRR	Power Supply Rejection Ratio	±5V ≤ V_S ≤ ±15V	70	88		I	70	88		II	dB
A_{VOL}	Large Signal Voltage Gain	R_L = 1 kΩ, V_{OUT} = ±10V, T_J = 25°C	74	90		I	74	90		I	dB
		R_L = 1 kΩ, V_{OUT} = ±10V	80			I	74			III	dB
V_O	Output Voltage Swing	R_L = 1 kΩ	±12			I	±12			II	V
I_{OUT}	Output Current	V_{OUT} = ±10V, T_J = 25°C, (Note 1)	±100			I	±100			I	mA
I_{CC}	Supply Current			20	23	I		20	23	II	mA

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EL2006/EL2006A
High Gain Fast FET Input Op Amp

DC Electrical Characteristics — Contd.

$V_S = \pm 15V$, $T_{MIN} < T_A < T_{MAX}$ (Note: These tests are in addition to those listed above.)

Parameter	Description	Test Conditions	EL2006A				EL2006AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage	$T_J = 25°C$			3	I			3	I	mV
$\Delta V_{OS}/\Delta T$	Offset Voltage Drift			15	25	I		15	25	I	µV/°C
A_{VOL}	Large Signal Voltage Gain	$T_J = 25°C$, $R_L = 1 k\Omega$, $V_{OUT} = \pm 10V$	74	90		I	74	90		II	dB
		$R_L = 1 k\Omega$, $V_{OUT} = \pm 10V$	74			I	74			III	dB

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1 k\Omega$, $T_J = 25°C$ (See AC Test Circuits)

Parameter	Description	Test Conditions	EL2006, EL2006A				EL2006C, EL2006AC				Units
			Min	Typ	Max	Test Level	Min	Typ	Max	Test Level	
t_r	Rise Time	$A_V = 10V$, $V_{OUT} = 1 V_{P-P}$		18		V		18		V	ns
		$A_V = 1V$, $V_{OUT} = 1 V_{P-P}$		12	15	I		12	15	I	ns
SR	Slew Rate (Note 2)	$A_V = 1V$, $V_{OUT} = 20 V_{P-P}$	350	450		I	350	450		I	V/µs
t_s	Settling Time to 1.0%	$A_V = -1V$, $V_{OUT} = 10 V_{P-P}$		90		V		90		V	ns
t_s	Settling Time to 0.1%	$A_V = -1V$, $V_{OUT} = 10 V_{P-P}$		160		V		160		V	ns
t_s	Settling Time to 0.01%	$A_V = -1V$, $V_{OUT} = 10 V_{P-P}$		250		V		250		V	ns
GBW	Gain Bandwidth Product	$A_V \geq 20V$		500		V		500		V	MHz
	Pull Power Bandwidth (Note 3)	$V_{OUT} = \pm 10V$	5.5	7		I	5.5	7		I	MHz
	Unity Gain Bandwidth	$C_A = 8$ pF, $C_B = 100$ pF		40		V		40		V	MHz
e_N	Noise Voltage	1 kHz to 1 MHz		20		V		20		V	nV/$\sqrt{Hz}$
t_D	Small Signal Delay	$A_V = 1V$		13	15	I		13	15	I	ns
C_{IN}	Input Capacitance			2		V		2		V	pF

Note 1: $T_J = 25°C$, duty cycle < 1%, pulse width < 10 µs.
Note 2: Slew rate is measured at the 25% and 75% points.
Note 3: The Full Power bandwidth is guaranteed by testing slew rate.

EL2006 Recommended Compensation

(See Figure 1)

A_{VOL}	C_A	C_B	R_{S+}	R_{S-}	R_F
+1	5–8 pF	100 pF	2k	Open Circuit	100
−1 to +5	5 pF	68 pF	0	< 1k	1k
±10	5 pF	10 pF	< 1k	1k	> 10k
> ±20	3 pF	10 pF	< 1k	1k	> 20k

Note: Use a small capacitor of about 1 pF in parallel with R_F to compensate for stray input capacitance.

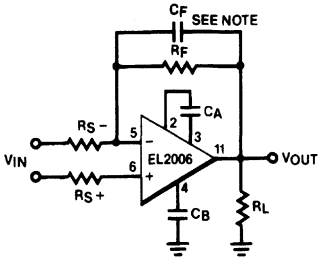
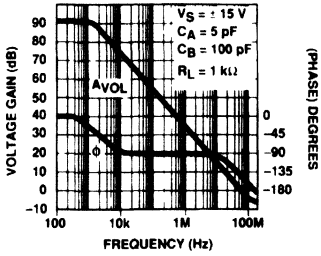


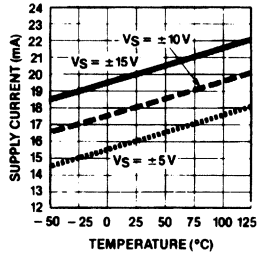
Figure 1

Typical Performance Curves

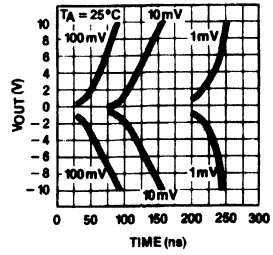
Bode Plot, Unity Gain Compensation



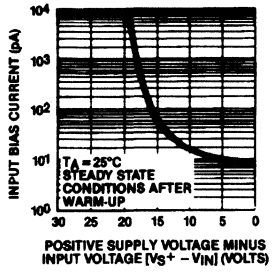
Supply Current vs Temperature



Inverting Gain of −1 Settling Time



Input Bias Currents as a Function of Input Voltage



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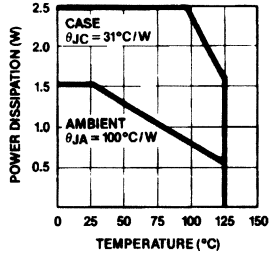
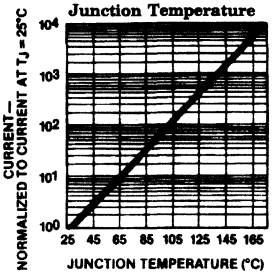
TO-8 Maximum Power Dissipation



Normalized Input Bias and Offset Current vs Junction Temperature



Applications Information

General

The EL2006 was designed to overcome the gain and stability limitations of prior high speed FET input operational amplifiers like the LH0032. Open loop gain is typically 90 dB allowing gain setting to 12-bit accuracy. This new design also eliminates "thermal tail", which is the tendency for the gain to diminish at very low frequencies to DC due to thermal feedback. The EL2006 is also easier to stabilize than earlier designs, thanks to an Elantec proprietary internal compensation technique which eliminates the "second stage bump." The EL2006 open loop gain

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EL2006/EL2006A
High Gain Fast FET Input Op Amp

Applications Information — Contd.

characteristic is well behaved well beyond the unity gain frequency so that spurious ringing or oscillation in the 100 MHZ–200 MHz region is avoided. Finally, we have provided temperature compensation so that gain and stability are relatively constant over temperature.

These improvements are provided in a configuration which is plug compatible with LH0032 and similar products so that designers can easily upgrade their system performance without extensive re-design. In most cases, the EL2006 can be used to replace LH0032 with no change in external compensation.

Video DAC Amplifiers

A typical application for the EL2006 is to provide gain for video signals. In the example shown, the EL2006 provides a gain of 2 with settling time around 35 ns to 10 mV.

Power Supply Decoupling

The EL2006/EL2006A, like most high-speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as possible with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power, thus raising the FET junction temperature 40°C–60°C above the free-air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at the time will be indicative of normal operating currents. An additional rise will occur as power is delivered to a load due to additional internal power dissipation.

Power Dissipation

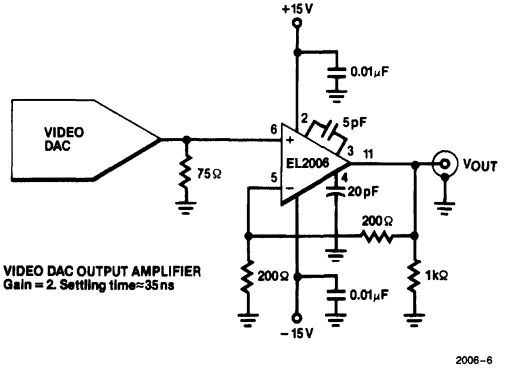
There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value, depending on FET geometry and doping levels. This effect will be noted as the input voltage of the EL2006 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the EL2006/EL2006A is typically 2 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a 1 pF.



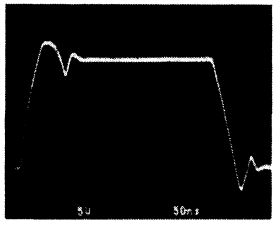
VIDEO DAC OUTPUT AMPLIFIER
Gain = 2. Settling time≈35ns

Applications Information — Contd.

Heatsinking

While the EL2006/EL2006A are specified for operation without any explicit heatsink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

Voltage Follower (A_V = +1)
Large Signal Pulse Response



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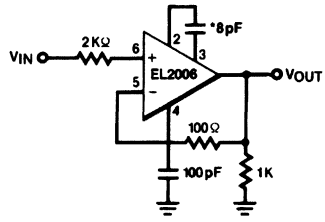
V_S = ±15V, V_{IN} = +10V to −10V and −10V to +10V

Large Signal Pulse Response Test Circuit



*INCLUDES STRAYS

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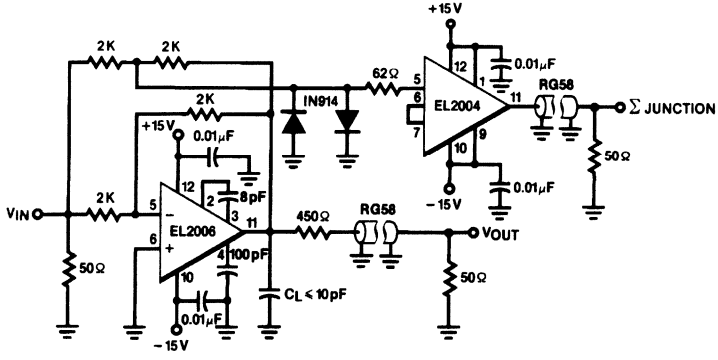
EL2006 Settling Time Test Circuit



R_L = 2KΩ // 2KΩ // 500Ω ≈ 333Ω

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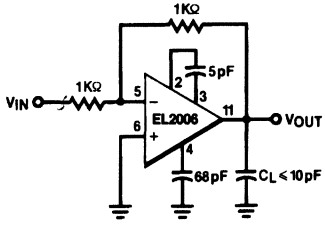
Inverting Unity Gain



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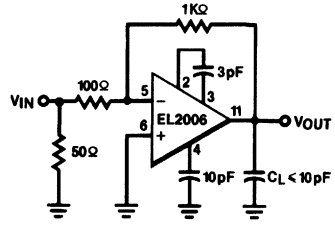
Inverting Gain of 10



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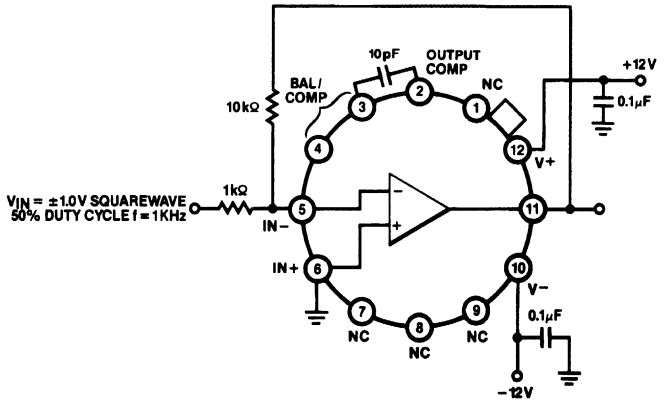
Burn-In Circuit

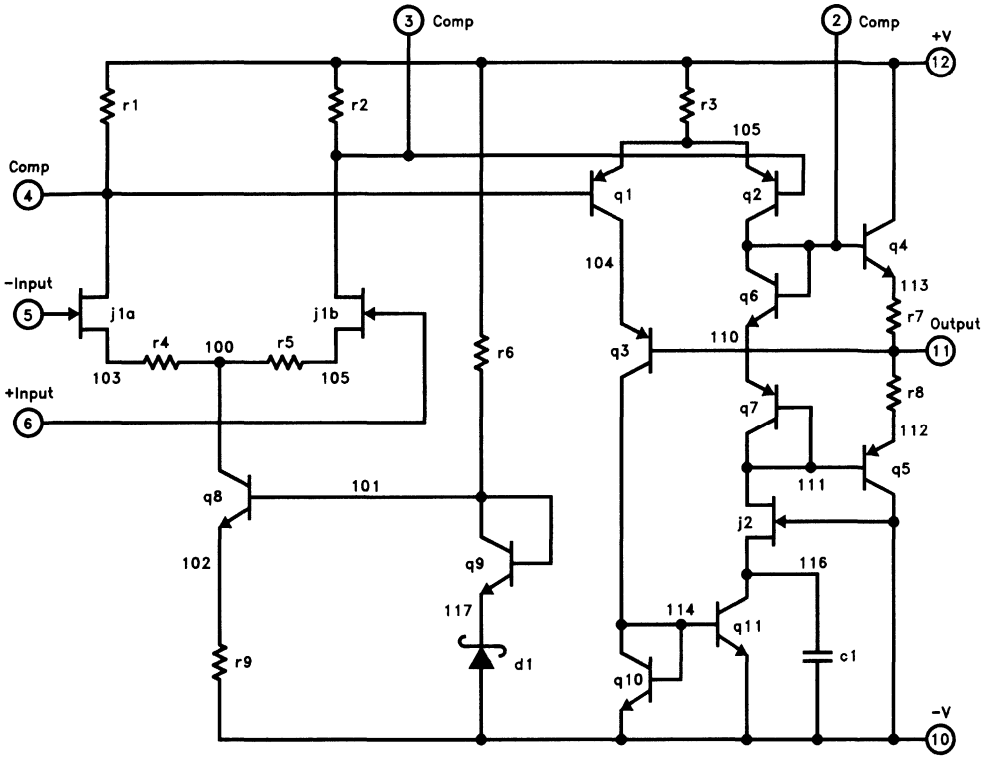


Pin Numbers are for TO-8 package. LCC uses the same schematic.

EL2006 Macromodel

```
* Connections:      +input
*                   |     -input
*                   |     |     +Vsupply
*                   |     |     |     -Vsupply
*                   |     |     |     |     Comp 3
*                   |     |     |     |     |     Comp 4
*                   |     |     |     |     |     |     Comp 2
*                   |     |     |     |     |     |     |     Output
*                   |     |     |     |     |     |     |     |
.subckt M2006       6     5     12    10    3     4     2     11
* Models
.model qfa njf (vto = -2.5V beta = 1.11e-3 cgd = 2pF cgs = 5pF m = 0.3744)
.model qp pnp (is = 5E-14 bf = 150 vaf = 100 ikf = 100mA tf = .53nS vtf = 0 ise = 1 nA,
+cjc = 4pF cje = 5.7pF tr = 170nS rb = 3 br = 5 mje = .32 mjc = .43 xtb = 2.1 ne = 4
+isc = 1nA nc = 4 itf = .4 vtf = 4 xtf = 6)
.model qn npn (is = 5e-14 bf = 150 vaf = 800 ikf = 200mA tf = .54nS vtf = 0
+cjc = 4pF cje = 5pF rb = 3 br = 5 mje = .42 mjc = .23 tr = 200nS xtb = 2.1
+ise = 4nA ne = 4 isc = 4nA nc = 4 itf = .4 vtf = 4 xtf = 2)
.model qfb njf (vto = -2.8V beta = 4e-3 cgd = 7pF cgs = 8pF lambda = 4e-3)
.model zener d (bv = 2.49V ibv = 1mA)
* Resistors and Capacitors
r1 12 4 700
r2 12 3 700
r3 12 105 160
r4 103 100 10
r5 108 100 10
r6 12 101 22K
r7 113 11 10
r8 11 112 10
r9 102 10 407
cs2 10 116 100pF
* Transistors and Diodes
j1a 4 5 103 qfa
j1b 3 6 108 qfa
j2 111 10 116 qfb
q1 104 4 105 qp
q2 2 3 105 qp
q3 114 11 104 qp
q4 12 2 113 qn
q5 10 111 112 qp
q6 2 2 110 qn
q7 111 111 110 qp
q8 100 101 102 qn
d1 10 117 zener
q9 101 101 117 qn
q10 114 114 10 qn
q11 116 114 10 qn
.ends
```

EL2006 Macromodel — Contd.



ELH0002H/883/7801301XX
Current Amplifier

Features

- 400 mA pulsed output current
- DC to 30 MHz bandwidth
- 200 V/μs slew rate
- Low harmonic distortion
- High input impedance—400 kΩ
- Low output impedance—6Ω
- High power efficiency
- Operation from ±5V to ±20V
- Output voltage swing approaches supply voltage
- MIL-STD-883 devices manufactured in U.S.A.

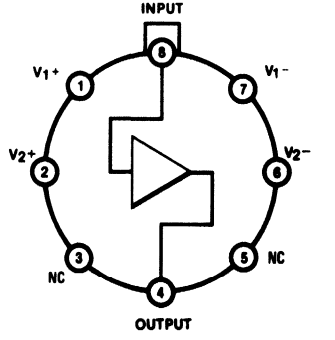
Applications

- Line driver
- 30 MHz buffer
- High-speed D/A conversion
- Instrumentation buffer
- Precision current source

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
ELH0002H/883B	−55°C to +125°C	TO-5	MDP0001

7801301XX is the DESC version of this device.



Top View

Case is electrically isolated.

General Description

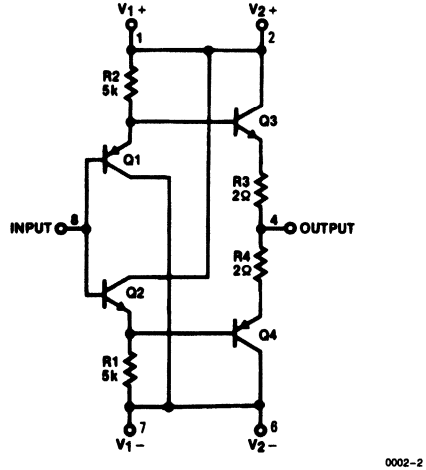
The ELH0002 is a general purpose hybrid current amplifier buffer that is built on a single substrate.

The ELH0002 is ideal for current buffering operational amplifiers without changing the characteristics of the Op. Amp. The ELH0002 uses a completely symmetrical circuit to provide a low output impedance when both sourcing and sinking current. This means the output will drive coaxial cables and other capacitive loads with equivalent rise and fall times.

The ELH0002 is specified for operation over the −55°C to +125°C military temperature range.

Elantec facilities comply with MIL-I-45208A and are MIL-STD-1772 certified. Elantec's Military devices comply with MIL-STD-883B Revision C and are manufactured in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance Policy and procedures request brochure QRA-1.

Equivalent Schematic



ELH0002H/883/7801301XX
Current Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±22V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	±22V		ELH0002	−55°C to +125°C
P_D	Power Dissipation Ambient	600 mW		Steady State Current	±100 mA
T_{ST}	Storage Temperature	−65°C to +150°C		Pulsed Output Current (50 ms On/1 second Off)	±400 mA

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±12V, $T_{MIN} \le T_A \le T_{MAX}$

Parameter	Description	Test Conditions	ELH0002				Units
			Min	Typ	Max	Test Level	
V_{OS}	Output Offset Voltage	R_S = 300Ω, R_L = 1 kΩ		±10	±30	I	mV
A_V	Voltage Gain	R_S = 10 kΩ, R_L = 1 kΩ, V_{IN} = ±10 V_{dc}	0.95	0.97		I	V/V
R_{IN}	Input Impedance	R_S = 200 kΩ, V_{IN} = ±1 V_{dc}, R_L = 1 kΩ	180	400		I	kΩ
R_{OUT}	Output Impedance	R_S = 50Ω, V_{IN} = ±1 V_{dc}, R_S = 10 kΩ		6Ω			
V_O	Output Voltage Swing	V_{IN} = ±12V, R_L = 1 KΩ	±10	±11		I	V
		V_S = ±15V, V_{IN} = ±12V, R_S = 50Ω, R_L = 100Ω, T_A = 25°C	±10			I	V
I_B	Input Current	R_S = 10 kΩ, R_L = 1 kΩ		±6	±10	I	μA
I_S+	Positive Supply Current	R_S = 10 kΩ, R_L = 1 kΩ		6	10	I	mA
I_S-	Negative Supply Current	R_S = 10 kΩ, R_L = 1 kΩ		−6	−10	I	mA

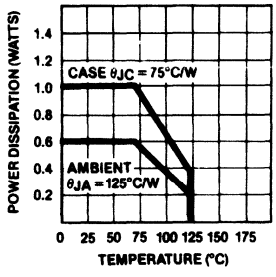
Note 1: Elantec's ELH0002H/200 is tested to the ELH0002 DC limits at −25°C, +25°C and +125°C, and the AC limits at 25°C. In addition, the parts are also tested to the DC limits for V_{OS}, A_{VOL} with R_L = 1 kΩ, I_{IN}, I_S+ and I_S- at 200°C.

AC Electrical Characteristics $V_S = \pm 12V$, $T_A = 25°C$

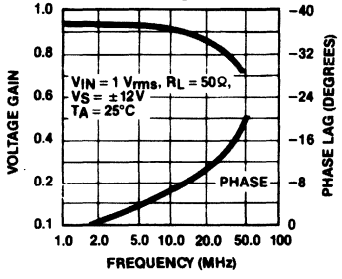
Parameter	Description	Test Conditions	ELH0002				Units
			Min	Typ	Max	Test Level	
A_V	Voltage Gain	$R_S = 10\ k\Omega$, $R_L = 1\ k\Omega$ $V_{IN} = 3\ V_{P-P}$, f = 1 kHz	0.95	0.97		I	V/V
A_I	Current Gain	$V_{IN} = 1\ V_{RMS}$, f = 1 kHz		40			A/mA
R_{IN}	Input Impedance	$R_S = 200\ k\Omega$, $V_{IN} = 1\ V_{RMS}$, $R_L = 1\ k\Omega$, f = 1 kHz	180	400		I	kΩ
R_{OUT}	Output Impedance	$R_L = 50\Omega$, $V_{IN} = 1\ V_{RMS}$, $R_S = 10\ k\Omega$, f = 1 kHz		6	10	I	Ω
HD	Harmonic Distortion	$V_{IN} = 5\ V_{RMS}$, f = 1 kHz		0.1		V	%
t_r	Rise Time	$R_L = 50\Omega$, $\Delta V_{IN} = 100$ mV		7	12	III	ns

Typical Performance Curves

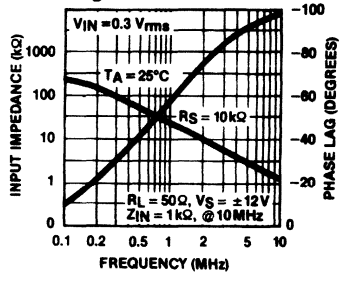
Maximum Power Dissipation



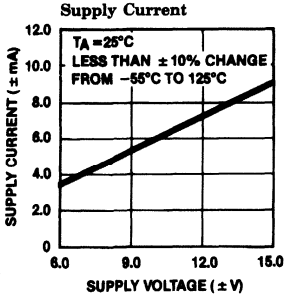
Frequency Response



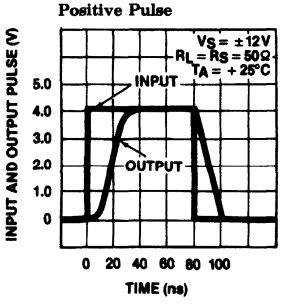
Input Impedance (Magnitude & Phase)



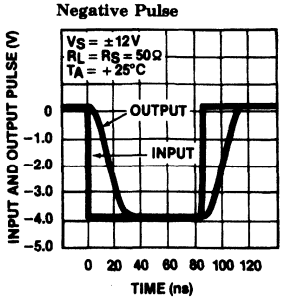
Supply Current



Positive Pulse



Negative Pulse

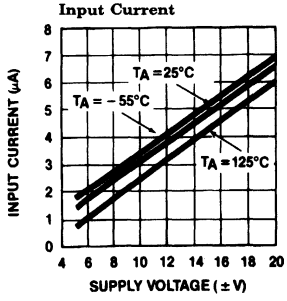


0002-3

9

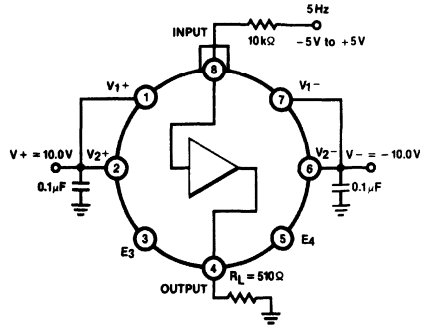
ELH0002H/883/7801301XX
Current Amplifier

Typical Performance Curves — Contd.



0002-4

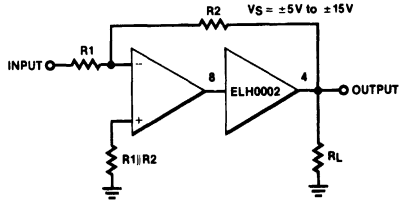
Burn-In Circuit



0002-5

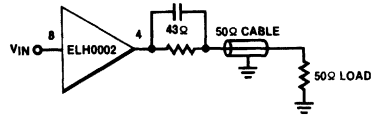
Typical Applications

High Current Operational Amplifier



0002-6

Line Driver



0002-7

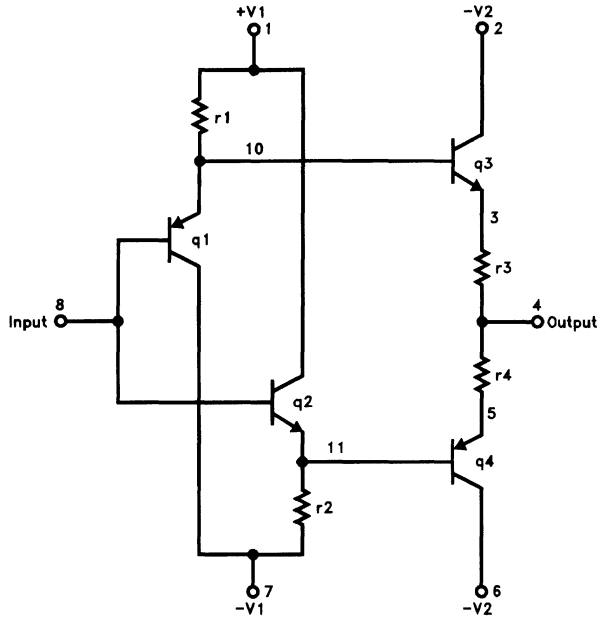
Select capacitor to adjust time response of pulse.

ELH0002 Macromodel

```
* Connections:  input
*               |     V1+
*               |     |     V2+
*               |     |     |     V1-
*               |     |     |     |     V2-
*               |     |     |     |     |     output
*               |     |     |     |     |     |
.subckt M0002   8     1     2     7     6     4
* Models
.model qp pnp (is=10e-14 bf=300 vaf=60 ikf=200mA var=6V br=9
+rb=30 cje=40pF cjc=15pF tf=1nS xtb=2.0)
.model qn npn (is=10e-14 bf=200 vaf=200 ikf=200mA var=12V br=8
+rb=30 cje=27pF cjc=10pF tf=1nS xtb=2.0)
* Resistors
r1 1 10 5K
r2 11 7 5K
r3 3 4 2.0
r4 5 4 2.0
* Transistors
q1 7 8 10 qp
q4 6 11 5 qp
q2 1 8 11 qn
q3 2 10 3 qn
.ends
```

ELH0002H/883/7801301XX
Current Amplifier

ELH0002 Macromodel — Contd.



ELH0021K/883/8508801YX
1 Amp Power Operational Amplifier

Features

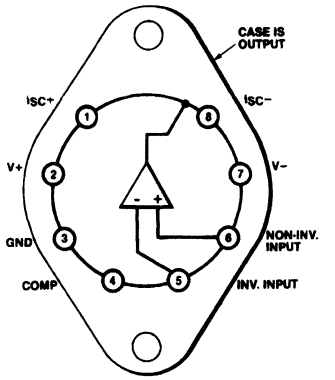
- High output current—1.2A
- Large output voltage swing—±12V
- Low standby power—100 mW
- Wide full power bandwidth—20 kHz
- Low input bias current
- Low input offset voltage
- High open-loop gain >100 dB
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
ELH0021K/883B	−55°C to +125°C	TO-3	MDP0003

8508801YX is the SMD version of this device.

Connection Diagram



Top View

General Description

The ELH0021 is a general purpose operational amplifier capable of delivering large output currents not usually associated with conventional IC op amps; the ELH0021 will provide output currents in excess of 1A at voltage levels of ±12V. In addition, both the inputs and outputs are protected against overload. The device is compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

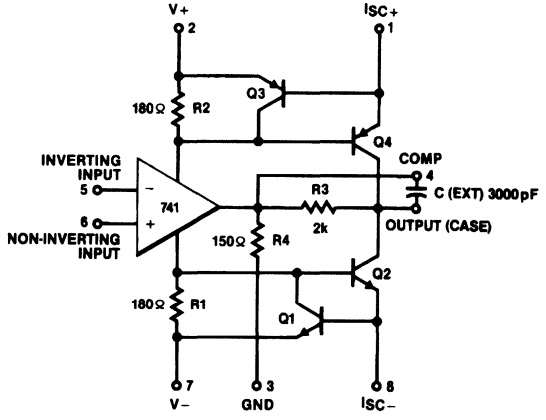
The excellent input characteristics and high output capability of the ELH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

Other applications include torque drivers for inertial guidance systems, diddle yoke drivers for alphanumeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

The ELH0021 is supplied in an 8-pin TO-3 package rated at 20W with suitable heatsink. The ELH0021 is guaranteed over the temperature range of −55°C to +125°C.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Equivalent Schematic



ELH0021K/883/8508801YX
1 Amp Power Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage (Note 1)	±15V		ELH0021	−55°C to +125°C
P_D	Power Dissipation (See Curves)		T_{ST}	Storage Temperature	−65°C to +150°C
	Differential Input Voltage	±30V		Lead Temperature	
	Peak Output Current (Note 2)	2A		(Soldering, 10 seconds)	300°C
	Output Short				
	Circuit Duration (Note 3)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$, C_C = 3000 pF

Parameter	Description	Test Conditions	ELH0021				Units
			Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$, T_C = 25°C (Note 4)		1	3	I	mV
		$R_S \le 100\Omega$ (Note 4)			5	I	mV
$\Delta V_{OS}/\Delta T$	Voltage Drift with Temperature	$R_S \le 100\Omega$		3	25	IV	µV/°C
	Offset Voltage Drift with Time	T_A = 25°C		5		V	$\mu V\sqrt{wk}$
$\Delta V_{OS}/\Delta P$	Offset Voltage Change with Output Power			5	15	I	µV/W
I_{OS}	Input Offset Current	T_C = 25°C (Note 4)		30	100	I	nA
		(Note 4)			300	I	nA
	Offset Current Drift with Temperature			0.1	1	IV	nA/°C
	Offset Current Drift with Time	T_A = 25°C		2		V	$nA/\sqrt{wk}$
I_B	Input Bias Current	T_C = 25°C (Note 4)		100	300	I	nA
		(Note 4)			1	I	µA
R_{IN}	Input Resistance	T_C = 25°C	0.3	1		I	MΩ
CMRR	Common-Mode Rejection Ratio	$R_S \le 100\Omega$, V_{CM} = ±10V	70	90		I	dB
V_{INCM}	Input Voltage Range		±12			IV	V

DC Electrical Characteristics $V_S = \pm 15V, T_{MIN} \leq T_A \leq T_{MAX}, C_C = 3000\ pF$ — Contd.

Parameter	Description	Test Conditions	ELH0021				Units
			Min	Typ	Max	Test Level	
PSRR	Power Supply Rejection Ratio	$R_S \leq 100\Omega$, $V_S = \pm 5V$ to $\pm 15V$	80	96		I	dB
A_{VOL}	Voltage Gain (Note 5)	$V_O = \pm 10V, R_L = 1\ k\Omega, T_C = 25°C$	100	200		I	V/mV
		$V_O = \pm 10V, R_L = 100\Omega$	25			I	V/mV
V_O	Output Voltage Swing	$R_L = 100\Omega$	± 13.5	14		I	V
		$R_L = 10\Omega, T_C = 25°C$	± 11	± 12		I	V
I_{SC}	Output Short Circuit Current	$T_C = 25°C, R_{SC} = 0.5\Omega$	0.8	1.2	1.6	I	A
I_S	Supply Current	$V_{OUT} = 0V$		2.5	3.5	I	mA
P_C	Power Consumption	$V_{OUT} = 0V$		75	105	I	mW

Note 1: Rating applies for supply voltages above $\pm 15V$. For supplies less than $\pm 15V$, rating is equal to supply voltage.
Note 2: Rating applies for ELH0021K with $R_{SC} = 0\Omega$.
Note 3: Rating applies as long as package power rating is not exceeded.
Note 4: Specifications apply for $\pm 5V \leq V_S \leq \pm 18V$.
Note 5: The ELH0021, like all Class B amplifiers, has a "dead band" when V_{OUT} is near 0V. Typical values for the "dead band" are in the 50 μV to 200 μV range. Open-loop gain is measured at V_{OUT} from $\pm 0.5\ V_{DC}$ TO $\pm 10.0\ V_{DC}$ which is out of the range of the "dead band".

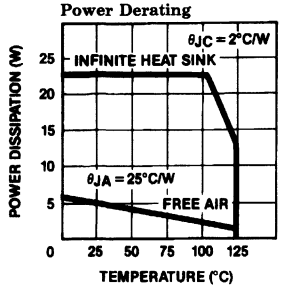
AC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V, C_C = 3000\ pF$

Parameter	Description	Test Conditions	ELH0021				Units
			Min	Typ	Max	Test Level	
SR	Slew Rate	$A_V = 1, R_L = 100\Omega$	1.5	3		I	V/μs
BW	Bandwidth	$R_L = 100\Omega$		20		V	kHz
t_r, t_f	Small Signal Rise or Fall Time			0.3	1	I	μs
	Small Signal Overshoot			5	20	I	%
t_S	Settling Time (0.1%)	$\Delta V_{IN} = 10V, A_V = 1$		4		V	μs
	Overload Recovery Time			3		V	μs
HD	Harmonic Distortion	$f = 1\ kHz, P_O = 0.5W$		0.2		V	%
e_n	Input Noise Voltage	$R_S = 50\Omega$, BW = 10 Hz to 10 kHz		5		V	μVrms
i_n	Input Noise Current	BW = 10 Hz to 10 kHz		0.05		V	nA_{rms}
C_{IN}	Input Capacitance			3		V	pF

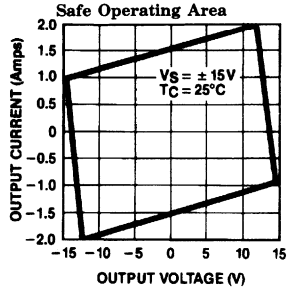
ELH0021K/883/8508801YX
1 Amp Power Operational Amplifier

Typical Performance Curves

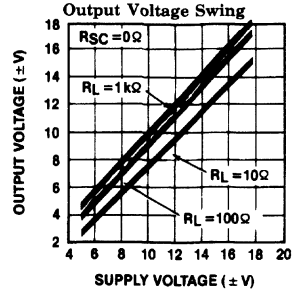
Power Derating



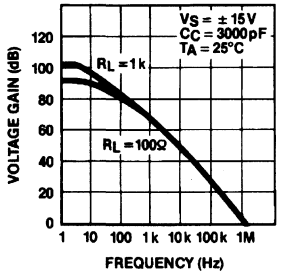
Safe Operating Area



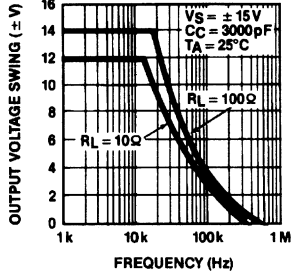
Output Voltage Swing



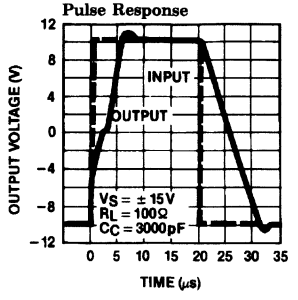
Open-Loop
Frequency Response



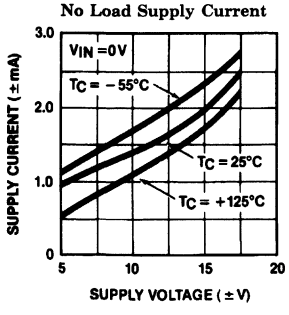
Large Signal
Frequency Response



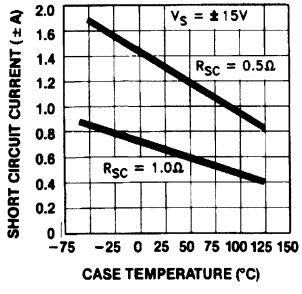
Voltage Follower
Pulse Response



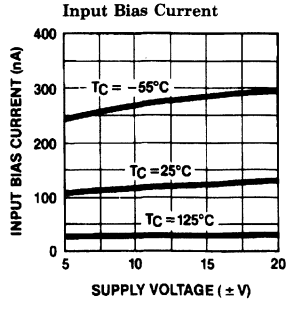
No Load Supply Current



Short Circuit Current
vs Temperature



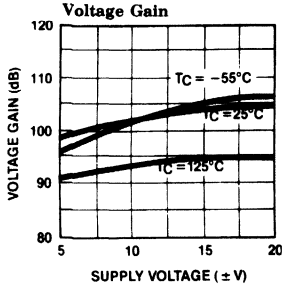
Input Bias Current



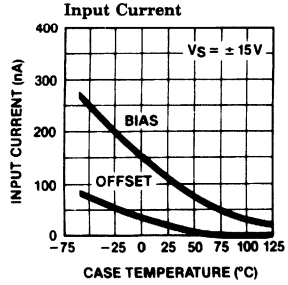
0021-3

Typical Performance Curves — Contd.

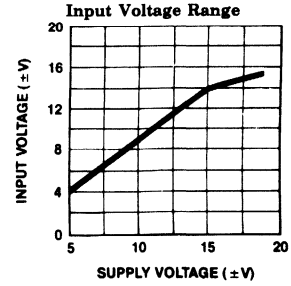
Voltage Gain



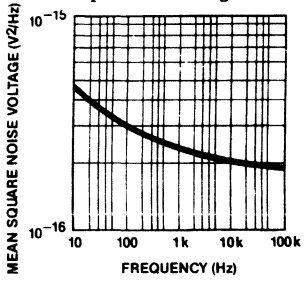
Input Current



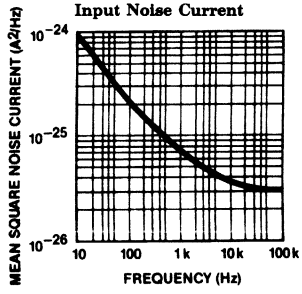
Input Voltage Range



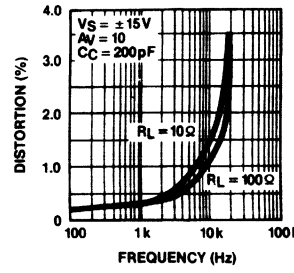
Input Noise Voltage



Input Noise Current



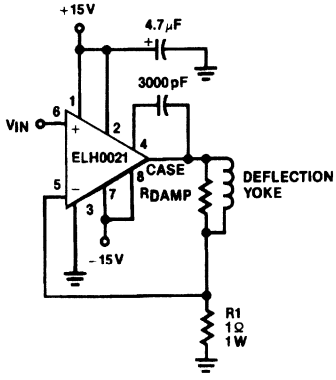
Distortion vs Frequency



0021-4

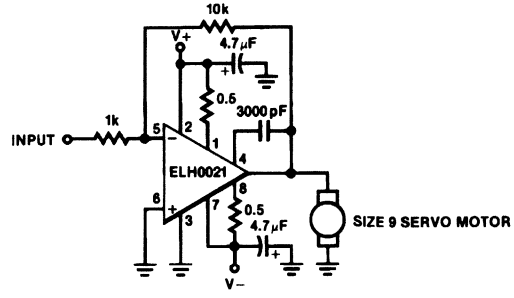
Typical Applications

CRT Deflection Yoke Driver



0021-5

DC Servo Amplifier

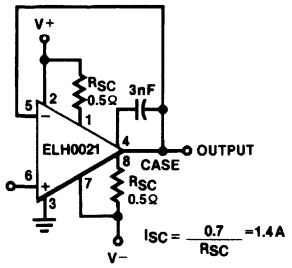


0021-6

ELH0021K/883/8508801YX
1 Amp Power Operational Amplifier

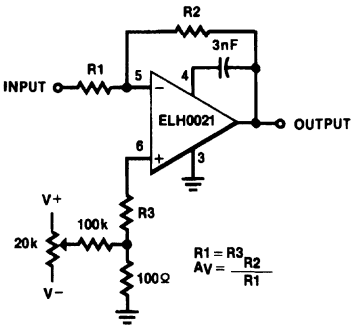
Typical Applications — Contd.

Unity Gain with Short Circuit Limiting



0021-7

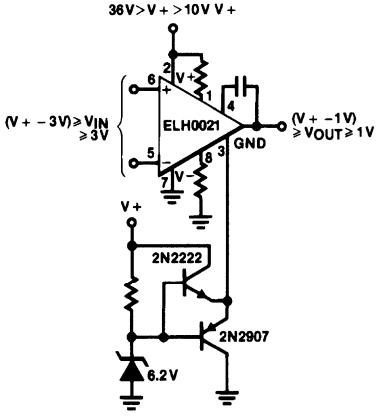
Offset Voltage Null Circuit



0021-8

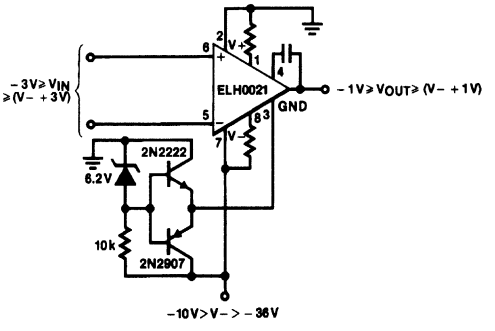
Operation from Single Supplies

Positive



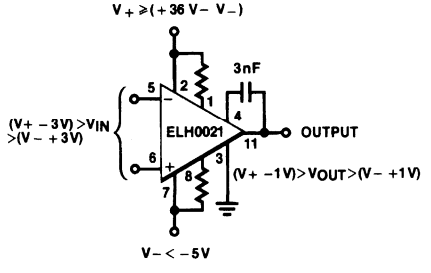
0021-9

Negative

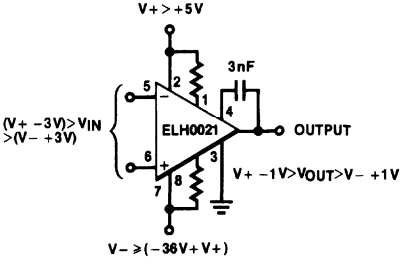


0021-10

Operation from Non-Symmetrical Supplies

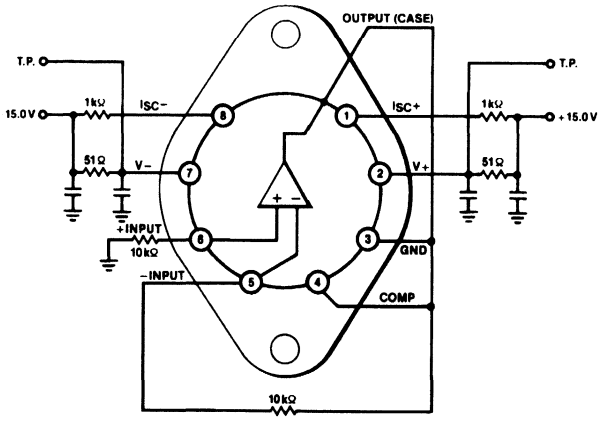


0021-11



0021-12

Burn-In Circuit



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELH0032G/883/8001301ZX
Fast Operational Amplifier

Features

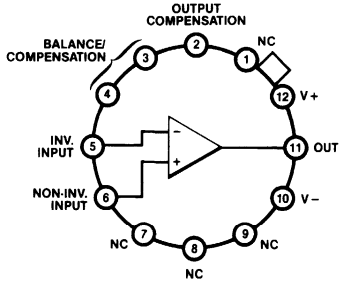
- 500 V/μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- 5 mV max. input offset voltage
- FET input
- Offset nulls with single pot
- No compensation required for gains above 50
- Peak output current to 100 mA
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Pkg. Outline #
ELH0032G/883B	−55°C to +125°C	TO-8 MDP0002

8001301ZX is the SMD version of this device.

Connection Diagram



Top View

Case is electrically isolated.

Manufactured under U.S. Patent No. 4,746,877

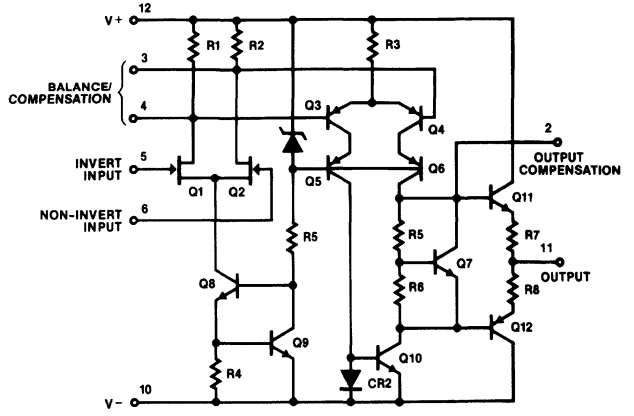
General Description

The ELH0032 is a high slew rate, high input impedance differential operational amplifier suitable for diverse application in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability make the ELH0032 particularly suitable for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The ELH0032's wide bandwidth, high input impedance and high output drive capability make it an ideal choice for applications such as summing amplifiers in high-speed D to A's, buffers in data acquisition systems, and sample and hold circuits. Additional applications include high-speed integrators and video amplifiers. The ELH0032 is guaranteed over the temperature range −55°C to +125°C.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Simplified Schematic



Absolute Maximum Ratings

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range:	
V_{IN}	Input Voltage	±15 V_S		ELH0032	−55°C to +125°C
	Differential Input Voltage	±30V or ±2 V_S	T_J	Operating Junction Temperature	175°C
P_D	Power Dissipation (Note 1)		T_{ST}	Storage Temperature	−65°C to +150°C
	T_A = 25°C 1.5W, derate 100°C/W to +125°C			Lead Temperature	
	T_C = 25°C 2.2W, derate 70°C/W to +125°C			(Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V, $T_{MIN} \le T_A \le T_{MAX}$, V_{IN} = 0V

Parameter	Description	Test Conditions	ELH0032				Units
			Min	Typ	Max	Test Level	
V_{OS}	Input Offset Voltage	T_J = 25°C (Note 2)		2	5	I	mV
					10	I	mV
$\Delta V_{OS}/\Delta T$	Average Offset Voltage Drift			25	150	I	µV/°C
I_{OS}	Input Offset Current	T_J = 25°C (Note 2)			25	I	pA
		T_A = 25°C (Note 3)			250	IV	pA
		T_J = Max			25	I	nA
I_B	Input Bias Current	T_J = 25°C (Note 2)			100	I	pA
		T_A = 25°C (Note 3)			1	IV	nA
		$T_J = T_{MAX}$			50	I	nA
V_{INCM}	Input Voltage Range		±10	±12		I	V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±10V	50	60		I	dB
A_{VOL}	Open-Loop Voltage Gain	V_O = ±10V, R_L = 1 kΩ, T_J = 25°C	48	60		I	dB
		V_O = ±10V, R_L = 1 kΩ	45			I	dB
		V_O = ±10V, f = 1 kHz, R_L = 1 kΩ, T_J = 25°C	60	70		I	dB
		V_O = ±10V, f = 1 kHz, R_L = 1 kΩ	57			I	dB

ELH0032G/883/8001301ZX
Fast Operational Amplifier

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$, $V_{IN} = 0V$ — Contd.

Parameter	Description	Test Conditions	ELH0032				Units
			Min	Typ	Max	Test Level	
V_O	Output Voltage Swing	$R_L = 1\ k\Omega$	±10	±13.5		I	V
I_S	Power Supply Current	$T_J = 25°C$, $I_O = 0$ mA		21	23	I	mA
		$T_A = 25°C$, $I_O = 0$ mA (Note 3)		18	20	IV	mA
PSRR	Power Supply Rejection Ratio	$\pm 5V \le V_S \le 15V$	50	60		I	dB
		$+5V \le V_S(+) \le +20V$, $V_S(-) = -15V$	50			I	dB
		$-5V \ge V_S(-) \ge -20V$, $V_S(+) = +15V$	50			I	dB

AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1\ k\Omega$, $T_J = 25°C$

Parameter	Description	Test Conditions	Min	Typ	Max	Test Level	Units
SR	Slew Rate	$A_V = +1$, $\Delta V_{IN} = 20V$	350	500		I	V/μs
t_S	Settling Time to 1% of Final Value	$A_V = -1$, $\Delta V_{IN} = 20V$		100	500	IV	ns
t_S	Settling Time to 0.1% of Final Value	$A_V = -1$, $\Delta V_{IN} = 20V$		300		V	ns
t_R	Small Signal Rise Time	$A_V = +1$, $\Delta V_{IN} = 1V$		8	20	I	ns
t_D	Small Signal Delay Time	$A_V = +1$, $\Delta V_{IN} = 1V$		10	25	I	ns

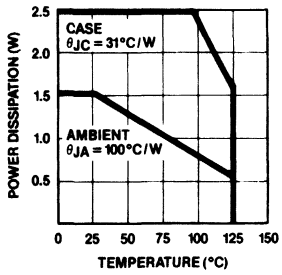
Note 1: In order to limit maximum junction temperature to +175°C, it may be necessary to operate with $V_S < \pm 15V$ when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation.

Note 2: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25°C$. When supply voltage are ±15V, no-load operating junction temperature may rise 40°C–60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs temperature graph for expected values.

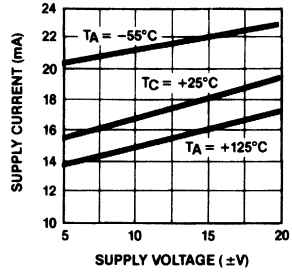
Note 3: Measured in still air 7 minutes after application of power.

Typical Performance Curves

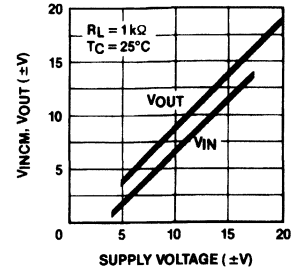
Maximum Power Dissipation



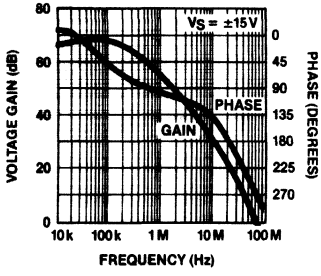
Supply Current vs Supply Voltage



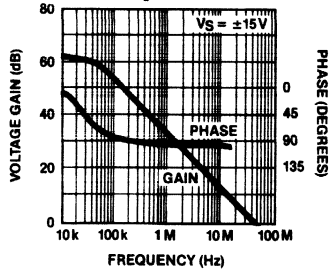
Input Voltage Range and Output Voltage vs Supply Voltage



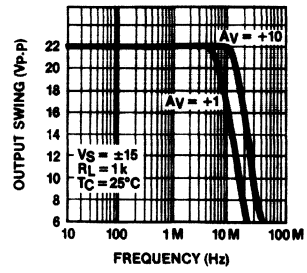
Bode Plot (Uncompensated)



Bode Plot (Unity Gain Compensation)



Large Signal Frequency Response



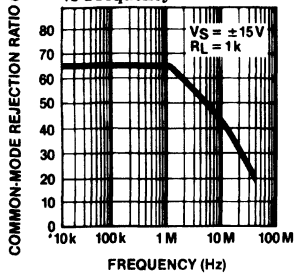
0032-3

9

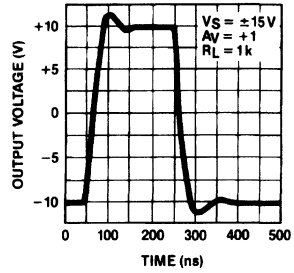
ELH0032G/883/8001301ZX
Fast Operational Amplifier

Typical Performance Curves — Contd.

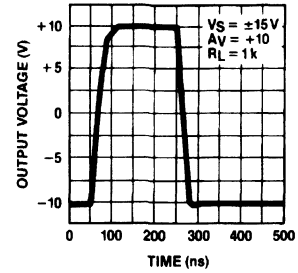
Common Mode Rejection Ratio vs Frequency



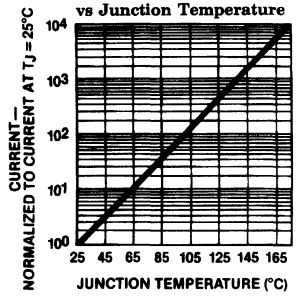
Large Signal Pulse Response



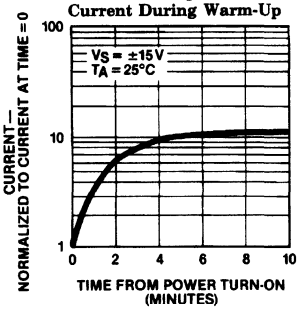
Large Signal Pulse Response



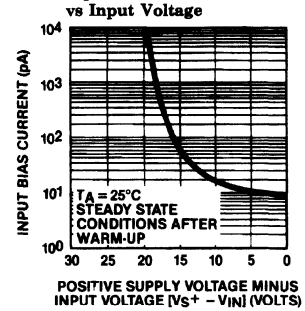
Normalized Input Bias and Offset Current vs Junction Temperature



Normalized Input Bias Current During Warm-Up

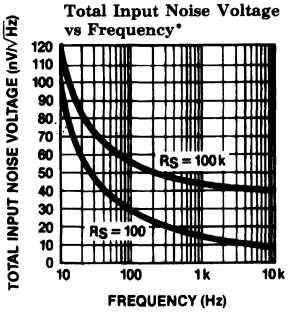


Input Bias Current vs Input Voltage



0032-4

Total Input Noise Voltage vs Frequency*

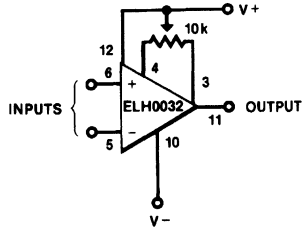


0032-5

*Noise voltage includes contribution from source resistance.

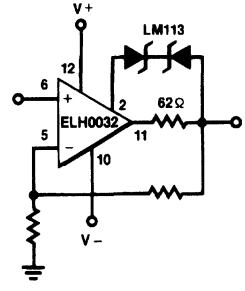
Auxiliary Circuits

Offset Null



0032-6

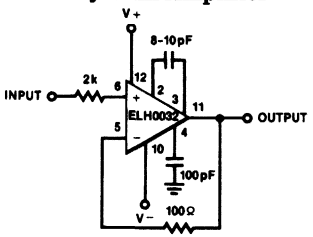
Output Short Circuit Protection



0032-7

Typical Applications

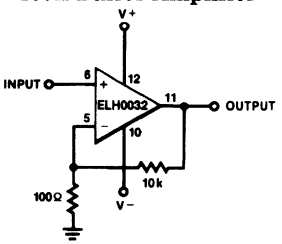
Unity Gain Amplifier



0032-8

TYP $BW_{3\ dB}$ = 45 MHz

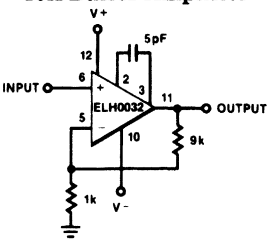
100X Buffer Amplifier



0032-9

TYP $BW_{3\ dB}$ = 10 MHz

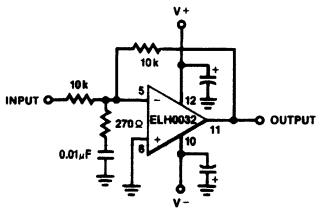
10X Buffer Amplifier



0032-10

TYP $BW_{3\ dB}$ = 5 MHz

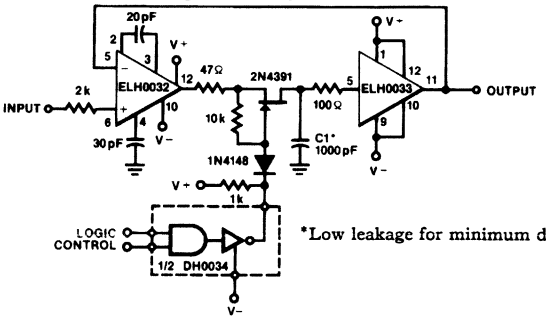
Non-Compensated Unity Gain Inverter



0032-11

TYP $BW_{3\ dB}$ = 70 MHz

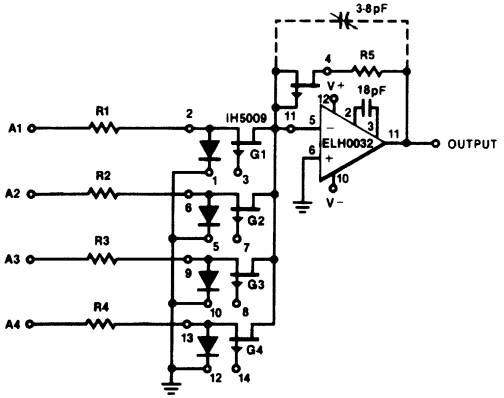
High-Speed Sample and Hold



*Low leakage for minimum drift

0032-12

High-Speed Current Mode MUX



0032-13

ELH0032G/883/8001301ZX
Fast Operational Amplifier

Applications Information

Power Supply Decoupling

The ELH0032, like most high-speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as possible with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

Input Current

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power, thus raising the FET junction temperature 40°C–60°C above the free-air ambient temperature when supplies are ±15V. The device temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at the time will be indicative of normal operating currents. An additional rise will occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalance-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value, depending on FET geometry and doping levels. This effect will be noted as the input voltage of the ELH0032 is taken below ground potential when the supplies are ±15V. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

Input Capacitance

The input capacitance to the ELH0032 is typically 5 pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

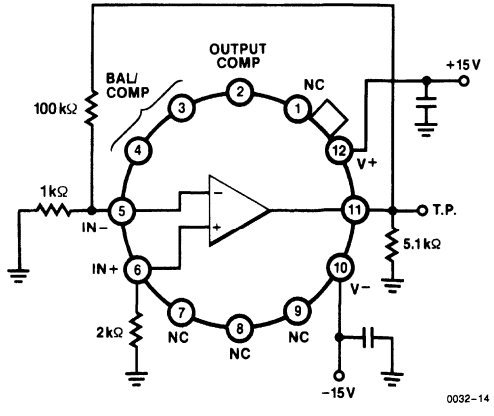
In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a 1 pF.

Heatsinking

While the ELH0032 is specified for operation without any explicit heatsink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

Burn-In Circuit

(Functional Diagram)

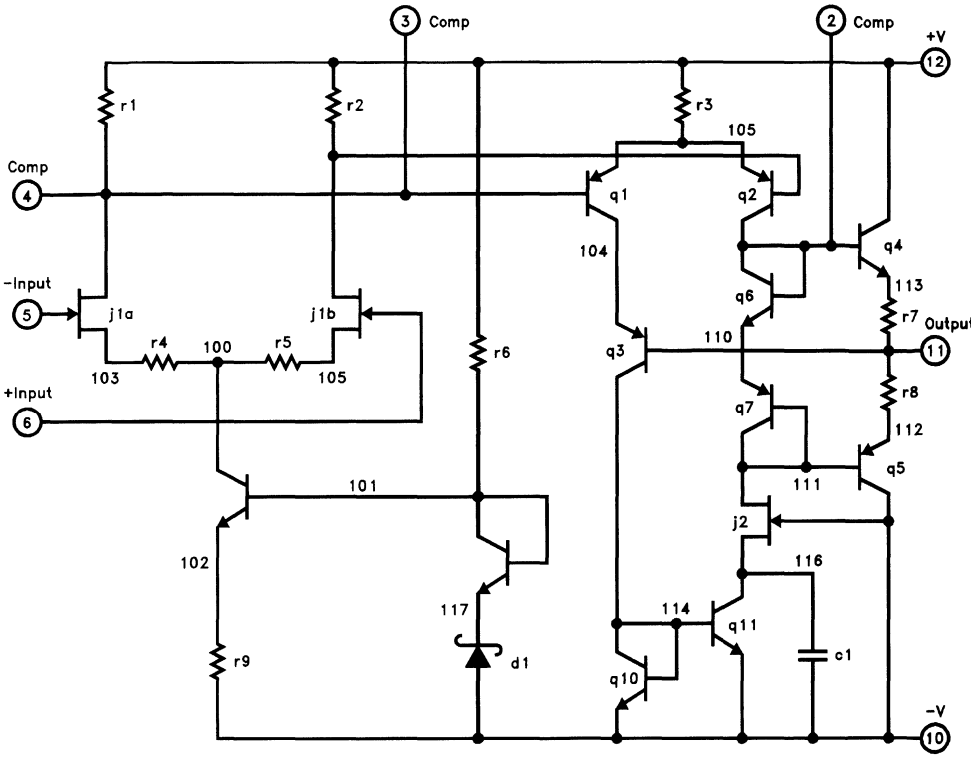


ELH0032 Macromodel

```
* Connections:      +input
*                   |    -input
*                   |    |    +Vsupply
*                   |    |    |    -Vsupply
*                   |    |    |    |    Comp 3
*                   |    |    |    |    |    Comp 4
*                   |    |    |    |    |    |    Comp 2
*                   |    |    |    |    |    |    |    Output
*                   |    |    |    |    |    |    |    |
*                   |    |    |    |    |    |    |    |
.subckt M0032       6    5    12   10   3    4    2    11
* Models
.model qfa njf (vto = -2.5V beta = 1.11e-3 cgd = 2pF cgs = 5pF m = 0.3744)
.model qp pnp (is = 5e-14 bf = 150 vaf = 100 ikf = 100mA tf = .53nS vtf = 0 ise = 1nA
+ cjc = 4pF cje = 5.7pF tr = 170nS rb = 3 br = 5 mje = .32 mjc = .43 xtb = 2.1 ne = 4
+ isc = 1nA nc = 4 itf = .4 vtf = 4 xtf = 6)
.model qn npn (is = 5e-14 bf = 150 vaf = 800 ikf = 200mA tf = .53nS vtf = 0
+ cjc = 4pF cje = 5pF rb = 3 br = 5 mje = .42 MJC = .23 tr = 200nS xtb = 2.1
+ ise = 4nA ne = 4 isc = 4nA nc = 4 itf = .4 vtf = 4 xtf = 2)
.model qfb njf (vto = -2.8V beta = 4e-3 cgd = 7pF cgs = 8pF lambda = 4e-3)
.model zener d (bv = 2.49V ibv = 1mA)
* Resistors and Capacitors
r1 12 4 700
r2 12 3 700
r3 12 105 160
r4 103 100 10
r5 108 100 10
r6 12 101 22K
r7 113 11 10
r8 11 112 10
r9 102 10 407
cs2 10 116 100pF
* Transistors and Diodes
j1a 4 5 103 qfa
j1b 3 6 108 qfa
j2 111 10 116 qfb
q1 104 4 105 qp
q2 2 3 105 qp
q3 114 11 104 qp
q4 12 2 113 qn
q5 10 111 112 qp
q6 2 2 110 qn
q7 111 111 110 qp
q8 100 101 102 qn
d1 10 117 zener
q9 101 101 117 qn
q10 114 114 10 qn
q11 116 114 10 qn
.ends
```

ELH0032G/883/8001301ZX
Fast Operational Amplifier

ELH0032 Macromodel — Contd.



ELH0033G/883/8001401ZX
Fast Buffer Amplifier

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Features
- Slew rate—1500 V/μs
- Output drive—100 mA
- Rise and fall times—2.9 ns
- Input resistance—$10^{11}\Omega$
- Power bandwidth—100 MHz
- MIL-STD-883 devices 100% manufactured in U.S.A.

Advantages
- Excellent phase linearity
- Driver cables and other capacitive loads
- Wide supply range, single or split

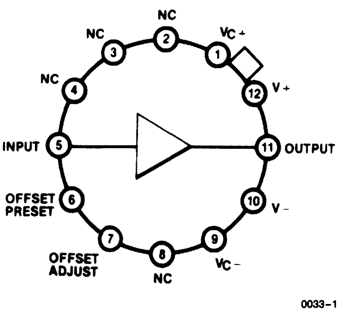
Ordering Information

Part No.	Temp. Range	Package	Outline#
ELH0033G/883B	−55°C to +125°C	TO-8	MDP0002

8001401ZX is the SMD version of this device.

Connection Diagram

12-Pin TO-8



Top View

Note: Case is electrically isolated.

General Description

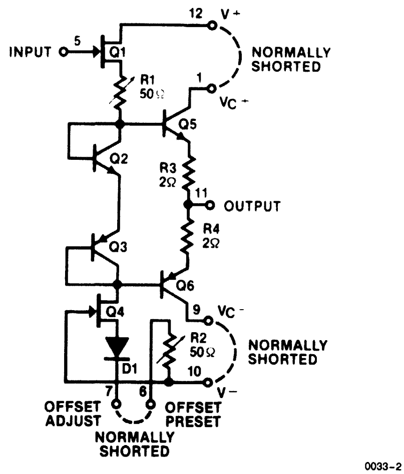
The ELH0033 is a high-speed, FET input voltage follower buffer designed to provide high output currents from DC to over 100 MHz. The ELH0033 slews at 1500 V/μs and will drive 100Ω loads. Phase linearity is excellent to 20 MHz, allowing the buffer to be included in op amp loops.

The ELH0033 is intended to fulfill a wide range of buffer applications such as high-speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high-speed A to D's and comparators.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The ELH0033 is specified for operation from −55°C to +125°C.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Equivalent Schematic



ELH0033G/883/8001401ZX

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July 1992 Rev H

ELH0033G/883/8001401ZX
Fast Buffer Amplifier

Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	40V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage	40V		ELH0033	−55°C to +125°C
P_D	Power Dissipation (See Curves)	1.5W	T_J	Operating Junction Temperature	175°C
I_{OC}	Continuous Output Current	±100 mA	T_{ST}	Storage Temperature	−65°C to +150°C
I_{OP}	Peak Output Current	±250 mA		Lead Temperature (Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics $V_S = \pm 15V, V_{IN} = 0V, T_{MIN} \le T_A \le T_{MAX}$

Parameter	Description	Test Conditions	ELH0033 Min	ELH0033 Typ	ELH0033 Max	ELH0033 Test Level	Units
V_{OS}	Output Offset Voltage	$R_S \le 100\ k\Omega$, T_J = 25°C (Note 1)		5	10	I	mV
		$R_S \le 100\ k\Omega$			15	I	mV
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Offset Voltage	$R_S = 100\Omega$		50		V	µV/°C
I_B	Input Bias Current	T_J = 25°C (Note 1)			250	I	pA
		T_A = 25°C (Note 2)			2.5	IV	nA
		$T_J = T_A = T_{MAX}$			10	I	nA
A_V	Voltage Gain	$R_S = 100\Omega$, R_L = 1 kΩ, $V_{IN} = \pm 10V$	0.97	0.98	1.00	I	V/V
R_{IN}	Input Impedance	R_L = 1 kΩ	10^{10}	10^{11}		IV	Ω
		T_J = 25°C (Note 1), R_L = 1 kΩ	10^{10}	10^{11}		I	Ω
R_O	Output Impedance	R_L = 1 kΩ, $V_{IN} = \pm 1V$		6	10	I	Ω
V_O	Output Voltage Swing	$V_{IN} = \pm 14V$, R_L = 1 kΩ	±12			I	V
		$V_{IN} = \pm 10.5V$, $R_L = 100\Omega$, T_A = 25°C	±9			I	V
I_S	Supply Current		14.5	20	22	I	mA
	Power Consumption			600	660	I	mW

Note 1: Specification is at 25°C junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at T_J = 25°C. When supply voltages are ±15V, no-load operating junction temperature may rise 40°C–60°C above ambient and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

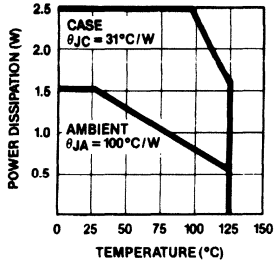
Note 2: Measured in still air 7 minutes after application of power.

AC Electrical Characteristics $T_C = 25°C$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1\,k\Omega$

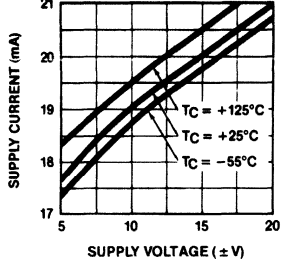
Parameter	Description	Test Conditions	ELH0033				Units
			Min	Typ	Max	Test Level	
SR	Slew Rate	$V_{IN} = \pm 10V$	1000	1500		III	V/μs
BW	Bandwidth	$V_{IN} = 1\,V_{rms}$		100		V	MHz
	Phase Non-Linearity	BW = 1 MHz to 20 MHz		2		V	°
t_r	Rise Time	$\Delta V_{IN} = 0.5V$		2.9		V	ns
t_p	Propagation Delay	$\Delta V_{IN} = 0.5V$		1.2		V	ns
HD	Harmonic Distortion	f > 1 kHz		<0.1		V	%
A_V	Voltage Gain	$R_S = 100\Omega$, $V_{IN} = 1\,V_{rms}$, f = 1 kHz	0.97	0.98	1.00	I	V/V
R_O	Output Impedance	$V_{IN} = 1\,V_{rms}$, f = 1 kHz		6	10	I	Ω

Typical Performance Curves

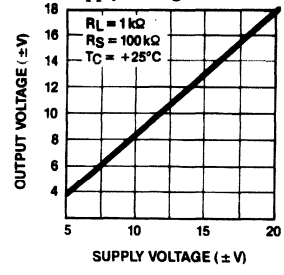
Maximum Power Dissipation



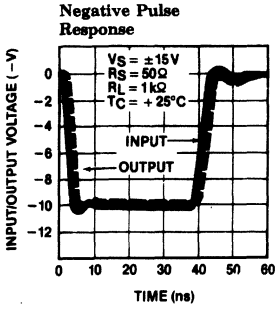
Supply Current vs Supply Voltage



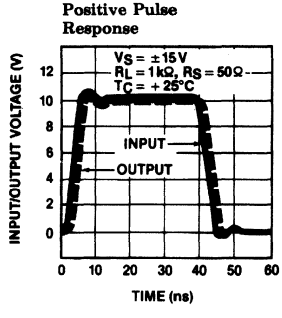
Output Voltage vs Supply Voltage



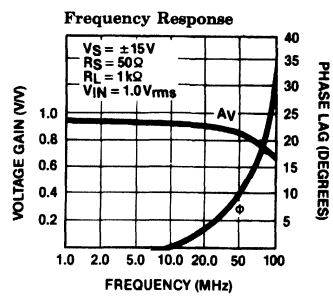
Negative Pulse Response



Positive Pulse Response



Frequency Response

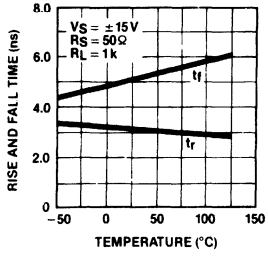


0033-3

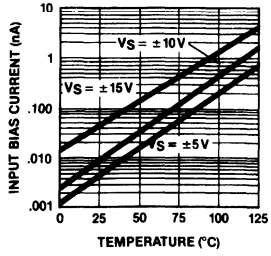
ELH0033G/883/8001401ZX
Fast Buffer Amplifier

Typical Performance Curves — Contd.

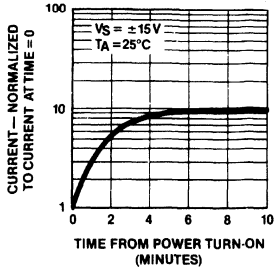
Rise and Fall Time vs Temperature



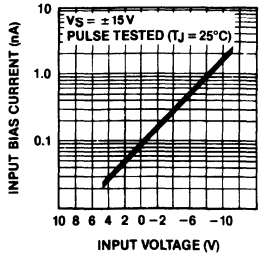
Input Bias Current vs Temperature



Normalized Input Bias Current During Warm-up



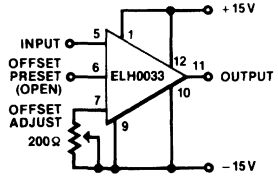
Input Bias Current vs Input Voltage



0033-4

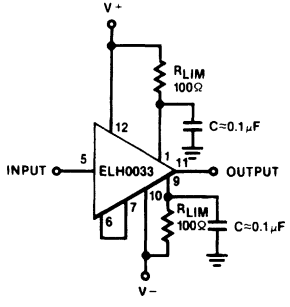
Typical Applications

Offset Zero Adjust



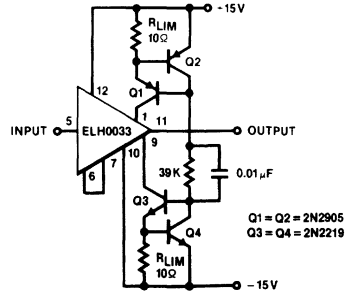
0033-5

Using Resistor Current Limiting



0033-6

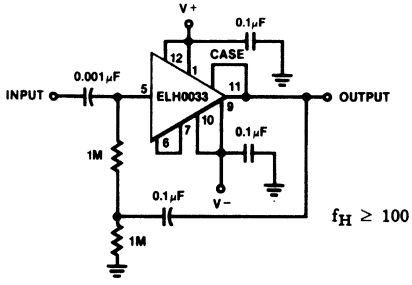
Current Limiting Using Current Sources



0033-7

Typical Applications — Contd.

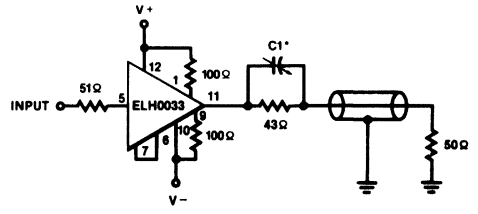
High Input Impedance AC Coupled Amplifier



$f_H \geq 100$ MHz

0033-8

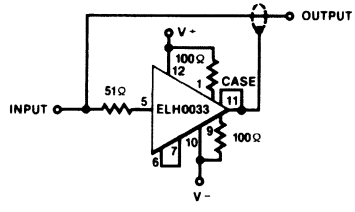
Coaxial Cable Driver



0033-9

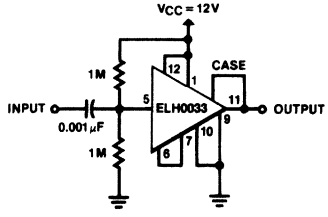
*Select C1 for optimum pulse response

Instrumentation Shield/Line Driver



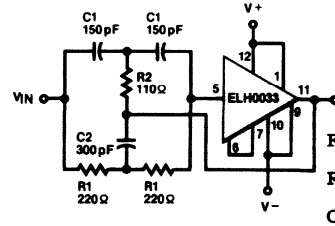
0033-10

Single Supply AC Amplifier



0033-11

4.5 MHz Notch Filter



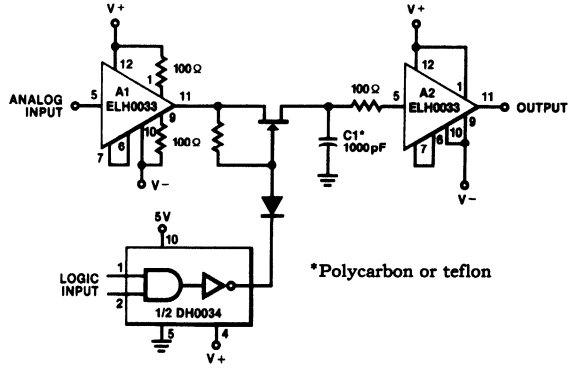
$$F_O = \frac{1}{2\pi R1C1}$$

$$R1 = 2\ R2$$

$$C1 = \frac{C2}{2}$$

0033-12

High-Speed Sample and Hold



*Polycarbon or teflon

0033-13

ELH0033G/883/8001401ZX
Fast Buffer Amplifier

Applications Information

Recommended Layout Precautions

RF/video printed circuit board layout rules should be followed when using the ELH0033 since it will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively, the case should be connected to the output to minimize input capacitance.

Offset Voltage Adjustment

The ELH0033's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. The pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω between the offset adjust pin and $V-$.

Operation from Single or Asymmetrical Power Supplies

This device type may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \cong (1 - A_V)\frac{(V^+ - V^-)}{2} = 0.005\,(V^+ - V^-)$$

where: A_V = No load voltage gain, typically 0.99
V^+ = Positive supply voltage
V^- = Negative supply voltage

For the above example, ΔV_O would be -35 mV. This may be adjusted to zero as described in Section 2. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the "typical applications" section.

Short Circuit Protection

In order to optimize transient response and output swing, output current limit has been omitted from the ELH0033. Short circuit protection may be added by inserting appropriate value resistors between $V+$ and V_C+ pins and $V-$ and V_C- pins. Resistor values may be predicted by:

$$R_{LIM} \cong \frac{V^+}{I_{SC}} = \frac{V^-}{I_{SC}}$$

where: $I_{SC} \leq 100$ mA for ELH0033

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_C+ and V_C- pins with capacitors to ground will retain full output swing for transient pulses. An alternate active current limit technique that retains full DC output swing uses current sources which are saturated during normal operation thus applying full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

$$R_{LIM} \cong \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\text{ mA}} = 10\Omega$$

Capacitive Loading

The ELH0033 is designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times d_v/d_t)$ should be limited below absolute maximum peak current ratings for the devices.

Thus:

$$\frac{\Delta V_{IN}}{\Delta t} \times C_L \leq I_{OUT} \leq \pm 250\text{ mA}$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below the total package power rating:

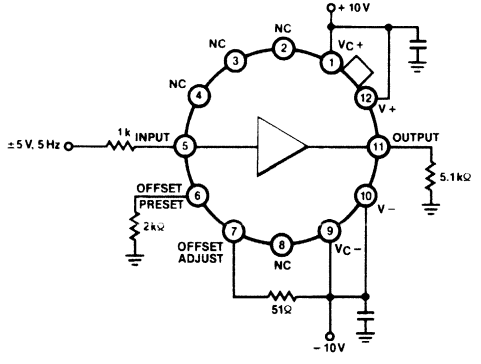
$$P_D \text{ pkg} \geq P_{DC} + P_{AC}$$
$$P_D \text{ pkg} \geq (V^+ - V^-) \times I_S + P_{AC}$$
$$P_{AC} \cong (V_{P\text{-}P})^2 \times f \times C_L$$

where: V_{P-P} = Peak-to-peak output voltage swing
f = Frequency
C_L = Load Capacitance

Operation within an Op Amp Loop

Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as the ELH0032 and HA2500 and HA2600 series. An isolation resistor of 47Ω should be used between the op amp output and the input of ELH0033. The wide bandwidth and high slew rates of the ELH0033 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

Burn-In Circuit



0033-14

Hardware

In order to utilize the full drive capabilities of the ELH0033, it should be mounted with a heatsink, particularly for extended temperature operation. The case is isolated from the circuit and may be connected to system chassis.

IMPORTANT!

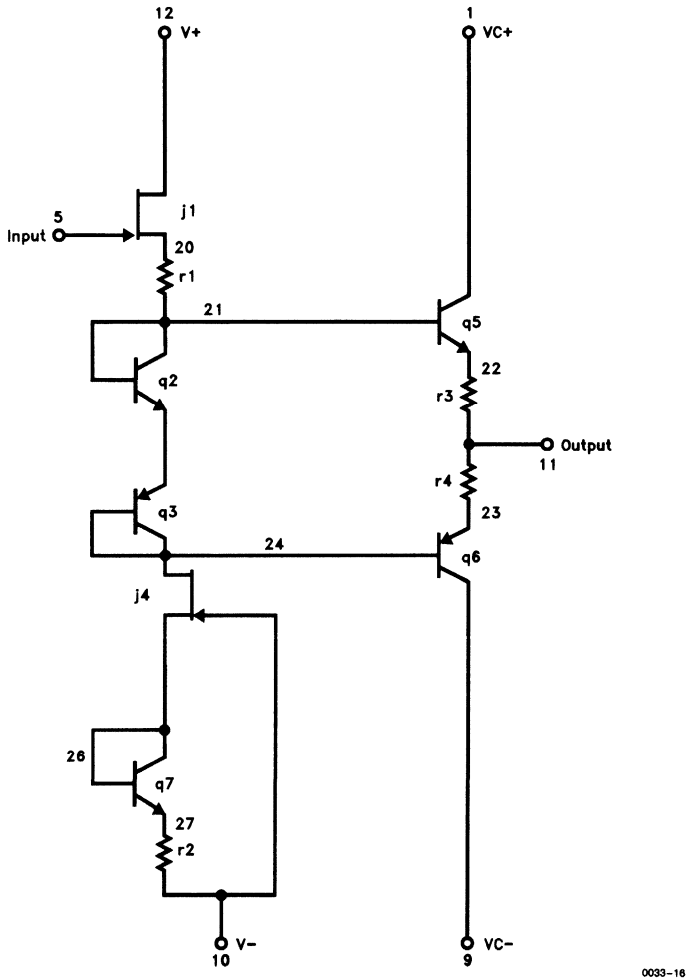
Power supply bypassing is necessary to prevent oscillation with the ELH0033 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within ¼" to ½" of the device package) to a ground plane. Capacitors should be one or two 0.1μF in parallel; adding a 4.7 μF solid tantalum capacitor will help in troublesome instances.

ELH0033G/883/8001401ZX
Fast Buffer Amplifier

ELH0033 Macromodel

```
* Connections:      input
*                   |     V+
*                   |     |     Vc+
*                   |     |     |     V-
*                   |     |     |     |     Vc-
*                   |     |     |     |     |     output
*                   |     |     |     |     |     |
.subckt M0033       5     12    1     10    9     11
* Models
.model qn npn (is=5e-14 bf=150 vaf=100 re=1 rb=5 re=1 ikf=200mA
+cje=5pF cjc=5pF mje=.42 mjc=.23 tf=.3nS tr=200nS br=5 vtf=0)
.model qp pnp (is=5e-14 bf=150 vaf=100 rc=.2 rb=3 re=1 ikf=100mA
+cje=5.7pF cjc=4pF tf=.3nS mje=.32 mjc=.43 tr=170nS br=5 vtf=0)
.model qf njf (vto=-3V beta=4.0e-3 cgd=4pF cgs=10pF lambda=671.0e-6)
* Resistors
r1 20 21 58.33
r2 27 10 58.33
r3 22 11 2
r4 11 23 2
* Transistors
j1 12 5 20 qf
j4 24 10 26 qf
q2 21 21 25 qn
q3 24 24 25 qp
q5 1 21 22 qn
q6 9 24 23 qp
q7 26 26 27 qn
.ends
```

ELH0033 Macromodel — Contd.



élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELH0041G/883/8508701ZX
0.1 Amp Power Operational Amplifier

Features

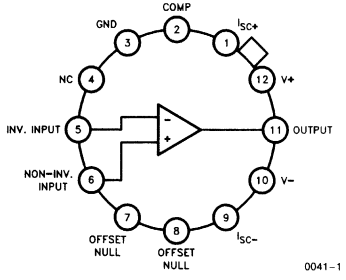
- High output current—200 mA
- Excellent open-loop gain—106 dB
- Low offset voltage—1 mV
- Wide full power bandwidth—20 kHz
- High slew rate—3 V/μs
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Pkg.	Outline #
ELH0041G/883B	−55°C to +125°C	TO-8	MDP002

8508701ZX is the SMD version of this device.

Connection Diagram



Top View

General Description

The ELH0041 are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC op amps; the ELH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload. These devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

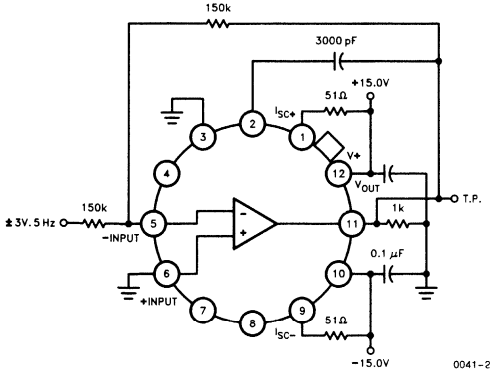
For applications requiring output currents in excess of 1A, see the ELH0021 data sheet.

The excellent input characteristics and high output capability of the ELH0041 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

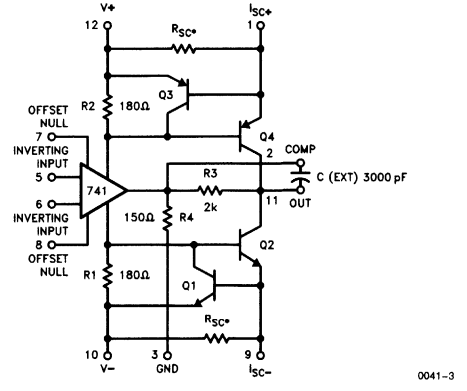
The ELH0041 is particularly suited for applications such as torque drivers for inertial guidance systems, diddle yoke drivers for alphanumeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Burn-In Circuit



Equivalent Schematic



ELH0041G/883/8508701ZX

0.1 Amp Power Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

V_S	Supply Voltage	±18V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage (Note 1)	±15V		ELH0041	−55°C to +125°C
P_D	Power Dissipation (See curves)		T_{ST}	Storage Temperature	−65°C to +150°C
	Differential Input Voltage	±30V		Lead Temperature	
	Peak Output Current (Note 2)	0.5A		(Soldering, 10 seconds)	300°C
	Output Short Circuit Duration (Note 3)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \le T_A \le T_{MAX}$, C_C = 3000 pF

Parameter	Description	Test Conditions	ELH0041 Min	Typ	Max	Test Level	Units
V_{OS}	Input Offset Voltage	$R_S \le 100\Omega$, T_A = 25°C (Note 4)		1	3	I	mV
		$R_S \le 100\Omega$ (Note 4)			5	I	mV
$\Delta V_{OS}/\Delta T$	Voltage Drift with Temperature	$R_S \le 100\Omega$		3		V	μV/°C
	Offset Voltage Drift with Time	T_A = 25°C		5		V	$\mu V/\sqrt{wk}$
$\Delta V_{OS}/\Delta P$	Offset Voltage Change with Output Power			15		V	μV/W
	Offset Voltage Adjustment Range			20		V	mV
I_{OS}	Input Offset Current	T_A = 25°C (Note 4)		30	100	I	nA
		(Note 4)			300	I	nA
	Offset Current Drift with Temperature			0.1	1	IV	nA/°C
	Offset Current Drift with Time	T_A = 25°C		2		V	$nA/\sqrt{wk}$
I_B	Input Bias Current	T_A = 25°C (Note 4)		100	300	I	nA
		(Note 4)			1	I	μA
R_{IN}	Input Resistance	T_A = 25°C	0.3	1		I	MΩ

ELH0041G/883/8508701ZX
0.1 Amp Power Operational Amplifier

DC Electrical Characteristics $V_S = \pm 15V, T_{MIN} \leq T_A \leq T_{MAX}, C_C = 3000\ pF$ — Contd.

Parameter	Description	Test Conditions	ELH0041				Units
			Min	Typ	Max	Test Level	
CMRR	Common-Mode Rejection Ratio	$R_S \leq 100\Omega, V_{CM} = \pm 10V$	70	90		I	dB
V_{INCM}	Input Voltage Range		±12			IV	V
PSRR	Power Supply Rejection Ratio	$R_S \leq 100\Omega, V_S = \pm 5V$ to $\pm 15V$	80	96		I	dB
A_V	Voltage Gain (Note 5)	$V_O = \pm 10V, R_L = 1\ k\Omega, T_A = 25°C$	100	200		I	V/mV
		$V_O = \pm 10V, R_L = 100\Omega$	25			I	V/mV
V_O	Output Voltage Swing	$R_L = 100\Omega$	±13	14		I	V
I_{SC}	Output Short Circuit Current	$T_A = 25°C, R_{SC} = 3.3\Omega$		200	300	I	mA
I_S	Supply Current	$V_{OUT} = 0V$		2.5	3.5	I	mA
P_C	Power Consumption	$V_{OUT} = 0V$		75	105	I	mW

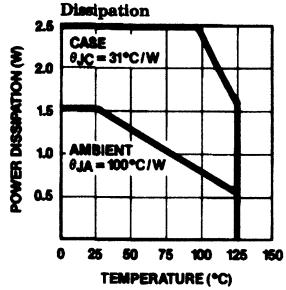
Note 1: Rating applies for supply voltages above ±15V. For supplies less than ±15V, rating is equal to supply voltage.
Note 2: Rating applies for LH0041G with $R_{SC} = 0\Omega$.
Note 3: Rating applies as long as package power rating is not exceeded.
Note 4: Specifications apply for $\pm 5V \leq V_S \leq 18V$.
Note 5: The ELH0041, like all Class B amplifiers, has a "dead band" when V_{OUT} is near zero volts. Typical values for the "dead band" are in the 50 μV to 200 μV range. Open-loop gain is measured at V_{OUT} from ±0.5 V_{DC} to ±10 V_{DC} which is out of the range of the "dead band".

AC Electrical Characteristics $T_A = 25°C, V_S = \pm 15V, C_C = 3000\ pF$

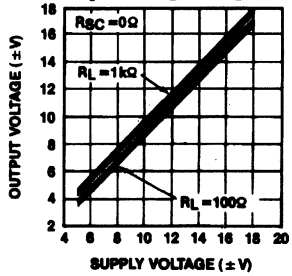
Parameter	Description	Test Conditions	ELH0041				Units
			Min	Typ	Max	Test Level	
SR	Slew Rate	$A_V = 1, R_L = 100\Omega$	1.5	3		I	V/μs
BW	Bandwidth	$R_L = 100\Omega$		20		V	kHz
t_r, t_f	Small Signal Rise or Fall Time			0.3	1	I	μs
	Small Signal Overshoot			5	20	I	%
t_S	Settling Time (0.1%)	$\Delta V_{IN} = 10V, A_V = 1$		4		V	μs
	Overload Recovery Time			3		V	μs
HD	Harmonic Distortion	$f = 1\ kHz, P_O = 0.5W$		0.2		V	%
E_N	Input Noise Voltage	$R_S = 50\Omega$, BW = 10 Hz to 10 kHz		5		V	μV_{rms}
I_N	Input Noise Current	BW = 10 Hz to 10 kHz		0.05		V	nA_{rms}
C_{IN}	Input Capacitance			3		V	pF

Typical Performance Curves

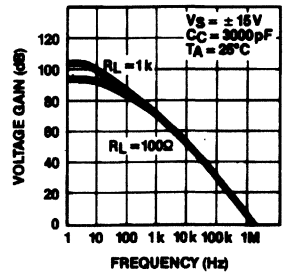
Maximum Power Dissipation



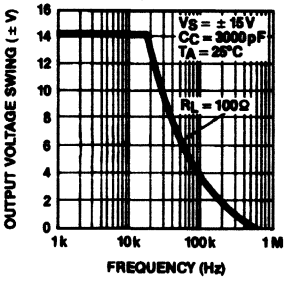
Output Voltage Swing



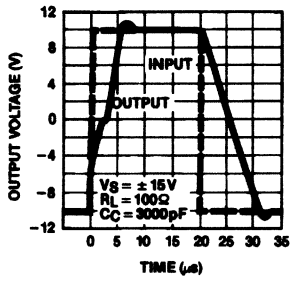
Open-Loop Frequency Response



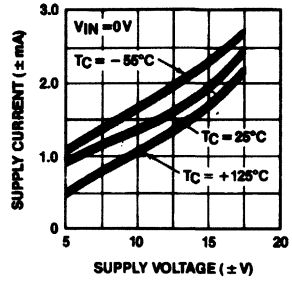
Large Signal Pulse Response



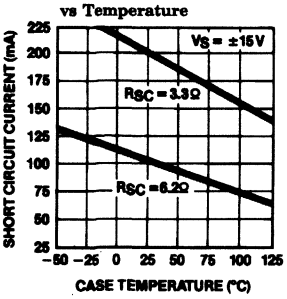
Voltage Follower Pulse Response



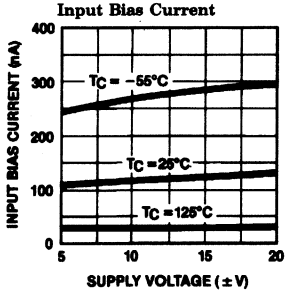
No Load Supply Current



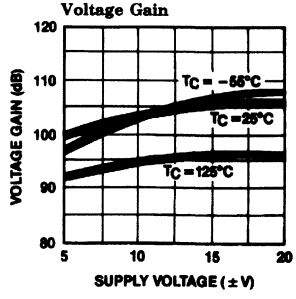
Short Circuit Current vs Temperature



Input Bias Current



Voltage Gain



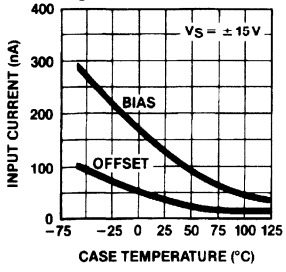
0041-4

9

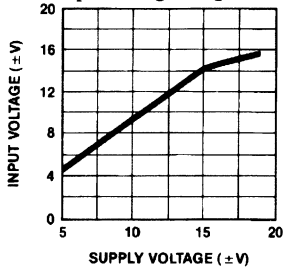
ELH0041G/883/8508701ZX
0.1 Amp Power Operational Amplifier

Typical Performance Curves — Contd.

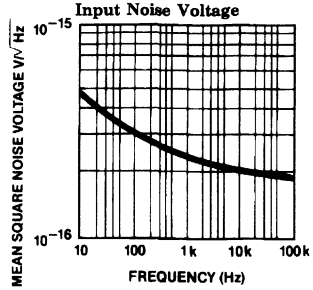
Input Current



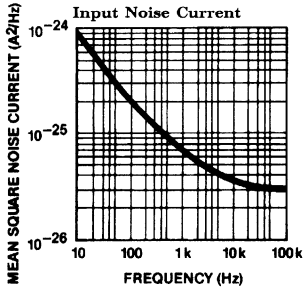
Input Voltage Range



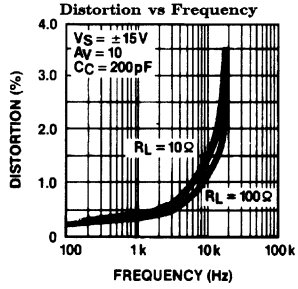
Input Noise Voltage



Input Noise Current



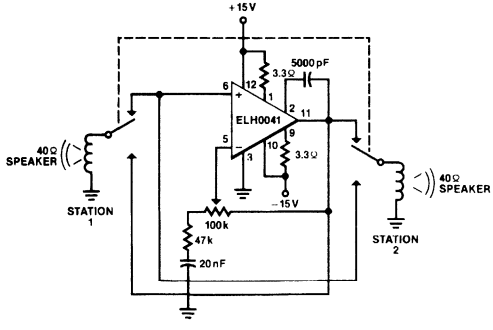
Distortion vs Frequency



0041-5

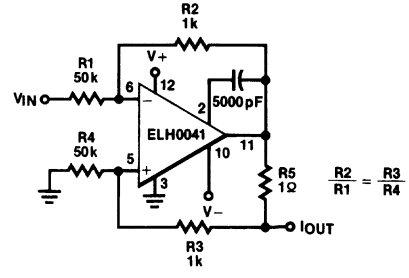
Typical Applications

Two Way Intercom



0041-6

Programmable High Current Source/Sink

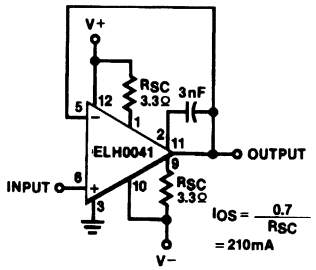


0041-7

$$I_{OUT} = \frac{V_{IN}}{R5}\left(\frac{R2}{R1}\right) + \frac{V_{OUT}}{R1 + R2} = 20\ mA/V_{IN}$$

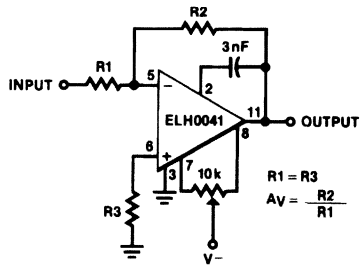
Typical Applications — Contd.

Unity Gain with Short Circuit Limiting



0041-8

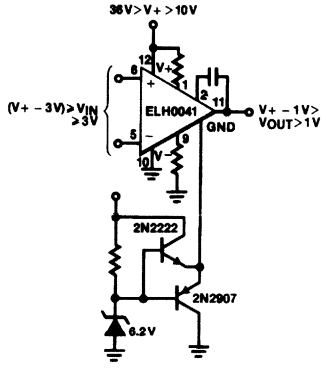
Offset Voltage Null Circuit



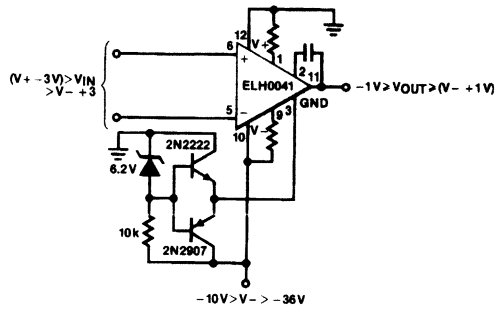
0041-9

Operation from Single Supplies

Positive



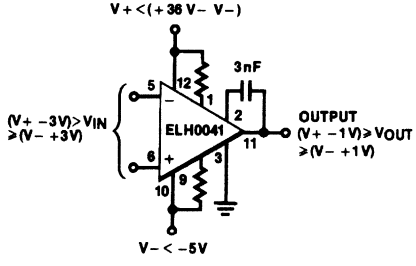
Negative



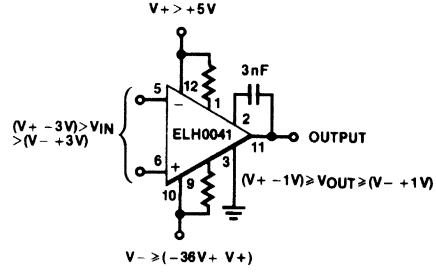
0041-10

0041-11

Operation from Non-Symmetrical Supplies



0041-12



0041-13

élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELH0101/883/8508901/2YX
Power Operational Amplifier

Features

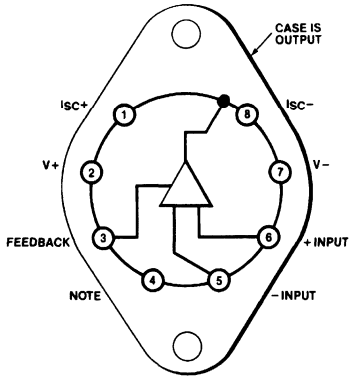
- 5A peak, 2A continuous output current
- 10 V/μs slew rate
- 300 kHz power bandwidth
- 850 mW standby power (±15V supplies)
- 300 pA input bias current
- Virtually no crossover distortion
- 2 μs settling time to 0.01%
- 5 MHz gain bandwidth
- MIL-STD-883 devices 100% manufactured in U.S.A.

Ordering Information

Part No.	Temp. Range	Package	Outline #
ELH0101AK/883B	−55°C to +125°C	TO-3	MDP0003
ELH0101K/883B	−55°C to +125°C	TO-3	MDP0003

8508901YX and 8508902YX are the SMD versions of this device.

Connection Diagram



0101-1

Top View

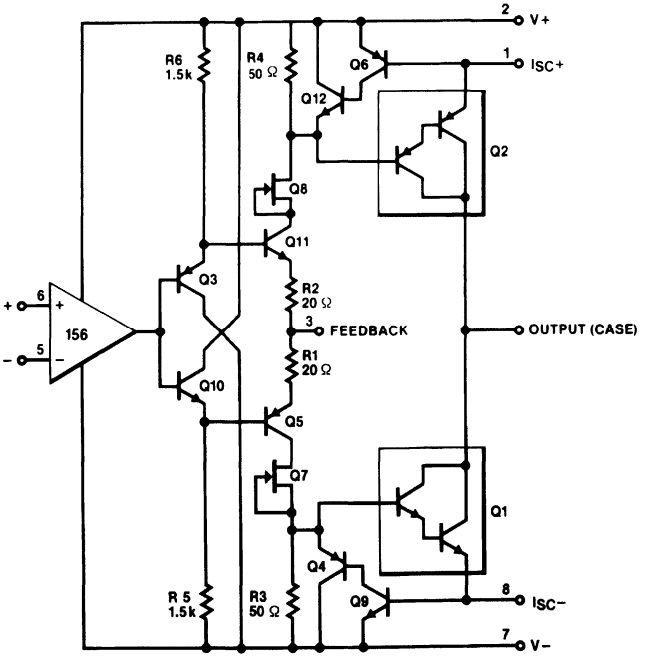
Note: Electrically connected internally. No connection should be made to pin.

General Description

The ELH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the ELH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drivers, programmable power supplies, and disk head positioner amplifiers.

Elantec facilities comply with MIL-I-45208A and other applicable quality specifications. Elantec's Military devices are 100% fabricated and assembled in our rigidly controlled, ultra-clean facilities in Milpitas, California. For additional information on Elantec's Quality and Reliability Assurance policy and procedures request brochure QRA-1.

Equivalent Schematic



0101-2

Absolute Maximum Ratings

V_S	Supply Voltage		V_{IN}	Input Voltage Range	
	ELH0101, ELH0101A	±22V		ELH0101, ELH0101A	±20V but < $\pm V_S$
P_D	Power Dissipation at T_A = 25°C	5W		Peak Output Current (50 ms pulse)	5A
	Derate linearly at 25°C/W			Output Short Circuit Duration	
	to zero at 150°C			(within rated power dissipation,	
P_D	Power Dissipation at T_C = 25°C	62W		R_{SC} = 0.35Ω, T_A = 25°C)	Continuous
	Derate linearly at 2°C/W		T_A	Operating Temperature Range:	
	to zero at 150°C			ELH0101, ELH0101A	−55°C to +125°C
	Differential Input Voltage		T_J	Maximum Junction Temperature	150°C
	ELH0101, ELH0101A	±40V but < $\pm V_S$	T_{ST}	Storage Temperature	−65°C to +150°C
				Lead Temperature	
				(Soldering, 10 seconds)	300°C

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics (Note 1) V_S = ±15V, T_A = 25°C, V_{CM} = 0V

Parameter	Description	Test Conditions	ELH0101			ELH0101A			Test Level	Units
			Min	Typ	Max	Min	Typ	Max		
V_{OS}	Input Offset Voltage			1	10		1	3	I	mV
		$T_{MIN} \le T_A \le T_{MAX}$, ELH0101			15			7	I	mV
$\Delta V_{OS}/\Delta P_D$	Change in Input Offset Voltage with Dissipated Power	(Note 2)		150			150		V	µV/W
$\Delta V_{OS}/\Delta T$	Change in Input Offset Voltage with Temperature			10			10		V	µV/°C
I_B	Input Bias Current				1,000			300	I	pA
		$T_A \le T_{MAX}$, ELH0101			1,000			300	I	nA

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ELH0101/883/8508901/2YX
Power Operational Amplifier

DC Electrical Characteristics (Note 1) $V_S = \pm 15V$, $T_A = 25°C$, $V_{CM} = 0V$ — Contd.

Parameter	Description	Test Conditions	ELH0101			ELH0101A			Test Level	Units
			Min	Typ	Max	Min	Typ	Max		
I_{OS}	Input Offset Current				250			75	I	pA
		$T_A \leq T_{MAX}$, ELH0101, A			250			75	I	nA
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 10\Omega$	50	200		50	200		I	V/mV
V_O	Output Voltage Swing	$R_{SC} = 0\Omega$, $A_V = 1$, $R_L = 100\Omega$ (Note 3)	± 11.7	± 12.5		± 11.7	± 12.5		I	V
		$R_{SC} = 0\Omega$, $A_V = 1$, $R_L = 10\Omega$ (Note 3)	± 11	± 11.6		± 11	± 11.6		I	V
		$R_{SC} = 0\Omega$, $A_V = 1$, $R_L = 5\Omega$ (Note 3)	± 10.5	± 11		± 10.5	± 11		I	V
CMRR	Common-Mode Rejection Ratio	$V_{IN} = \pm 10V$	85	100		85	100		I	dB
PSRR	Power Supply Rejection Ratio	$\pm 5V \leq V_S \leq \pm 15V$	85	100		85	100		I	dB
		$+5V \leq V_{S(+)} \leq +15V$, $V_{S(-)} = -15V$	80	110		80	110		I	dB
		$-5V \geq V_{S(-)} \geq -15V$, $V_{S(+)} = +15V$	80	95		80	95		I	dB
I_S	Supply Current			28	35		28	35	I	mA

AC Electrical Characteristics $V_S = \pm 15V$, $T_A = T_C = T_J = 25°C$

Parameter	Description	Test Conditions	ELH0101			ELH0101A			Test Level	Units
			Min	Typ	Max	Min	Typ	Max		
e_n	Equivalent Input Noise Voltage	f = 1 kHz		25			25		V	$nV/\sqrt{Hz}$
C_{IN}	Input Capacitance	f = 1 MHz		3			3		V	pF
PBW	Power Bandwidth, −3 dB	$R_L = 10\Omega$, $A_V = 1$		300			300		V	kHz
SR	Slew Rate	$R_L = 10\Omega$, $A_V = 1$ ELH0101AK	7.5	10		7.5	10		I	$V\mu s$
t_r, t_f	Small Signal Rise or Fall Time	$R_L = 10\Omega$, $A_V = 1$		200			200		V	ns
	Small Signal Overshoot	$R_L = 10\Omega$, $A_V = 1$		10			10		V	%

AC Electrical Characteristics $V_S = \pm 15V, T_A = T_C = T_J = 25°C$ — Contd.

Parameter	Description	Test Conditions	ELH0101			ELH0101A			Test Level	Units
			Min	Typ	Max	Min	Typ	Max		
GBW	Gain-Bandwidth Product	$R_L = \infty, A_V = 1$ ELH0101AK	4	5		4	5		I	MHz
t_S	Large Signal Settling Time (0.01%)	$R_L = \infty, A_V = 1$		2			2		V	μs
THD	Total Harmonic Distortion	$f = 1$ kHz, $P_O = 0.5W$, $R_L = 10\Omega$		0.008			0.008		V	%

Note 1: Specification is at $T_A = 25°C$. Actual values at operating temperature may differ from the $T_A = 25°C$ value. When supply voltages are ±15V, quiescent operating junction temperature will rise approximately 20°C without heatsinking. Accordingly, V_{OS} may change 0.5 mV and I_B and I_{OS} will change significantly during warm-ups. Refer to I_B vs. temperature and power dissipation graphs for expected values.

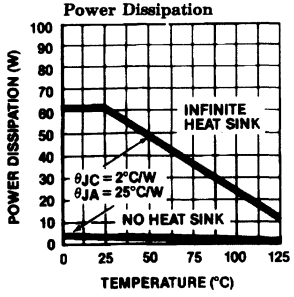
Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heatsink.

Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation. R_{SC} is the current sense resistor.

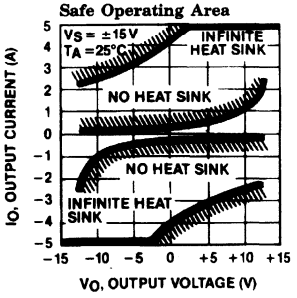
ELH0101/883/8508901/2YX
Power Operational Amplifier

Typical Performance Curves

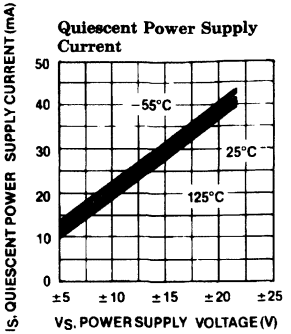
Power Dissipation



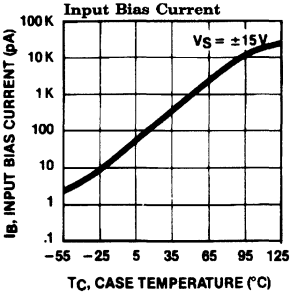
Safe Operating Area



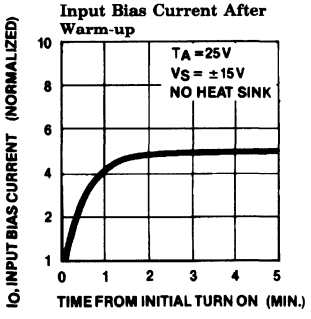
Quiescent Power Supply Current



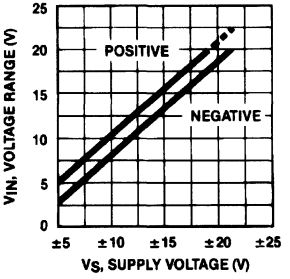
Input Bias Current



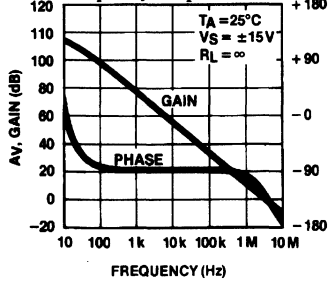
Input Bias Current After Warm-up



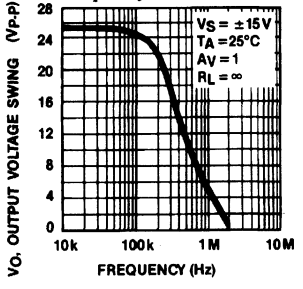
Input Common-Mode Voltage Range



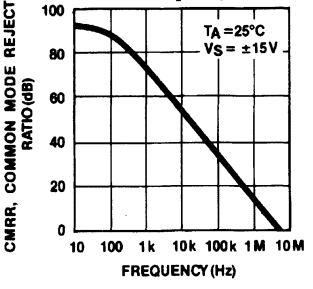
Open-Loop Small Signal Frequency Response



Output Voltage Swing vs Frequency



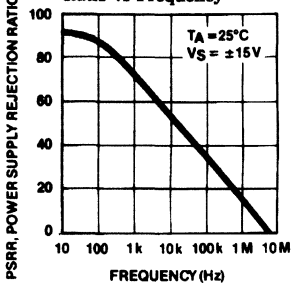
Common-Mode Rejection Ratio vs Frequency



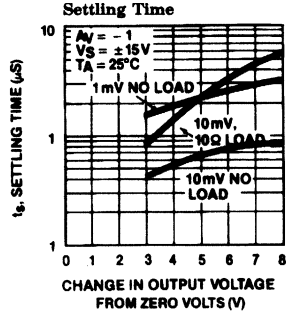
0101-3

Typical Performance Curves — Contd.

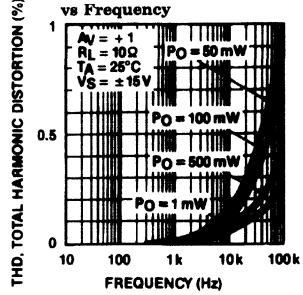
Power Supply Rejection Ratio vs Frequency



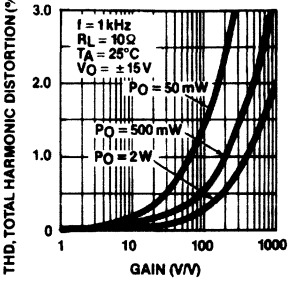
Settling Time



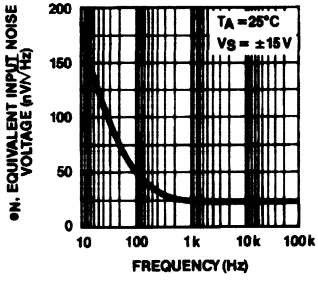
Total Harmonic Distortion vs Frequency



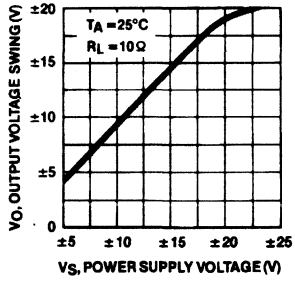
Total Harmonic Distortion vs Gain



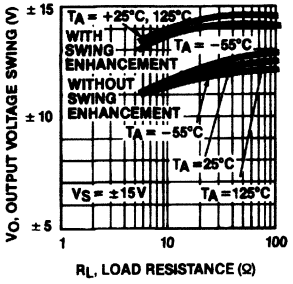
Equivalent Input Noise Voltage



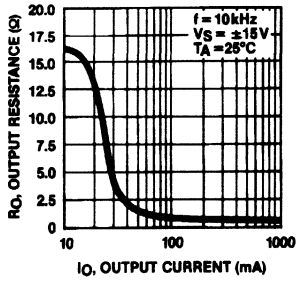
Output Voltage Swing with Swing Enhancement



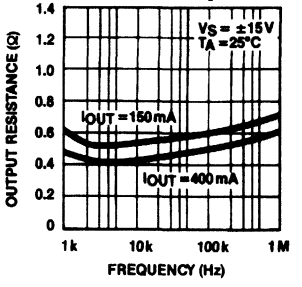
Output Voltage Swing vs Load Resistance



Open-Loop Output Resistance



Open-Loop Output Resistance vs Frequency



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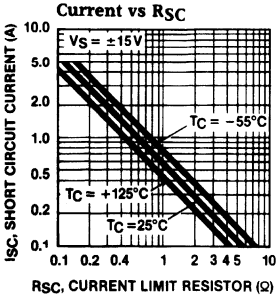
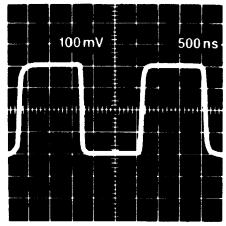
ELH0101/883/8508901/2YX
Power Operational Amplifier

Typical Performance Curves — Contd.

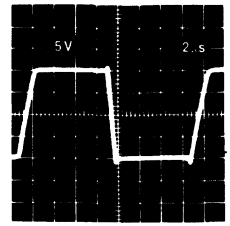
Short Circuit Current vs R_{SC}



Small Signal Pulse Response



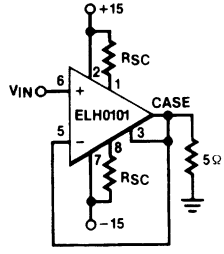
Large Signal Pulse Response



0101-5

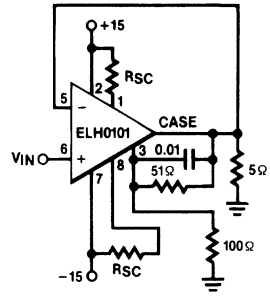
Typical Applications

High Power Voltage Follower



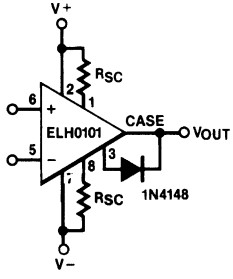
0101-6

High Power Voltage Follower with Swing Enhancement



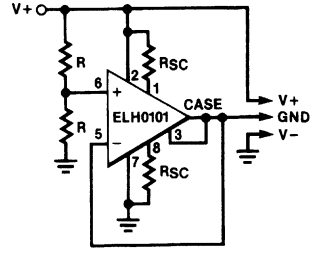
0101-7

Restricting Outputs to Positive Voltage Only



0101-8

Generating a Split Supply from a Single Voltage Supply



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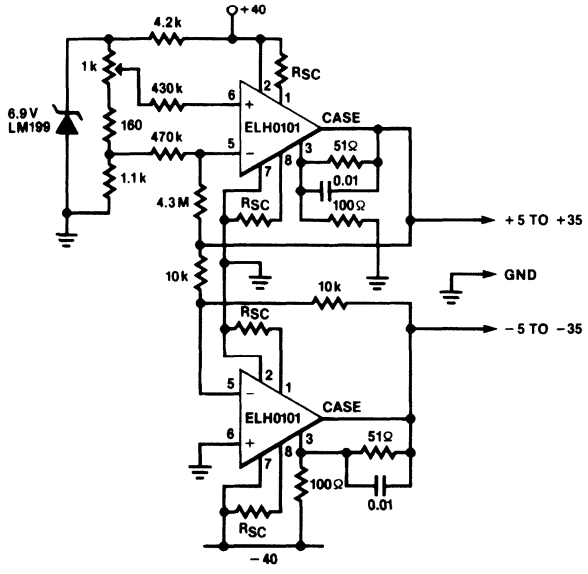
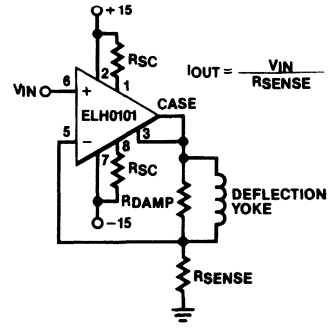
Typical Applications — Contd.

±5 to ±35 Power Source or Sink



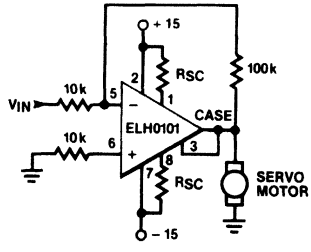
0101-10

CRT Deflection Yoke Driver



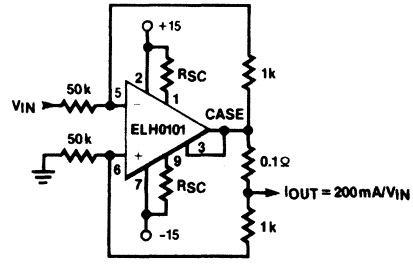
0101-11

DC Servo Amplifier



0101-12

High Current Source/Sink



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ELH0101/883/8508901/2YX
Power Operational Amplifier

Applications Information

Input Voltages

The ELH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however; if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the ELH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μF bypass on the supply bus.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the ELH0101.

Layout Considerations

When working with circuitry capable of resolving picoampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs.

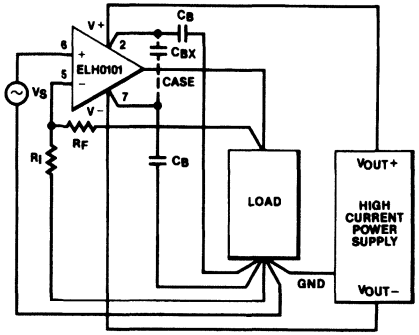
Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the ELH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

Applications Information — Contd.

Every attempt should be made to achieve a single point ground system as shown in the figure below.



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Bypass capacitor C_{BX} should be used if the lead lengths of bypass capacitors C_B are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the ELH0101 is capable of producing.

Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC− should be shorted to V−. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit will be approximately 0.3%.

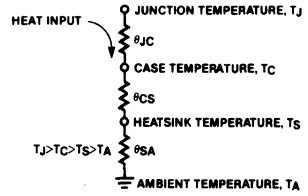
Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D} °C/W \qquad (1)$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heatsink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures, T_J, T_C, and T_S, (no temperature distribution in junction, case, or heatsink). Nevertheless, this is a reasonable approximation of actual performance.



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*Short circuit current will be limited to approximately $\frac{0.6}{RSC}$.

The junction-to-case thermal resistance, θ_{JC}, specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heatsink thermal resistance, θ_{CS}, depends on the mounting of the device to the heatsink and upon the area and quality of the contact surface. Typical θ_{CS} for a TO-3 package is 0.5°C/W to 0.7°C/W, and 0.3°C/W to 0.5°C/W using silicone grease.

The heatsink to ambient thermal resistance, θ_{SA}, depends on the quality of the heatsink and the ambient conditions.

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Power Operational Amplifier

Application Information — Contd.

Cooling is normally required to maintain the worst case operating junction temperature, T_J, of the device below the specified maximum value, $T_{J(MAX)}$. T_J can be calculated from known operating conditions. Rewriting equation (1), we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} °C/W$$

$$T_J = T_A + P_D\theta_{JA} °C$$

Where: $P_D = (V_S - V_{OUT})\, I_{OUT} + |V \pm (V-)|I_Q$

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and
V_S = Supply Voltage

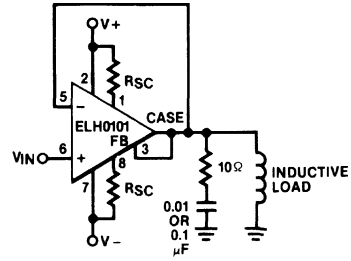
θ_{JC} for the ELH0101 is typically 2°C/W.

Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

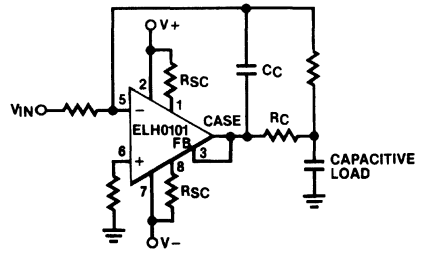
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Some inductive loads may cause output stage oscillation. A 0.01 μF ceramic capacitor in series with a 10Ω resistor from the output to ground will usually remedy this situation.



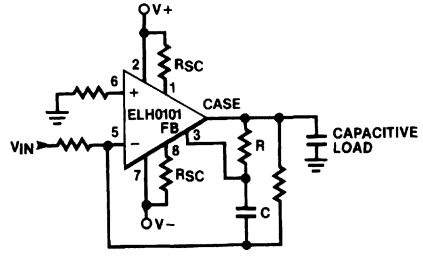
0101-16

Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley.)



0101-17

A similar but alternative technique may be used for the ELH0101.



0101-18

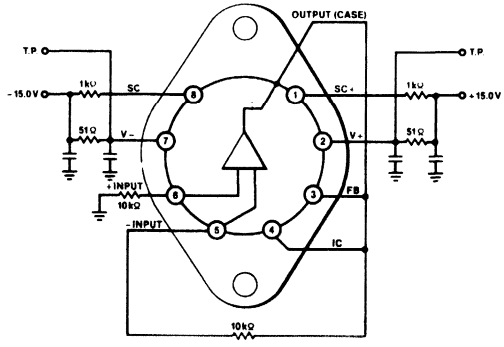
Output Swing Enhancement

When the feedback pin is connected directly to the output, the output voltage swing is limited by the driver stage and not by output saturation. Output swing can be increased by taking gain in the output stage as shown below in the High Power Voltage Follower with Swing Enhancement. Whenever gain is taken in the output stage, either the output stage, or the entire op amp must be appropriately compensated to account for the additional loop gain.

Output Resistance

The open-loop output resistance of the ELH0101 is a function of the load current. No-load output resistance is approximately 10Ω. This decreases to under an Ω for load currents exceeding 100 mA.

Burn-In Circuit



ELH0101 Macromodel

```
* Connections:  +input
*               |     -Input
*               |     |     V+
*               |     |     |     Isc+
*               |     |     |     |     Feedback
*               |     |     |     |     |     V-
*               |     |     |     |     |     |     Isc-
*               |     |     |     |     |     |     |     Output
*               |     |     |     |     |     |     |     |
* em0101        6     5     2     1     3     7     8     4
.subckt buffer  21          2     1     3     7     8     4
* Resistors
r1 3 27 10
r2 26 3 10
r3 30 7 50
r4 2 23 50
r5 29 7 2K
r6 2 22 2K
r7 27 28 10
r8 24 26 10
* Transistors
q1 4 30 8 qnd
d1 8 4 dclamp
q2 4 23 1 qpd
d2 4 1 dclamp
q3 7 21 22 qp
q4 23 22 24 qn
q5 21 21 26 qn
q6 23 1 2 qp
q7 2 21 29 qn
q8 27 27 21 qn
q9 30 29 28 qp
q10 30 8 7 qn
* Models
.model qpd pnp (is=88.013e-12 ikf=5A tf=32nS vaf=50V cje=45pF cjc=60pF
+xtb=2.1 bf=12000 ne=4 ise=1e - 10)
.model qnd npn (is=88.013e-12 ikf=5A tf=32nS vaf=50V cje=45pF cjc=60pF
+xtb=2.1 bf=12000 ne=4 isc=1e - 10)
.model dclamp d (is=10e-28 tt=100nS)
```

ELH0101 Macromodel — Contd.

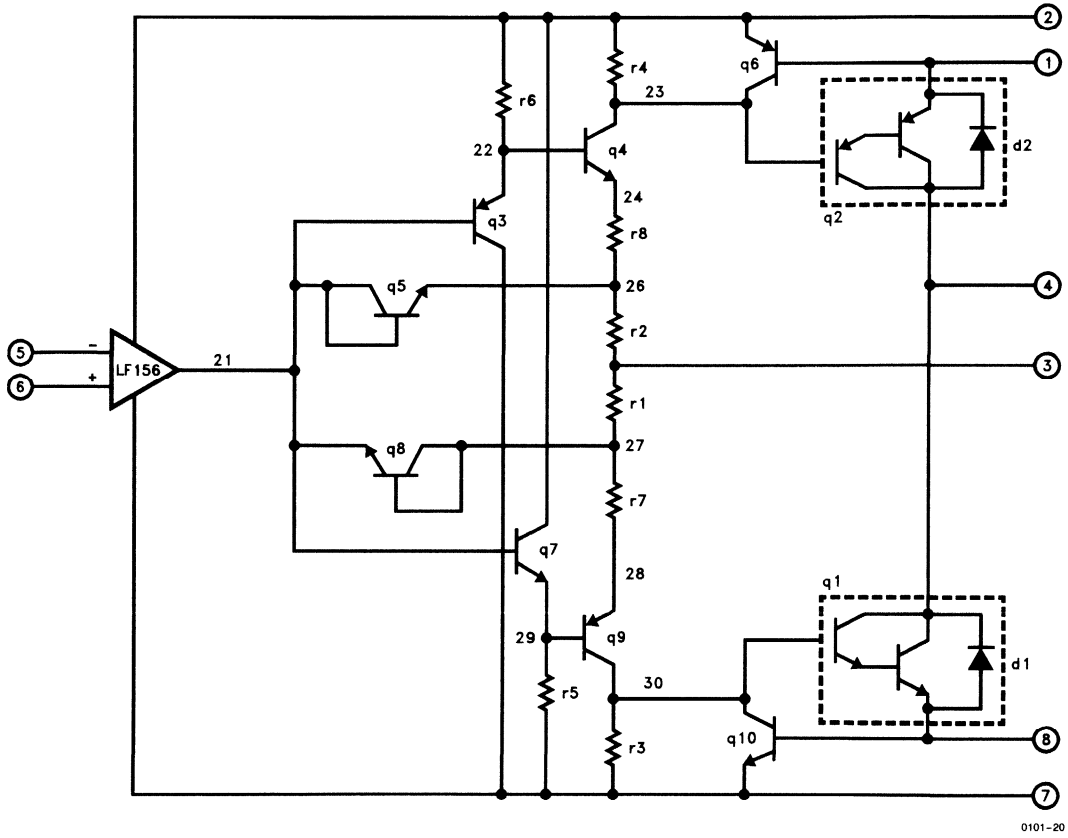
```
.model qp pnp (is=10e-15 xti=3 eg=1.11V vaf=91V bf=200 ne=2.321 ise=6.2fA
+ikf=500mA xtb=2.1 br=3.3 nc=2 cjc=14.6pF vjc=0.75V mjc=0.3333 fc=0.5 cje=20pF
+vje=0.75V mje=0.3333 tr=29nS tf=0.4nS itf=0.4 vtf=10 xtf=2 rb=10)
.model qn npn (is=3e-15 xti=3 eg=1.11V vaf=151V bf=220 ne=1.541 ise=14fA
+ikf=500mA xtb=2.1 br=6 nc=2 cjc=14.6pF vjc=0.75V mjc=0.3333 fc=0.5 cje=26pF
+vje=0.75V mje=0.3333 tr=51nS tf=0.4nS itf=0.6 vtf=1.7 xtf=2 rb=10)
.ends buffer
* lf156 Subcircuit
* Connections:      +Input
*                   |     -Input
*                   |     |     V+
*                   |     |     |     V-
*                   |     |     |     |     Output
*                   |     |     |     |     |
.subckt lf156        6     5     2     7     21
* Input Stage
vcm2 40 7 2
rd1 40 80 1.06K
rd2 40 90 1.06K
j1 80 102 12 jm1
j2 90 103 12 jm2
cin 5 6 4pF
rg1 5 102 2
rg2 6 103 2
* CM Clamp
dcm1 107 103 dm4
dcm2 105 107 dm4
vcmc 105 7 4V
ecmp 106 7 103 7 1
rcmp 107 106 10K
dcm3 109 102 dm4
dcm4 105 109 dm4
ecmn 108 2 102 2 1
rcmn 109 108 10K
cl 80 90 15pF
iss 2 12 0.48mA
gosit 2 12 90 80 2.4e-4
* Intermediate Stage
gcm 0 88 12 0 9.425e-9
ga 88 0 80 90 9.425e-4
r2 88 0 100K
c2 91 88 30pF
gb 91 0 88 0 28.6
ro2 91 0 74
```

ELH0101/883/8508901/2YX
Power Operational Amplifier

ELH0101 Macromodel — Contd.

```
* Output Stage
rso 91 21 1
ecl 18 0 91 21 20.69
gcl 0 88 20 0 1
rcl 20 0 1K
d1 18 20 dm1
d2 20 18 dm1
d3a 131 70 dm3
d3b 13 131 dm3
gpl 0 88 70 2 1
vc 13 21 3.1552V
rpla 2 70 10K
rplb 2 131 100K
d4a 60 141 dm3
d4b 141 14 dm3
gnl 0 88 60 7 1
ve 21 14 3.1552V
rnla 60 7 10K
rnlb 141 7 100K
ip 2 7 4.52mA
dsub 7 2 dm2
* Models
.model jm1 pjf (is=3.15e-11 beta=9.2528e-4 vto=-1.0)
.model jm2 pjf (is=2.85e-11 beta=9.2528e-4 vto=-0.999)
.model dm1 d (is=1.0e-15)
.model dm2 d (is=8.0e-16 bv=52.8)
.model dm3 d (is=1.0e-16)
.model dm4 d (is=1.0e-9)
ends lf156
* lf156 model courtesy of Linear Technology Corp.
```

ELH0101 Macromodel — Contd.



Package Outlines

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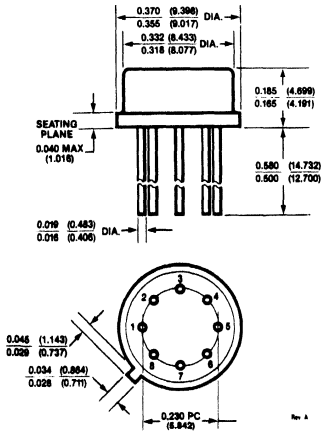
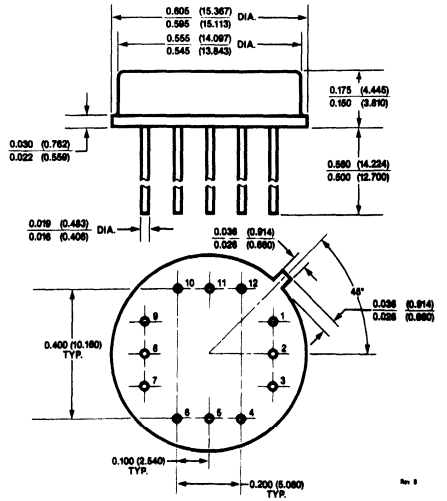
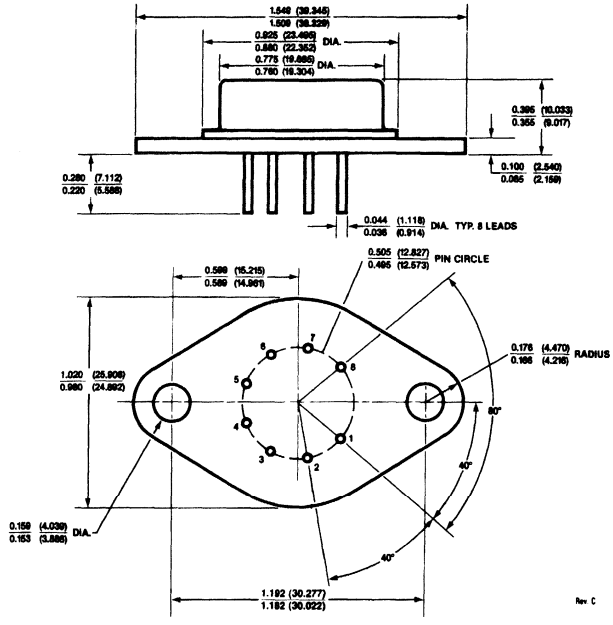
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS



MDP0001 Rev. A
8-Lead TO-5 Metal Can Package
Lead Finish (Coml)—Tin Plate
Lead Finish (Mil)—Gold or Hot Solder DIP

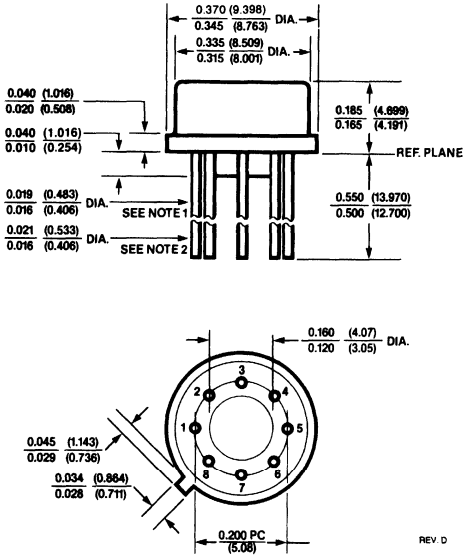


MDP0002 Rev. B
12-Lead TO-8 Metal Can Package
Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Gold or Hot Solder DIP



MDP0003 Rev. C
8-Lead TO-3 Metal Can Package
Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Hot Solder DIP

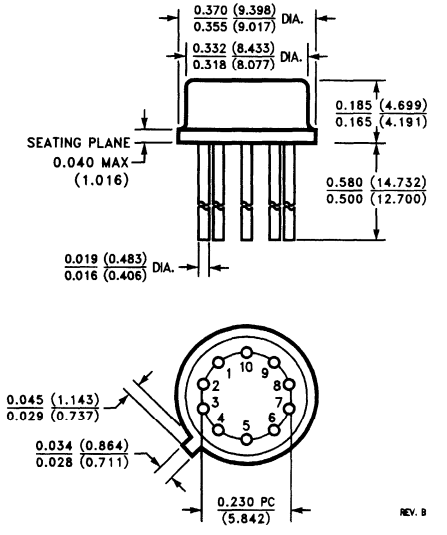
Package Outlines



Note 1: Tolerance applies between the seating plane and 0.250 from the reference plane.
Note 2: Tolerance applies between 0.250 and 0.500 from the reference plane.

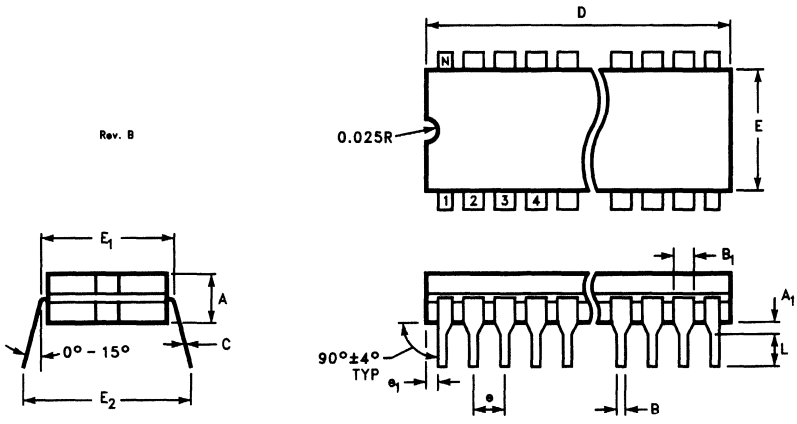
MDP0004 Rev. C
8-Lead TO-99 Metal Can Package

Lead Finish (Coml)—Tin Plate
Lead Finish (Mil)—Gold or Hot Solder DIP



MDP0009 Rev. A
10-Lead TO-5 Metal Can Package

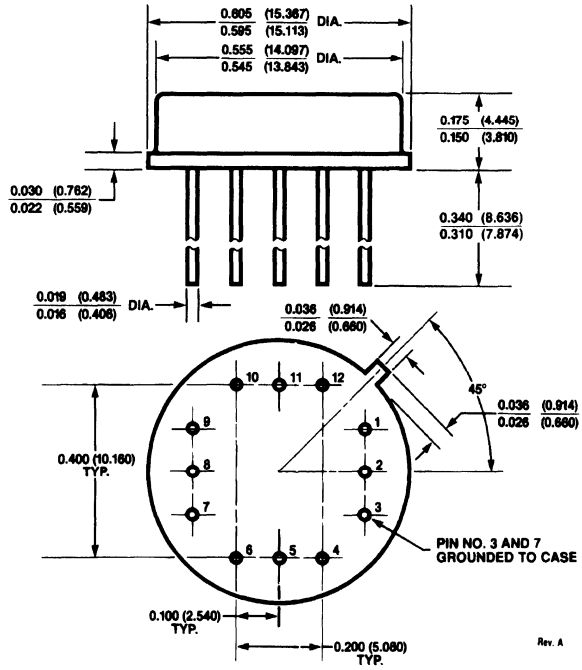
Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Gold or Hot Solder DIP



MDP0016 Rev. B
CerDIP Package
Lead Finish (Coml)—Tin Plate or Hot Solder DIP
Lead Finish(Mil)—Hot Solder DIP

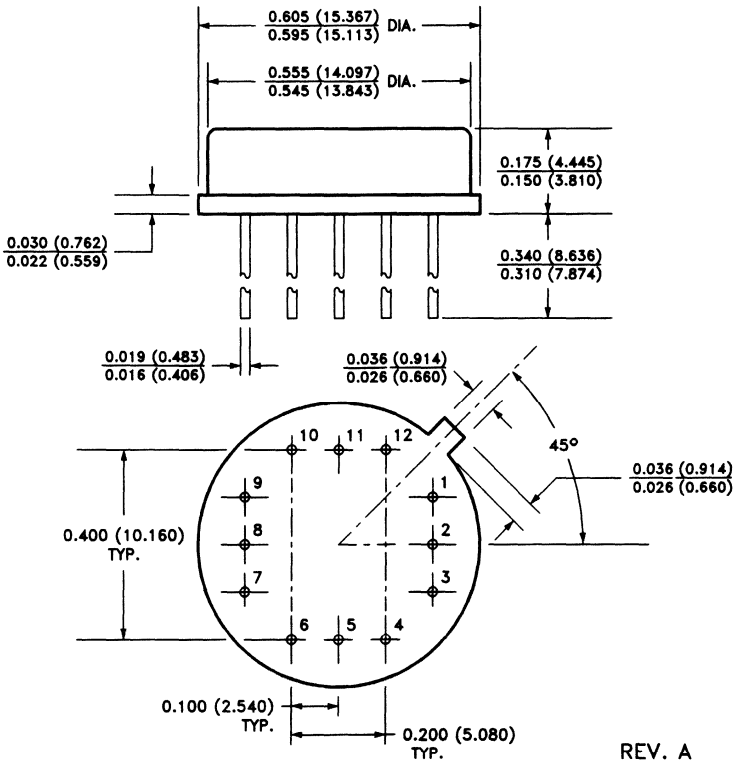
Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A	.140	.160	.140	.160	.140	.160	.140	.160
A_1	.115	.055	.020	.050	.015	.060	.020	.050
B	.016	.023	.016	.021	.014	.026	.016	.021
B_1	.050	.065	.050	.060	.038	.068	.050	.060
C	.008	.012	.008	.012	.008	.018	.008	.012
D	.375	.395	.760	.785	.940	.960	1040.925	1.060
E	.245	.265	.220	.291	.220	.310	.2780	.298
E_1	.300	.320	.300	.320	.290	.320	.300	.320
E_2	.340	.390	.340	.390	.360	.410	.340	.390
e	.090	.110	.090	.110	.090	.110	.090	.110
e_1	.020	.055	.078	.098	.068	.098	.078	.098
L	.125	.150	.125	.150	.125	.150	.130	.150
N	8-Lead		14-Lead		18-Lead		20-Lead	

Package Outlines



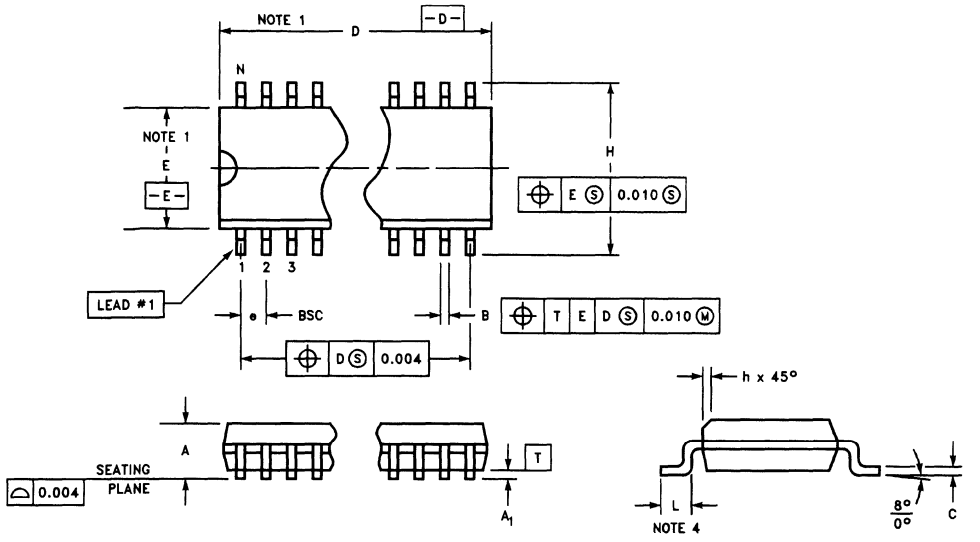
MDP0019 Rev. A
12-Lead TO-8 Metal Can Package
Pins 3 and 7 Grounded to Case

Lead Finish (Coml)—Gold or Hot Solder DIP
Lead Finish (Mil)—Gold or Hot Solder DIP



MDP0026 Rev. A
12-Lead TO-8 Metal Can-Short Lead
Commercial—Gold or Hot Solder DIP

Package Outlines

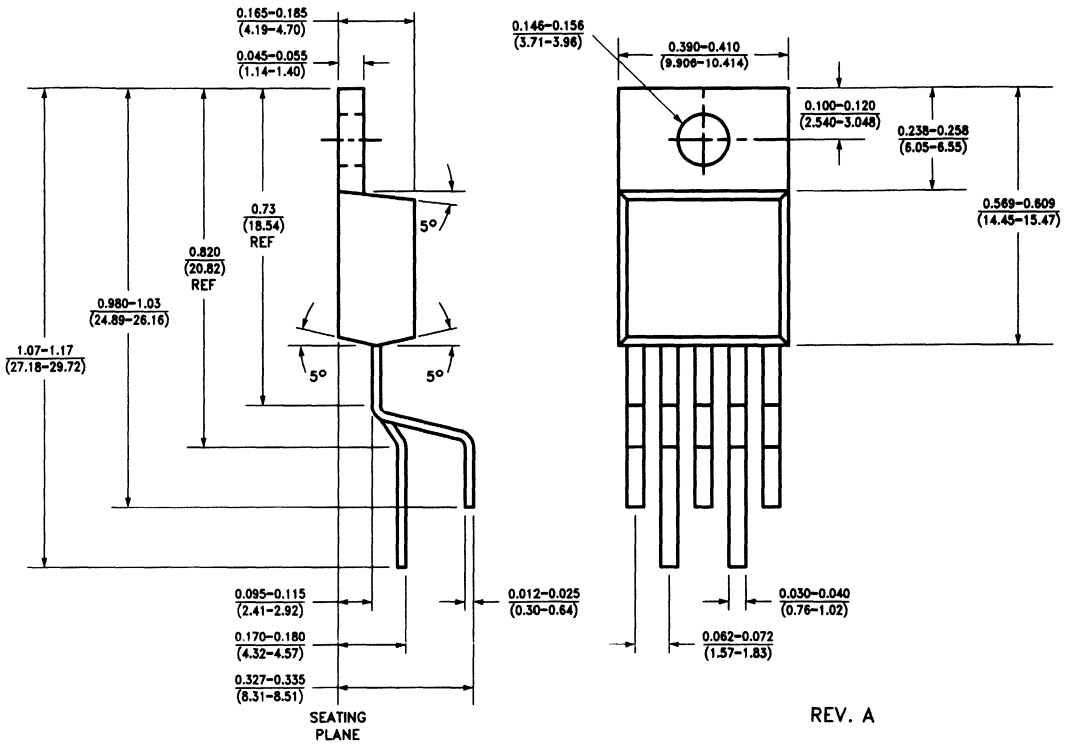


REV. C

Note 1: These dimensions do not include mold flash or protrusions. Mold flash protrusion shall not exceed .006" on any side.
Note 2: 8 and 14 leads are narrow body.
Note 3: Dimensions and tolerancing per ANSI Y14.5M-1982.
Note 4: Flat area of lead foot.
Note 5: SOL-24T2 (thermal package) has 2 fused leads on each side of package.

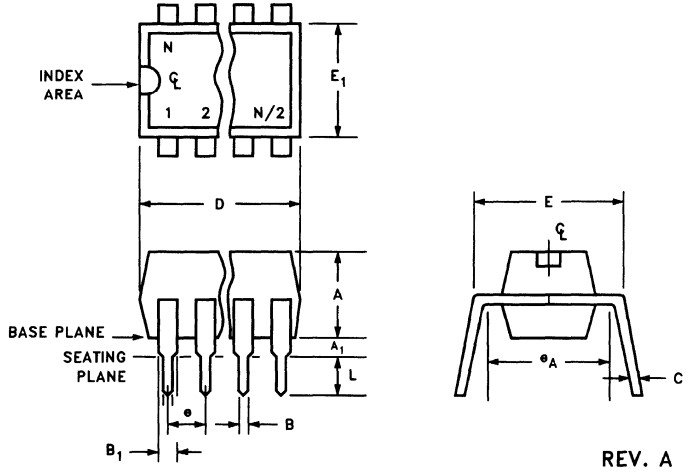
MDP0027 Rev. C
Package Outline—SOIC
Lead Finish—Solder Plate

Symbol	Lead Count													
	SOL-28		SOL-20		SOL-16		SO-16		SO-14		SO-8		SOL-24	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.096	0.104	0.096	0.104	0.096	0.104	0.061	0.068	0.061	0.068	0.061	0.068	0.096	0.104
A_1	0.004	0.011	0.004	0.011	0.004	0.011	0.004	0.010	0.004	0.010	0.004	0.010	0.004	0.011
B	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019	0.014	0.019
C	0.009	0.012	0.009	0.012	0.009	0.012	0.008	0.010	0.008	0.010	0.008	0.010	0.009	0.012
D	0.696	0.712	0.498	0.510	0.397	0.430	0.386	0.394	0.337	0.344	0.189	0.196	0.598	0.614
E	0.291	0.299	0.291	0.299	0.291	0.299	0.150	0.157	0.150	0.157	0.150	0.157	0.291	0.299
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC	
H	0.398	0.414	0.398	0.414	0.398	0.414	0.230	0.244	0.230	0.244	0.230	0.244	0.398	0.414
h	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016	0.010	0.016
L	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024	0.016	0.024



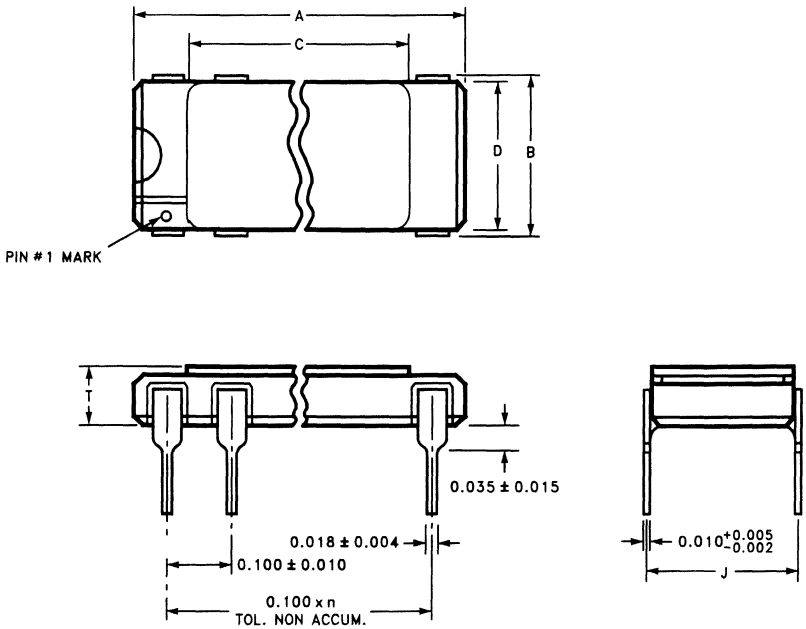
MDP0028 Rev. A
5-Lead TO-220
Lead Finish—Solder Plate

Package Outlines



MDP0031 Rev. A
Plastic Package
Lead Finish—Hot Solder DIP

Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A_1	0.020	0.040	0.020	0.040	0.020	0.040	0.020	0.040
A	0.125	0.145	0.125	0.145	0.125	0.145	0.125	0.145
B	0.016	0.020	0.016	0.020	0.016	0.020	0.015	0.021
B_1	0.050	0.070	0.050	0.070	0.050	0.070	0.050	0.070
C	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
D	0.350	0.385	0.750	0.770	0.745	0.755	0.925	1.045
E	0.290	0.310	0.300	0.320	0.300	0.325	0.300	0.320
E_1	0.245	0.255	0.245	0.255	0.245	0.255	0.245	0.255
e	0.100 Typ		0.100 Typ		0.100 Typ		0.100 Typ	
e_A	0.300 Ref		0.300 Ref		0.300 Ref		0.300 Ref	
L	0.130	0.150	0.115	0.150	0.125	0.150	0.130	0.150
N	8		14		16		20	



NOTE:
ALL DIMENSIONS ARE IN INCHES.

MDP0033
Side Brazed DIP Package
Lead Finish—Lead Tin Solder Plate

	8 Leads		14 Leads		16 Leads		20 Leads	
Common Dimensions	Min	Max	Min	Max	Min	Max	Min	Max
A	—	0.527	—	0.760	—	0.840	—	1.020
B	0.300	0.320	0.300	0.320	0.300	0.320	0.300	0.320
C	0.466	0.480	0.466	0.480	0.466	0.480	0.466	0.480
D	0.285	0.305	0.285	0.305	0.285	0.305	0.285	0.305
J	0.290	0.310	0.290	0.310	0.290	0.310	0.290	0.310
T	—	0.125	—	0.125	—	0.125	—	0.125
N	3		6		7		9	

Ordering Information

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

In North America, Elantec has three levels of sales support. Regional Sales Managers are located in the Boston and San Jose areas. Field Applications Engineers are located in the Boston and San Jose offices. Elantec also maintains a network of sales representatives covering the United States and Canada. Finally, major nationwide and regional distributors provide local stock. Elantec maintains an up-to-date distributor inventory status and provides an inventory referral service through Distribution Sales in San Jose. Orders may be placed through the sales representatives or distributors. A list of sales representatives and distributors is included with this Elantec 1994 Databook, or please contact any of the regional sales offices.

In Europe, Elantec has a Regional Sales Office in London. Local sales support is provided through stocking representatives in all of the major countries. A current list of representatives and distributors may be obtained from the London office.

Elantec has stocking agents in all Pacific Rim Countries, Australia, and New Zealand. A list may be obtained from Elantec's headquarters in Milpitas, California.

In Asia, Elantec has a regional sales office in Tokyo. Local sales support is provided through stocking representatives in all of the major countries. A current list of representatives may be obtained by contacting the Tokyo sales office.

Elantec Proprietary and NSC Alternate Source

E L 2006 A G /883B

PREFIX
ELANTEC

FAMILY
LH NSC Alternate Source
L Proprietary Linear
P PNP Array
N NPN Array

PART NUMBER

OPTIONAL SUFFIX
A Selected Electrical Performance
C −0°C to +75°C or −40°C to +85°C
E −40°C to +150°C
None −55°C to +125°C

PACKAGE
B Sidebraze
G TO-8 Metal Can
H TO-5 or TO-99 Metal Can
J CerDIP
K TO-3
N Plastic DIP
T TO-220
M Large Body SOIC
S Narrow Body SOIC

RELIABILITY PROGRAM
/883B 100% MIL-STD-883 Class B, Current Revision Processing

Applications Assistance / Sample Ordering Information

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Making Applications and Sample Requests Easier

Elantec's Policy

Elantec receives many applications inquiries every day which vary widely in nature. We believe that Application assistance is as inherently important to our customers as the performance and quality of our products. To assist our customers in getting the best and fastest support possible, the following information is provided.

Sample and Literature Requests

If you know what product sample or literature you need, probably the best and fastest way to obtain them is to call Elantec's local sales office, sales representative, or distributor. A complete listing is on pages 19-3 through 19-14 of this book. If you are not sure what you need, call our Applications hot line 1 (800) 333-6314. For literature only, touch or request extension 234. For applications assistance, touch or request extension 311.

New Applications Assistance

Technical assistance for a new application is a toll free phone call away. Call 1 (800) 333-6314 and touch or request extension 311. Probably the most important information that Elantec needs to assist you is a clear picture of what the circuit needs to do. What we mean by that is the cost and performance objectives of the circuit or system. If you have a preliminary topology or schematic, feel free to FAX that to the Factory at 1 (408) 945-9305 in confidence. The following is a check list which will expedite our assistance to you:

What does the circuit need to do?

What power supply voltages are available?

What is the temperature range?

What is the load?

What are the key specs: bandwidth, slew rate, settling time, noise, output voltage, etc. and what are your expectations?

Problems with an Existing Circuit and Other Issues

Applications assistance for an existing application is a toll free phone call away. Call 1 (800) 333-6314 and touch or request extension 311. Probably the most important information that Elantec needs to assist you is a clear picture of what the circuit is doing or not doing. The following is a check list which will expedite our assistance to you:

What is the part number?

What is the device's date code?

What are the symptoms?

Are scope photos or frequency plots available?

How many devices are involved?

Unreleased Product

As a general rule, Elantec does not sample new devices that have not completed our rigorous formal release cycle. However, occasionally we will "beta " site customers with advanced Engineering samples. We view this as a productive exchange between our Factory and customer Engineering teams to pin point problems and issues. In all instances, these devices will be marked "Engineering Sample." If you are interested in such a device, call your nearest Elantec sales office, local sales representative, or the Factory at 1 (800) 333-6314 and touch or request extension 252.

Demo Boards

Contact factory applications for demo board availability.

Quality or Reliability Issues

On the rare occasion that you experience what may be a Reliability or Quality issue, please contact the nearest Elantec sales office, local sales representative, or distributor. You may choose to call the Factory directly at 1 (800) 333-6314, and touch or request extension 310 or 279.

Price Quotes/Delivery Status

For pricing and delivery information, please contact the appropriate full service representative or local Elantec franchised distributor as listed on page 19-6. For additional information you may contact the Elantec Customer Service Department @ 1 (800) 333-6314.

Quality and Military Programs

élantec

HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Forward

This document summarizes Elantec's philosophy and policies towards Quality Assurance and Reliability for both MIL-STD-883 and commercial products. It is intended as an overview only, to give the reader a quick visualization of Elantec's capabilities and standard procedures. Elantec's quality system is structured on *MIL-I-45208.

Customers wishing more detail should refer to either "QRA-3, Elantec's 883B program for Hybrid Integrated Circuits", or contact us at the factory. Also available are "QRA-4 Hybrid S-Flow" and "QRA-5 Monolithic Class S Flow". Our facilities and process documentation are available for customer inspection at any time. We welcome you to visit us at your earliest convenience, as we believe our factory to be "our best salesman".

Philosophy

Elantec was founded on the principle of supplying Analog Integrated Circuits of advanced performance with quality levels beyond that normally available from the semiconductor industry. Our product range has been intentionally limited to service commercial, industrial and Military/Areospace applications only. It is our firm belief that by placing quality and reliability over all other objectives, we will achieve our goal of providing our customers maximum cost-effectiveness and long term satisfaction.

Using both monolithic and hybrid technologies, Elantec provides leading edge Analog Integrated Circuit devices whose performance routinely exceeds that of most commercial manufacturers.

It is our policy to insure that each and every device is:

1) Designed to provide maximum long-term reliability.
2) Manufactured in strict compliance with thoroughly documented procedures in a tightly controlled environment.
3) Tested to insure that every device meets each parameter specified on the data sheet or customer specification.
4) Covered by a rigorous regularly scheduled Quality and Reliability Audit Program.

Commercial/Industrial Program Summary

Elantec:

- Provides the most thoroughly tested product available.
- Specifies clearly on each data sheet exactly which parameters are 100% tested, Q.A. sampled, or guaranteed by design and characterization.
- Performs 100% A.C. testing of critical performance parameters (see individual data sheets).
- Operates to extremely tight AQL sampling plans (see Table I).
- Provides 100% Temperature Cycling, Centrifuge, Fine and Gross Leak checks on all hermetic package commercial devices (see Table II).
- Uses superior manufacturing processes for microcircuit devices to eliminate failure modes inherent in conventional assembly techniques.
- Maintains traceability on production lots.
- Manufactures thick film substrates and performs final electrical testing of commercial devices 100% in our Milpitas, California facility.

Military/Aerospace Program Summary

Elantec:

- Provides product screened and quality performance tested in accordance with MIL-STD-883.
- Is an approved supplier to DESC/SMD drawing numbers:

  78013—similar to ELH0002H/883B
  80013—similar to ELH0032G/883B
  80014—similar to ELH0033G/883B
  85087—similar to ELH0041G/883B
  85088—similar to ELH00021K/883B
  85089—similar to ELH0101K/883B or ELH0101AK/883B

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Summary of Elantec's Reliability and Quality Assurance Policy and Procedures QRA-1

- Maintains an on-going product qualification and reliability monitor program. Current quality conformance data is always available to support military product.
- Manufactures MIL-STD-883 Hybrid products 100% in the United States in our facility in Milpitas, California.
- Specifies clearly on each data sheet exactly which parameters are 100% tested, Q.A. sampled, or guaranteed by design and characterization.
- Performs 100% A.C. testing of critical performance parameters (see individual data sheets).
- Operates to extremely tight AQL sampling plans (see Table I).
- Facilities have been surveyed and approved by major military/aerospace customers—names available upon request.
- Maintains complete traceabilty and manufacturing history on each production lot.
- Has been audited, certified, and qualified by DESC to MIL-STD-1772.
- Maintains shelf stock of MIL-STD-883 product for rapid delivery at competitive prices.
- Welcomes customer Source Control Drawings, special selections and custom reliability processing.

Facility

All military hybrid product manufactured by Elantec is completely built in the U.S.A. at our factory in Milpitas, California, all testing is performed in Milpitas. Commercial product thick film processing and all electrical testing is done in Milpitas. Commercial assembly may be done either in Milpitas or offshore.

The Milpitas factory has been certified by many customers to meet the requirements of MIL-I-45208. Defense Electronics Supply Center (DESC) has performed an audit and certified Elantec to the Hybrid Line Certification Specification, MIL-STD-1772.

The factory has 46,000 square feet of space. 10,000 square feet is a Class 1000 clean room (Fed. Std 209) where assembly and electrical test are performed. All assembly operations are done under Class 100 laminar flow hoods. Temperature and humidity are monitored and controlled in accordance with MIL-STD-883. Gases are filtered at point of use. De-ionized water is filtered and bacteria controlled, and resistivity is continuously monitored. All semiconductor work-in-process is stored in nitrogen-purged dessicators.

A comprehensive ESD program is in effect. All work surfaces are either stainless steel or conductive laminate. Every work surface is grounded for Electrostatic Discharge protection in accordance with OSHA requirements. Shelving at all inventory locations is grounded. Floors in all manufacturing and inventory areas are covered with conductive tile attached with conductive tile cement. Conductive heel straps are worn by all operators. All product, commercial and military, is marked with an equalateral triangle to indicate static sensitivity in accordance with MIL-I-38535 and MIL-H-38534. Finished product is packaged in anti-static materials which are completely shielded by aluminum-lined boxes or conductive bags.

Elantec maintains complete *in-house* capability to 100% process devices to the requirements of MIL-STD-883 Class B. Additional in-house capability includes Particle Impact Noise Detection (PIND). All testing for initial product qualification and periodic quality conformance is performed in-house except for moisture resistance, internal water vapor, mechanical shock and vibration which are performed at DESC certified laboratories.

All manufacturing equipment is calibrated in accordance with MIL-STD-45662 as modified by MIL-I-38535 and MIL-H-38534.

Elantec maintains a complete Program Plan. The plan is available for review by customers at Elantec. Included within the Program Plan is a complete equipment and facilities list.

Quality System

All quality assurance functions at Elantec report to the President and are totally independent of the manufacturing organization. These functions include Incoming Quality Control, In-Process Quality Control, Product Qualification, Quality Conformance, Document Control, Customer Specification Review, Internal Quality Audit, and Failure Analysis.

Elantec's operation is controlled by a thorough documentation system. Peripheral support systems such as document control, calibration, customer specification review, the ESD program, and archives are fully documented as to procedure and responsibility. All manufacturing operations have specifications describing the equipment operation and procedures. Product manufacturing flow charts define precise operational sequences to insure each lot is built in conformance to Elantec and Military requirements. All raw materials are purchased to Elantec Procurement Documents. Military package materials and finishes are in accordance with MIL-I-38535 and MIL-H-38534.

Raw materials are inspected to rigorous requirements by Incoming Quality Control prior to release for manufacture. Minimum inspections for hybrid military products are those specified in MIL-STD-883 Method 5008 for Element Evaluation. Many of these tests are performed more often than required by the military standards. In addition, various other tests are performed to insure the integrity of each raw material. Similar tests are performed on raw materials destined for commercial products.

Travelers used throughout Elantec are structured to maintain traceability of raw materials and operators to each manufacturing lot. Lots are shipped with accurate lot numbers on the containers to provide backward traceability should this ever be required.

In-line Quality Control gates monitor the process to insure critical manufacturing operations are under control. These include wire bond pull, die shear, die and preseal visual inspection, mark permanency, and electrical test.

Before release of any Elantec product, an exhaustive product qualification is performed. This includes life testing on multiple lots and various mechanical package tests. On-going Reliability Monitor testing is done on all Commercial product and package families. The reliability monitors include electrical and mechanical test as described in QAP0073 Military products subsequently receive complete Group A, B, C, and D per MIL-STD-883 testing prior to shipment of the first part. Military Quality Conformance testing is done in compliance with Method 5005 or Method 5008.

In Conclusion

It has been and continues to be Elantec's goal to provide product of the highest quality available. We believe the extra effort we have expended in the design, construction techniques, testing and quality control procedures results in a product which is observably superior in performance, consistently higher in quality, and provides greater reliability in the actual application. We also believe such product will provide the overall lowest cost and greatest long term satisfaction to the customer.

*Note: Elantec does not accept customer or government supplied equipment or materials.

Summary of Elantec's Reliability and Quality Assurance Policy and Procedures QRA-1

Table I. QA Inspection Sampling Plan

Die Visual:	0.25% AQL			
Precap Visual:	0.25% Military, 1.5% Commercial			
Mark Permanency:	4 Parts/Day/Package			
Electrical Test (All Products):				
Non-Military Lots	**LTPD (%)**	**Sample Size**	**Accept No.**	**Equiv. AQL(%)**
Computer Tests at Room Temp	2	116	0	0.04
Computer Tests Hot	3	76	0	0.07
Computer Tests Cold	5	45	0	0.11
A.C. Bench Tests at Room Temp	2	116	0	0.04
Military Lots				
Computer Tests at Room Temp		116	0	0.04
Computer Tests Hot		116	0	0.04
Computer Tests Cold		116	0	0.04
A.C. Bench Tests at Room Temp		116	0	0.04

Note 1: Computer tests are all D.C. tests plus A.C. on those products where A.C. can be tested on the enhanced LTX automatic tester.

Note 2: All military lots are Q.A. sampled at all temperatures.

Note 3: All non-military lots (E+, Prime, Commercial) are Q.A. sampled at room temperature (D.C.) Until adequate history is developed on these new products, each lot is sample tested at temperatures and on the bench. Non-military lots of mature products with adequate history are skip lot tested at temperatures or on the bench, e.g., they are Q.C. sampled every fourth or fifth lot. (This frequency may change with time as more product history is developed.)

Note 4: If a device which is in skip lot mode should suffer a lot failure, every lot is then tested until three lots in succession are passed before returning to skip lot mode.

Table II. Elantec Hybrid Metal Can Process Flow Summary

Operation	Commercial	Prime(1)	/883B(2)
Incoming QC			
Die Evaluation	X	X	X
Package Evaluation	X	X	X
Raw Material Evaluation	X	X	X
Assembly			
Wire Bond Pull QC	X	X	X
Die Shear QC	X	X	X
Internal Visual	X	X	X
Seal	X	X	X
Stabilization Bake	2 Hours	2 Hours	24 Hours
Temperature Cycling	5 Cycles	5 Cycles	10 Cycles
Constant Accel.			
TO-3, LCC (5KG)	X	X	X
TO-5 (30KG)	X	X	X
TO-8 (20KG)	X	X	30KG
Fine Leak			
TO-3 ($2x10^7$ cc/sec)	X	X	X
TO-5 ($5x10^8$ cc/sec)	X	X	X
TO-8, LCC ($5x10^8$ cc/sec)	X	X	X
Gross Leak			
With Pressurization			X
No Pressurization	X	X	
Class Test		X	X
Burn-in			160 Hours
Electrical Test 25°C(3)	X	X	X
Q.C. 25°C(3)	X	X	X
Electrical Test Cold(3)		X	X
Q.C. Cold(3)	X	X	X
Electrical Test Hot(3)		X	X
Q.C. Hot(3)	X	X	X
External Visual	X	X	X
Group B, C, D Testing			X

Note 1: A prime part is a commercial part tested over the range of −55°C to +125°C.

Note 2: For complete details of Elantec's "/883B" military program see "QRA-3, Elantec's 883B Program for Hybrid Integrated Circuits."

Note 3: Electrical tests performed are as documented on the individual device data sheet.

Summary of Elantec's Reliability and Quality Assurance Policy and Procedures QRA-1

Table III. Elantec Monolithic Process Flow Summary

Operation	Commercial	Prime(1)
Incoming QC		
Package Evaluation	X	X
Raw Material Evaluation	X	X
Assembly		
Wire Bond Pull QC	X	X
Die Shear QC	X	X
Internal Visual	X	X
Seal	X	X
Temperature Cycling	5 Cycles	5 Cycles
Constant Accel. (30KG)(3)	X	X
Fine Leak ($5x10^8$ cc/sec)(3)	X	X
Gross Leak(3)		
With Pressurization		
No Pressurization	X	
Class Test		X
Burn-in		
Electrical Test 25°C(5)	X	X
Q.C. 25°C(5)	X	X
Electrical Test Cold(5)		X
Q.C. Cold(5)	X	X
Electrical Test Hot(5)		X
Q.C. Hot(5)	X	X
External Visual	X	X
Group B, C, D Testing		

Note 1: A prime part is a commercial part tested over the range of −55°C to +125°C.

Note 2: For complete details of Elantec's "/883B" military program, see "QRA-2, Elantec's Military Processing-Monolithic Integrated Circuits."

Note 3: Applies to all packages except plastic packages.

Note 4: Military burn-in may be either 150°C for 80 hours or 125°C for 160 hours.

Note 5: Electrical tests performed are as documented on the individual device data sheet.

Elantec manufactures a standard family of hybrid circuits for military applications in accordance with MIL-M-38534 and MIL-STD-883. Testing is performed to Class B. All manufacturing is done on Elantec's MIL-STD-1772 Certified Line. Specifics of this program are outlined herein. Parenthetical references utilized in this document indicate applicable Elantec internal specifications.

I. CONTROL SYSTEMS

1.0 Certified Line

1.1 Elantec's factory located at 1996 Tarob Ct., Milpitas, Ca. is certified and qualified by the Defense Electronics Supply Center (DESC) to the requirements of MIL-STD-1772 (Certification Requirements for Hybrid Microcircuit Facilities and Lines). All Elantec Military Hybrid Products are manufactured at this facility and under the controls of MIL-STD-1772.

2.0 Quality Organization

2.1 The Quality Organization at Elantec reports to the President of the corporation. All quality functions are independent of the manufacturing organization.

2.2 Functions under the Quality Organization's control include:

Incoming Inspection
In-Process Quality Control
Internal Audit
Qualification Testing
Quality Conformance Testing
Document Control
Failure Analysis
Material Returns

3.0 Facility (QAP0030)

3.1 Method 5008 requires that hybrid assembly be performed under Class 100,000 conditions per Fed. Std. No. 209. Elantec assembly and test are performed in a Class 1000 clean room. In addition, all assembly operations from die visual inspection through precap visual are performed under Class 100 laminar flow hoods. The area and hoods are routinely monitored per Fed. Std. No. 209. Temperature and humidity are monitored and controlled in accordance with MIL-STD-883.

3.2 Gases are filtered at point of use.

3.3 De-ionized water is filtered and bacteria controlled and resistivity is continuously monitored.

3.4 All semiconductor work-in-process is stored in nitrogen purged desiccators.

4.0 ESD (QAP0016)

4.1 All work surfaces are either stainless steel or conductive laminate. Every work surface is grounded for Electrostatic Discharge protection in accordance with OSHA requirements.

4.2 Shelving at all inventory locations is grounded.

4.3 Floors in all manufacturing and inventory areas are covered with conductive tile attached with conductive tile cement.

4.4 All operators wear conductive heel straps.

4.5 All product is marked with an equilateral triangle to indicate static sensitivity in accordance with MIL-M-38534.

4.6 Finished product is packaged in anti-static materials which are completely shielded by aluminum-lined boxes.

5.0 Calibration (QAP0003)

5.1 All manufacturing equipment is calibrated in accordance with MIL-STD-45662 as modified by Appendix A paragraph 30.1.2.5 of MIL-M-38534.

6.0 Inspection Systems

6.1 Inspection System Requirements are in accordance with MIL-I-45208.

7.0 Program Plan (QAP0039)

7.1 Elantec maintains a complete Program Plan in accordance with MIL-H-38534. The plan is available for review by customers at Elantec.

7.2 Included within the Program Plan is a complete equipment and facilities list.

8.0 Failure Analysis (QCX0010)

8.1 Elantec has in-house capabilities to perform failure analysis in accordance with MIL-STD-883 Method 5003 Condition A.

II. MANUFACTURING

1.0 Location

1.1 All Elantec thick film work, assembly, electrical test, and 100% environmental testing is performed at Elantec owned facilities located in the United States. Moisture resistance and internal water vapor testing are performed at DESC certified laboratories.

2.0 Incoming Inspection (QAP0006)

2.1 All raw materials used in the manufacture of Elantec hybrids are specified by procurement documents. They are inspected by the Incoming Inspection Department prior to release for manufacture. Minimum inspections are those specified by Method 5008 of MIL-STD-883 for Element Evaluation. Many tests are performed more often than required by 5008. In addition, various other tests are performed to insure the integrity of the raw materials.

3.0 Materials

3.1 All package materials and finishes are in accordance with MIL-H-38534.

4.0 Seal

4.1 Prior to package seal on metal can packages, each device is baked in a vacuum oven which is connected to the welder dry box. The seal is performed in a nitrogen purged dry box which is continuously monitored for moisture content.

5.0 Screening (QAP0052)

5.1 Screening is performed in accordance with Method 5008 of MIL-STD-883. A summary of the screening operations is shown in Table I.

5.2 Burn-in is done for 160 hours at 125°C. Post-burn-in electrical testing is done with 96 hours of removal of bias. PDA is 10%. Cool-down is performed under bias.

5.3 Electrical test limits, conditions, temperatures, and burn-in circuits are as specified in the appropriate Elantec data sheet. Elantec data sheets show their current revision letter and are fully controlled documents. The latest revision of any data sheet is available from Elantec Specification Control. All 100% test operations are guardbanded, i.e., tested to limits tighter than required by the specification to provide margin for test system variations with time and between machines.

6.0 Marking (MPX0047)

6.1 All devices are marked with the Elantec part number, Elantec logo, 5 character date code indicating year and week of seal, and the lot within the week of seal, ESD equilateral triangle, and USA for country of origin.

III. QUALITY

1.0 Process Quality Control

1.1 Die visual and precap visual are Q.C. sampled to a 0.25% AQL. (QCX0004, QCX0005)

1.2 Wire bond pull testing, both destructive and non-destructive, are performed to limits and with the frequency specified by Method 5008 of MIL-STD-883. (QCX0001)

1.3 Production lots are sample die shear tested during assembly in addition to the testing required by Group B. (QCX0003)

2.0 Qualification (QAP0038)

2.1 Each Elantec device is tested to the requirements of MIL-H-38534. Elantec Quality and Reliability Assurance performs the function of Qualifying Activity per paragraph 1.2.1 of MIL-STD-883.

3.0 Quality Conformance (QAP0038)

3.1 Group A testing is performed in-line, after each temperature screening test. See Table I. (QCX0002).

3.2 Group B testing is performed per Method 5008 on every inspection lot for each package type, lead finish and assembly technique. See Table II.

III. QUALITY — Contd.

3.3 Group C testing is performed more frequently than required by MIL-M-38534 4.6.2.2.3, which requires it to be done only once in the life of the product for Class B. Elantec performs Group C at least every 26 weeks of seal date code by microcircuit group. Life test endpoint electrical testing is to limits and conditions as specified in the Elantec data sheet and is done at three temperatures within 96 hours of removal of bias. See Table III.

3.4 Group D is performed as required by Method 5008. Testing is done at least once per 6 month period for each package type. See Table IV.

3.5 All 883B products are fully qualified by Groups, A, B, C, and D Quality Conformance inspections prior to shipment.

IV. PROCESS CHANGES (QAP0002)

1.0 Elantec maintains a fully documented change control system. All manufacturing changes, including those specified by MIL-M-38534, must be submitted to and approved by Elantec Engineering and Quality and Reliability Assurance prior to implementation. Additionally, Elantec utilizes multiple sources for semiconductor die to insure availability. Each die type from each vendor is fully qualified for form, fit and function as well as reliability. Internal documentation completely specifies each manufacturing alternative. Elantec Quality and Reliability Assurance submits reports to the "Qualifying Activity" for changes of qualified product as per MIL-H-38534

V. SPECIFICATION COMPLIANCE

1.0 Elantec hybrid military products shipped are manufactured in strict compliance with MIL-H-38534 and MIL-STD-883 with no exceptions or deviations.

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Table I. Device Screening

Operation	883 Method	Conditions
Incoming Q.C.	5008 Element Evaluation	
Assembly		
Wire Bond Pull	5008, 2011	
	5008, 2023	
Die Shear Strength	2019	
Internal Visual	2017 Class B	
Seal		
Stabilization Bake	1008C	
Temperature Cycling	1010C	
Constant Acceleration	2001A	(TO-3, LCC)
	2001E	(TO-5, TO-8)
Fine Leak	1014 A1	(TO-3 Limit = 2×10^7 cc/sec)
		(TO-5 Limit = 5×10^8 cc/sec)
		(TO-8 Limit = 5×10^8 cc/sec)
Gross Leak	1014 C1	
Class Test		
Mark	Note 1	
Burn-In	1015	125°C, 160 Hours
Electrical Test		25°C, Elantec Data Sheet (Guardbanded), 96 Hour Window, PDA = 10%
Q.C. (Group A)	5008	25°C, Elantec Data Sheet
Electrical Test		Cold, Elantec Data Sheet (Guardbanded)
Q.C. (Group A)	5008	Cold, Elantec Data Sheet
Electrical Test		Hot, Elantec Data Sheet (Guardbanded)
Q.C. (Group A)	5008	Hot, Elantec Data Sheet
External Visual	2009	
Group B, C, D Hold	5008	Verify Group B, C, and D Data

Note 1: May be performed in any sequence prior to Group B testing.

Table II. Group B Test Outline

Subgroup	Test	883 Method	Sample Size	Acc. No.
1	Physical Dimensions	2016	2 Devices	0
3	Resistance to Solvents	2015	4 Devices	0
4	Internal Vis. and Mech.	2014	1 Device	0
5	Bond Strength	2011	2 Devices, 11 Wires Ea. Min.	0
6	Die Shear	2019	2 Devices Min.; 22 Internal Elements	0
7	Solderability	2003	1 Device, 15 Leads Min.	0
8	Seal—Fine Leak Gross Leak	1014A1 1014C1	15 Devices	0

Table III. Group C Test Outline

Subgroup	Test	883 Method	Sample Size	Acc. No.
1	External Visual Temperature Cycling Constant Acceleration Fine Leak Gross Leak Visual End Point Electricals	2009 1010C 2001 1014A1 1014C1 1010 Subgroups 1, 2 and 3	15 Devices	0
2	Pre-Life Electricals Steady State Life Test End Point Electricals	 1005 Subgroups 1, 2 and 3	22 Devices	0
3	Internal Water Vapor	1018	3 Devices or 5 Devices	0 1

Table IV. Group D Test Outline

Test	883 Method	Sample Size	Acc. No.
Thermal Shock	1011C	5 Devices	0
Stabilization Bake	1008 (1 Hr.)	5 Devices	0
Lead Integrity	2004B2 or D	1 Device	0
Seal	1014A1 1014C1	5 Devices	0

1.0 Purpose

1.1 To define Elantec's standard Class S Minus process flow for Hybrid products. This flow meets or exceeds all the requirements of MIL-H-38534 for Class B Hybrids but is not fully compliant with the Class S requirements.

2.0 Scope

2.1 This specification applies to Hybrid products processed to Elantec's standard Class S Minus flow.

3.0 Associated Specifications

3.1 Documents specified herein, of the issue in effect on the date of processing, form a part of this drawing to the extent specified herein.

3.2 MIL-STD-883 Test Methods and Procedures for Microelectronics

3.3 MIL-H-38534 General Military Specification for Hybrid Microcircuits

4.0 Procedure

4.1 Microcircuit and semiconductor dice evaluation requirements shall be per MIL-STD-883, Method 5008, *Class B*.

4.2 Package evaluation shall be per MIL-STD-883, Method 5008, *Class B*.

4.3 In process controls shall be per MIL-STD-883, Method 5008, *Class B*.

4.4 Device screening shall be as specified in Table I herein.

4.5 Qualification/Quality Conformance evaluation shall be performed when specified on the purchase order and shall be per MIL-STD-883 Method 5008, Class S, Groups B, C and D.

4.6 All screening and Quality Conformance testing shall be controlled by an Elantec Custom Process Instruction (CPI).

4.7 If specified on the Purchase Order, data to be shipped shall include: (Otherwise data will be kept on file per MIL-H-38534).

4.7.1 C of C

4.7.2 Pre and Post Burn-in variables. Delta data (if applicable).

4.7.3. Attributes data for Table I Screening.

4.7.4 X-ray Report

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Class S Minus Hybrid Flow QRA-4

Table I. Class S Minus Hybrid Device Flow USA Build

Assembly

Standard MIL Assembly: With the following additional requirements:

1) Wafer Traceability:
2) Piece part traceability and control:
3) Die attach and lead bond monitor every 2 hours plus other standard requirements/shift change, operator change, spool change, machine down, etc.
4) 100% bond pull per MIL-STD-883, Method 2023 with a 2% PDA (MIL-H-38534 4.5.4).
5) 100% Internal Visual per MIL-STD-883, Method 2017 Condition A.
6) QA Internal Visual per MIL-H-38534 4.1.2.3 Sample Size 22 accept # = 0.
7) QC DPA Req'd @ Pre Seal

PRODUCT SCREENING per MIL-STD-883	Method 5008
	|
	Stabilization Bake
	|
	Temp. Cycle
	|
	Constant Acceleration
	|
25% PDA on a max of 5 Passes	PIND Condition A
	|
Elantec imposed electrical screen	25°C
	|
	−55°C
	|
	125°C
	|
	Serialization (serial # and Date code is the device ID)
	|
	XRay
	|
Test read/record if delta's are req'd	25°C electrical Read and Record
	|
Burn/in board 100% socket check *Junction temp max 175°C	Burn-in 160 hours *125°C
	|
	Failure analysis of burn-in screen failure
	|
96 hour test window	25°C electrical test Go-no-go
	|
Burn/in board 100% socket check	Burn-in 160 Hours *125°C
	|

96 hour test window	25°C electrical Group A Subgroup 1 parameters Read and Record
	|
Pre Read/Record to post Read/Record	Compute delta's if required
	|
	PDA check 2% Group A subgroup 1 & delta parameters PDA is Base on the # of failures from the 2nd 160 hours of burn-in (F/A required on all functional failures)
	|
	QA sample 25°C
	|
	−55°C electrical Go-no-go
	|
	QA sample −55°
	|
	125°C electrical Go-no-go
	|
	QA sample 125°C
	|
	100% AC tests if applicable
	|
	QA sample AC tests
	|
	Mark (remark serial # − if necesray to keep serial # ID)
	|
	Solder DIP (if applicable)
	|
	25°C electrical test
	|
	Fine/Gross leak 100%
	|
	100% external Visual
	|
	QC DPA Req'd
	|
QA DPA Sample Elantec Imposed	Pull QCI Group B, C, & D samples if applicable
	|
	Pack
	|
	Hold or completion of QCI's

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Class S Minus Hybrid Flow QRA-4

Group B	MIL-STD-883 Method-5008 TABLE XI	Sample Size
Subgroup 1	Physical Dimensions	2
Subgroup 2	PIND condition A	15
Subgroup 3	Resistance to solvents	4
Subgroup 4	Internal Visual and Mechanical	1
Subgroup 5	Bond Strength min 2 devices (# wires)	45
Subgroup 6	Die shear test	2
Subgroup 7	Solderability min 1 devices (# leads)	15
Subgroup 8	N/A for Class S	
Subgroup 9	Electrostatic Test	3
	Note: Devices are marked with an equilateral triangle.	
	(Note: tested per MIL-H-38534 3.6.8.2)	
Group C	**MIL-STD-883 Method 5008 TABLE XII**	
Subgroup 1	External visual, Temperature cycling	
	Constant Acceleration, Seal Fine/Gross Leak, X-ray	15
	Visual examination external, Electrical test 25°C, −55°C and +125°C	
Subgroup 2	a. Electrical read and record, 25°C, −55°C and +125°C	22
	Group A subgroup 1, 2, 3	
100% board	b. Burn in 1000 hours @ 125°C or 500 Hours @ 150°C	
Socket check	(Note: Must be the same temp as 100% Burn-in)	
	All testing must be completed in 96 hours after removal from burn-in	
	c. Electrical read and record 25°C, −55°C and +125°C	
	Group A subgroup 1, 2, 3	
	d. Complete delta's if applicable	
Subgroup 3	Internal Water Vapor	3
Group D	**MIL-STD-883 Method 5008 TABLE XIII**	
	Thermal Shock	5
	Stabilization Bake	5
	Lead integrity 1 device (# of Leads)	15
	Seal: Fine and Gross Leak	5

Min: samples required Group B 30 devices
Group C 40 devices 15 are Shippable
Group D 16 devices 5 are Shippable

Electro Static Discharge (ESD) Sensitivity

All semiconductor devices are sensitive to Electro Static Discharge (ESD) to some degree. For this reason, Elantec treats *all* of our devices as sensitive. Customers are urged to use similar controls throughout their facilities. This will optimize yields, prevent latent reliability problems, and eliminate component quality complaints which are due to ESD. Even components which are returned to Elantec for analysis should be handled with proper ESD procedures.

Device Design and Processing

Wherever possible, ESD protection networks are used on device pins. Metal routing and oxide thicknesses are carefully considered for optimum ESD performance. Testing per MIL-STD-883 Method 3015 is used to determine device and process performance.

Work Areas

Floors are covered with conductive tiles, attached with conductive adhesive.

Operators wear non-static generating or static dissipative smocks. Heel straps are used to ground the operators. Heel straps are checked daily for effectiveness.

Work station surfaces are conductive laminates or stainless steel. These are tied to Earth ground through protective resistors. Grounds are routinely inspected. Air ionizers are used to neutralize charges in areas which may generate static.

Storage shelving is grounded through protective resistors.

Handling

All handling containers (boxes, bags, etc.) are conductive. Pink poly which depends on surface properties and may wear out is not used. Common plastics (such as polystyrene and polypropylene) which are nasty static generators are *never* used in the work area.

Marking

All devices are marked with an equalateral triangle to warn the user that they are ESD sensitive.

Packaging

Devices are packed in either antistatic materials which are surrounded by a conductive Faraday shield or directly in conductive materials. The shielded containers are labeled with a yellow ESD warning label. Only antistatic treated "popcorn" is used as filler material in shipping boxes.

Macromodel Information

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The selected macromodels provided at the end of product datasheets are being supplied to users as an aid to circuit designs. While it reflects reasonably close similarity to the actual device in terms of performance, it is not suggested as a replacement for breadboarding. Simulation should be used as a forerunner or a supplement to traditional lab testing.

Users should very carefully note the following factors regarding these models:

Model performance in general will reflect typical baseline specs for a given device, and certain aspects of performance may not be modeled fully to keep the model as simple as possible thus minimizing computer running time. For example, PSRR and CMRR effects, parametric variation with temperature, operation under output short circuit conditions, and input noise sources are not included in the models. The current mode feedback amplifiers are not slew rate limited and yield optimistic values for large signal pulse responses.

While reasonable care has been taken in their preparation, we cannot be responsible for correct application on any and all computer systems. Model users are hereby notified that these models are supplied "as is", with no direct or implied responsibility on the part of Elantec, Inc. for their operation within a customer circuit or system. Further, Elantec, Inc. reserves the right to change these models without prior notice.

In all cases, the current data sheet information for a given real device is your final design guideline, and is the only actual performance guarantee. For further technical information, refer to individual device data sheets.

The Elantec engineering staff is in the process of improving these models, and we welcome your comments and feedback. Inquiries should be made to:

Applications Engineering Manager
Elantec, Inc.
1996 Tarob Ct.
Milpitas, CA 95035

Voice Telephone: (800) 333-6314
FAX: (408) 945-9305
TELEX: 910-997-0649

*MACROMODELS ON DISK ARE AVAILABLE UPON REQUEST.
CONTACT FACTORY OR LOCAL AREA REPRESENTATIVE.
Disks are 5¼" Low Density for IBM PC Compatible Computers.

Capabilities

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Mission

"To be the leading supplier of high performance analog intensive solutions for the computer peripheral, video processing, power control and instrumentation markets."

Elantec, Inc., founded in 1983 and located in Milpitas, California, is a fully integrated semiconductor company focused on providing high performance analog intensive functions for growing markets. The company specifically targets video processing and power control as dynamic markets requiring the companies specialized analog expertise. Elantec serves these markets with standard and application specific standard product, using high speed complementary bipolar and advanced CMOS technology.

To serve our customers requirements, close customer interface and time to market is essential for success. Our strategy is to establish a competitive advantage through a combination of market knowledge, design expertise, advanced process technologies, close customer interface, coupled with a management and design team with many years of analog experience.

Accomplishments

The company has over 125 employees and since 1983 has established an impressive record of technical accomplishments in its target markets. Elantec, Inc. has approximately 100 products in its catalog, representing a wide range of marketing and design expertise.

Video

The EL2020, introduced in 1986, was the industry's first monolithic current mode feedback (C.M.F.) amplifier. The EL2020 has since become the industry standard video amplifier and is augmented by a broad family of advanced C.M.F. amplifiers expressly designed for video applications.

Since then Elantec, Inc. has introduced a broad range of proprietary application specific products for video applications, such as DC restoration, variable gain amplifiers, video multipliers, multiplexers, and timing circuits.

These products are representative of Elantec's emerging family of video A.S.S.P. chips which provide significant advances for video system designers.

Power Products

The EL2007, introduced in 1986 was the industry's first integrated servo driver for the disk drive marketplace. Elantec has supplied many application devices to the leading disk drive suppliers, working closely with the customer to serve their demanding application specific requirements.

The EL7000 series Power Mosfet driver family, introduced in November of 1993, represents the industry's most comprehensive high-performance family of application specific ICs. Devices from this family serve the high-performance power supply, CCD imaging, and low cost A.T.E. pin electronics applications.

Instrumentation and A.T.E.

Elantec has a broad range of proprietary amplifiers for high speed applications. These products offer a selection and optimization of wide bandwidth, high slew rate and high output drive capability and are available in single, dual and quad configurations. In addition, the company has introduced industry-leading pin drivers, such as the EL2021 and EL1056, and companion pin receivers for the A.T.E. market.

Capabilities

The Future

In 1994 the company will introduce a total of 50 new products for the video, instrumentation, disk drive and power control markets. Approximately half of these products will be CMOS products, aimed at providing high performance analog at low voltage and low power. 90% of the company's products are proprietary and provide unique value at competitive costs to the customer.

Technology

The company has developed and uses a variety of technologies for its products. In particular, Elantec has focussed on developing an advanced complementary bipolar technology using dielectric isolation and silicon on insulator techniques for its high speed circuits. Complementary bipolar technology allows high speed analog signals to be processed efficiently in either signal polarity which greatly simplifies design methodology and substantially improves power dissipation. Because of the dielectric isolation technique, Elantec's complementary process has the additional inherent advantages of low capacitance, low crosstalk, no latch-up, high voltage, high temperature operation, and improved speed. Advances in technology together with outstanding design expertise will continue to provide superior solutions for Elantec's target markets.

In 1992 Elantec formed a CMOS design group to pursue a wider range of product in its target markets. The base technology is a 2 micron, dual metal, dual poly, mixed signal process. These CMOS products include video timing circuits and CMOS power driving and management circuits.

Process Technology

Bipolar Technology Capabilities

Elantec utilizes a combination of internal and external world class bipolar foundries. We match the appropriate technology to best serve the requirements of our customers' demanding design problems. Elantec currently uses the following bipolar technologies:

- Standard Linear J.I. (junction isolation)
  40V, NPN Ft = 600 MHz, PNP Ft = 5 MHz
- High Voltage, Oxide Isolated—Fully Complementary Bipolar for high performance, high voltage circuit applications.
  40V, NPN Ft = 800 MHz, PNP Ft = 800 MHz
  25V, NPN Ft = 1.5 GHz, PNP Ft = 1.5 GHz
- Low Voltage, Fast, Complementary Bipolar
  10V, NPN Ft = 4.0 GHz, PNP Ft = 3.0 GHz

CMOS Technology Capabilities

Elantec utilizes world class CMOS foundries. We match the appropriate process that best serves the stringent design requirements of our customers. Elantec's family of High Performance CMOS products are based on (2) processes, the first, optimized for 15 volt analog, and the second, for mixed signal design. Both use 2μ feature sizes, and stepper based technology. The next generation process will merge bipolar technology with the addition of 2 GHz vertical NPN's and both substrate and lateral PNP's.

Process 1 (Analog)

A single-poly, single metal technology, process 1 is optimized for analog. LDD (lightly doped drain) structures on both the pmos and nmos transistors extend the breakdown voltage, reduce the "Miller" overlap capacitance, and increase gain (Lambda). An epitaxial P-type substrate provides a solid ground plane. A substrate PNP (useful for ground referenced sources) is inherent to the process.

Process 2 (Mixed Signal)

An extension of process 1, process 2 adds second poly and metal layers to provide higher density, poly capacitors, non-volatile EE memory, and high sheet rho resistors.

Both processes are useable to 50 MHz.

Advanced CAD Capabilities

Elantec provides each circuit designer and layout artist with the most up to date Sun workstations at their desk. All stations are networked together to a Sun server. Extra "computing engines" are also available on the network. The Sun network is connected to the corporate network to facilitate corporate wide communication. Elantec uses Cadence and MicroSim design software and Cadence IC layout software and design verification tools. The design tool suite can use the computing capability of the entire Sun network to allow extensive simulations covering the variations of the wafer fabrication process, based on data derived from capability studies.

Design Capabilities

Elantec's engineering team has many years of experience defining, designing, manufacturing and testing analog and mixed signal devices, utilizing both Bipolar and CMOS technologies.

Functions we currently supply are: current and voltage feedback amplifiers, multipliers, video specific standard products, pin drivers and receivers, C.R.T. drivers, buffers, servo electronics, MOSFET and IGBT drivers, instrumentation amplifiers, and precision amplifiers. Please discuss your challenging system requirements with our talented technical team.

Test Automation/Equipment Capability

Elantec utilizes the LTX Model 77 test system with TS80 and TS88 test stations for primarily DC testing operational amplifiers, buffers, comparators, and other linear devices. In general, custom socket adaptors have been developed for unique devices such as current feedback amplifiers, DC restored video amplifiers, sync separators, and disk drive servo motors. A wide range of automatic handlers allow high speed, room temperature, and extended range temperature testing of Dual in Line (DIP), Small Outline (SO) packages, metal cans such as TO3, TO99, and TO8.

The DC testing capability of the LTX Model 77 is augmented with rack mounted AC test systems which are integrated into the LTX. The time domain systems which are used to measure very fast rise times, slew rates and propagation delays are comprised of programmable pulse generators and 1 GHz digitizing oscilloscopes and are capable of measurements under 10 pS. The frequency domain systems which are used to measure bandwidth, differential phase, differential gain, phase linearity, gain flatness, distortion, etc. are composed of programmable signal sources and network analyzers and are capable of measurements to 500 MHz.

Elantec ensures the accuracy of all critical test parameters by testing using alternative devices to the LTX system.

Capabilities

Packaging Capability

Elantec supports most industry standard package types. Currently we are manufacturing standard products in the following packages:

P-DIP, SO: P-DIP packages—8, 14, 16-pin, SO packages—8, 14, 16, 20, 28 lead

Power Packages: TO-220—5-lead, TO-3—8-lead, TO-5—10-lead, TO-8—12-lead

Additionally, we can supply special packages upon request for volume and special applications. Contact Elantec's marketing department for availability.

Quality and Service

Elantec's commitment to quality begins with the product definition, design and characterization and continues through the complete process. We are a fully integrated semiconductor company with its own complete manufacturing facility, including wafer fabrication, assembly and test, Elantec is positioned to provide excellent service and quality to its customers.

Superior product performance and quality are augmented by a commitment to customer service and technical support in order to make our customers successful. Technical customer support is provided through corporate applications, field applications engineers and technical seminars. Sales support is provided through the Elantec field sales force which directs a world wide network of technical representatives and distributors.

Terms and Conditions of Sale

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

ELANTEC, INCORPORATED ("SELLER") TERMS AND CONDITIONS OF SALE

1. ACCEPTANCE OF ORDER

THIS ACKNOWLEDGEMENT AND ACCEPTANCE IS EXPRESSLY LIMITED TO AND MADE CONDITIONAL UPON THE TERMS AND CONDITIONS CONTAINED HEREIN AND ANY OF THE BUYER'S TERMS AND CONDITIONS WHICH ARE IN ADDITION TO OR DIFFERENT FROM THOSE CONTAIN HEREIN WHICH ARE NOT SEPARATELY AND SPECIFICALLY AGREED TO IN WRITING ARE HEREBY OBJECTED TO AND SHALL BE OF NO EFFECT.

Only those orders accepted by Seller as its home office in Milpitas, California shall be binding upon Seller.

2. PRICES

Irrespective of any prices quoted by Seller or listed on Buyer's order, Seller's acceptance of any order is subject to the prices shown on Seller's acknowledgment. Said prices are firm and are not subject to adjustment other that "precious metals adjustments" or "precious metals surcharges" at Seller's option to cover Seller's cost of fluctuations in the price of precious metals utilized in the manufacture of Seller's products.

3. TAXES

All prices are exclusive of all federal, state and local excise, sales, use and similar taxes. Such taxes shall be paid by Buyer, or in lieu thereof Buyer shall provide Seller with a tax exemption certificate acceptable to the taxing authorities. When applicable, such taxes will appear as separate additional items on the invoice unless Seller receives a proper tax-exemption certificate from Buyer prior to shipment.

4. PAYMENT

Unless Seller has extended credit to Buyer as described below, Buyer shall pay Seller, at Seller's option either by: Cash with Order, C.O.D., Letter of Credit or Sight Draft.

Should Seller elect to extend credit to Buyer, payment shall be made in full within thirty (30) days of the date of Seller's invoice. Seller reserves the right at any time to change the amount of or to withdraw any credit extended to Buyer.

Any payments made in excess of thirty (30) days may be subject to late charges.

5. TITLE AND DELIVERY

Seller shall deliver products sold hereunder to Buyer F.O.B. Seller's factory. Partial deliveries shall be permitted. Upon such delivery to a carrier at Seller's factory, title to the products and all risk of loss or damage shall pass to Buyer.

6. SHIPMENT

All shipping charges and expenses shall be paid by Buyer. Seller will not insure the products sold hereunder unless requested by Buyer in which case Buyer will pay for such insurance.

Shipments will be made, at Seller's option, either by Parcel Post, Railway Express. Air Express, Air Freight, or as otherwise determined by Seller.

Shipping dates are approximate and are dependent upon Seller's prompt receipt of all necessary information from Buyer.

7. PATENTS

With respect to products manufactured soley to Seller's designs and specifications, Seller shall defend any suit or proceeding brought against Buyer insofar as such suit or proceeding is based on a claim that any such products furnished hereunder infringe any patent of the United States. If Seller is notified promptly in writing of such suit or proceeding and given full and complete authority, information, and assistance by Buyer for such defense, Seller shall pay all damages and costs finally awarded against Buyer in any such suit or proceeding, but Seller shall not be responsible for any compromise thereof made by Buyer without the written consent of Seller. In the event that such products are held in such suit or proceeding to infringe a patent of the United States and their use is enjoined, or if in the opin-

ion of Seller such products are likely to become the subject of a claim of infringement of a patent of the United States, Seller, in its sole discretion and at its won expense, may either: (a) procedure for Buyer the right to continue using such products with noninfringing products; or (b) modify such products so that they become noninfringing; or (c) replace such products with noninfringing products; or (d) accept the return of such products, granting Buyer a refund therefor equal to the depreciated value thereof.

Seller shall have no liability to Buyer under any provision hereof if any patent infringement or claim thereof is based upon (a) a modification of the products not introduced by or approved by Seller; or (b) the interconnection or use of the products in combination with products with other devices not made by Seller; or (c) the use of the products in other than an application recommended by Seller.

The foregoing states the entire liability of Seller for infringement of patents by Seller's products or any part(s) thereof.

8. INDEMNITY

Buyer shall indemnify, defend, and hold Seller harmless from and against any and all liability, damages, expenses, costs or losses resulting from any suit or proceeding brought for infringement of a patent(s), copyright(s), or trademark(s), or for a misappropriation of use of any trade secret(s), or for unfair competition arising from Seller's compliance with Buyer's design, specifications or instructions.

9. SECURITY INTEREST

Notwithstanding passage of title of products sold hereunder to Buyer F.O.B. Seller's factory, Seller shall retaln a security interest in the products until payment has been made in full by Buyer for such products. Buyer shall perform all acts necessary to perfect and maintaln such security interest.

10. WARRANTIES

Seller warrants to Buyer that Seller's standard products sold hereunder (and any services furnished therewith) which are not used in any medical or life support application shall be free from defects in material and workmanship and shall conform to the applicable specifications (if any) for a period of one year from the date of shipment. For products which are not standard products of Seller, such as dice and developmental or custom designed products. Seller warrants to Buyer that such products sold hereunder (and any services furnished therewith) shall be free from defects in material and workmanship and shall conform to the applicable specifications (if any) for a period of thirty (30) days from the date of shipment.

Should products sold hereunder fall to meet the above applicable warranty, Seller, at its option, shall repair or replace such products or issue Buyer a credit provided that (a) Seller is notified in writing by Buyer within thirty (30) days after discovery of such failure; (b)Buyer obtains a Return Material Authorization from Seller prior to returning any defective products to Seller; (c) the defective products are returned to Seller, transportations charges prepaid by Buyer; (d) the defective products are received by Seller for adjustment no later than four (4) weeks following the last day of the warranty period, and (e) Seller's examination of such products shall disclose, to its satisfaction, that such failures have not been caused by misuse, abuse, neglect, improper installation or application repair, alteration, accident or negligency in use, storage, transportation or handling.

In the event of failure to meet the above applicable warranty with respect to products sold hereunder cannot be corrected by Seller's reasonable efforts, the Seller and Buyer shall negotiate an equitable adjustment in price.

The foregoing warranty provisions set forth the Seller's sole liability and the Buyer's exclusive remedies for claims (except as to title) based on defects in or failure of any products sold hereunder or services furnished hereunder whether the claim is based in contact, tort, (including negligence), warranty or otherwise and however instituted. Upon the expiration of the applicable warranty for any products sold hereunder, all such liability shall terminate.

The above warranty periods shall not be extended by the repair or replacement of products pursuant to any of the above warranties. The above warranties shall apply only to Buyer and shall not apply to Buyer's customers or any other third parties.

SELLER PRODUCTS ARE NOT DESIGNED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS WITHOUT THE SPECIFIC WRITTEN CONSENT OF THE PRESIDENT OF ELANTEC. LIFE SUPPORT SYSTEMS ARE EQUIPMENT INTENDED TO SUPPORT OR SUSTAIN LIFE AND WHOSE FAILURE TO PERFORM WHEN PROPERLY USED IN ACCORDANCE WITH INSTRUCTIONS PROVIDED CAN BE REASONABLY EXPECTED TO RESULT IN SIGNIFICANT PERSONAL INJURY OR DEATH. USERS CONTEMPLATING APPLICATION OF SELLER PRODUCTS IN LIFE SUPPORT SYSTEMS ARE REQUESTED TO CONTACT SELLER FACTORY HEADQUARTERS TO ESTABLISH SUITABLE TERMS AND CONDITIONS FOR THESE APPLICATIONS. SELLER'S WARRANTY IS LIMITED TO REPLACEMENT OF DEFECTIVE COMPONENTS AND DOES NOT COVER INJURY TO PERSONS OR PROPERTY OR OTHER CONSEQUENTIAL DAMAGES.

11. LIMITATION OF LIABILITY

In no event, whether as a result of breach of contract, warranty or tort (including negligence) or otherwise shall Seller be liable for any special, consequential, incidental or penal damages, including but not limited to, loss of profit or revenues, loss of the product or any associated equipment, damaged to associated equipment, cost of captial, cost of substitute products, facilities, service or replacement power, down time costs or claims of Buyer's customers for such damages. If Buyer transfers title to or leases products sold hereunder to any third party, Buyer shall obtain from such third party a provision affording the Seller the protection of the preceding sentence.

Except as provided in the above "Patents" article, whether a claim is based in contract, tort (including negligence) or otherwise, the Seller's liability for any loss or damage arising out of, or resulting from any products sold hereunder or services furnished hereunder shall in no case exceed the price of the specific product(s) or service(s) which gives rise to the claim. Except as to title, any such liability shall terminate upon the expiration of the applicable warranty period specified in the above "Warranties" article.

12. U.S. GOVERNMENT CONTRACTS

If the products to be furnished hereunder are to be used in the performance of a U.S. Government contract or subcontract, no Government requirments or regulations shall be binding upon Seller unless specifically agreed to by Seller in writing.

If the Government terminates such a contract or subcontract in whole or in part through no fault of or failure to perform by Buyer, this order may be canceled in writing in the same proportion, and the liability of Buyer for termination allowances shall be determined by the then applicable regulations of the Government regarding termination of contracts.

13. EXCUSABLE DELAYS

Seller shall not be liable for delays in delivery or performance due to any cause beyond its reasonable control, including, without limitation, acts of God, acts of Buyer, strikes or other labor disturbances, inability to obtain necessary materials, components, services or facilities.

14. CANCELLATIONS OF STANDARD PRODUCTS

Should Buyer terminate any order accepted hereunder or should Seller terminate any order accepted hereunder due to Buyer's nonperformance of its obligations hereunder, then Buyer shall pay Seller its reasonable termination charges within fifteen (15) days from the date of invoice of same.

Buyer may request rescheduling or cancellation by providing thirty (30) days written notice to Elantec provided however, that elantec is not obligated to accept such notice, but if such notice is given and accepted by Elantec, then Elantec has the right to deliver and be paid by Buyer for:

1. 100% of quantity of devices scheduled for delivery within thirty (30) days following receipt of said notice.

Terms and Conditions

2. 50% of quantity of devices scheduled for delivery within 30–60 days following receipt of said notice.

15. CANCELLATION OF PRODUCTS MANUFACTURED TO BUYER'S DESIGN/SPECIFICATIONS INCLUDING ALL NON-STANDARD AND DISK DRIVE PRODUCTS

Charge for engineering, design, generation of data, lot charges or any other special charges that are not for product are non-cancelable except with prior written permission from Seller.

Buyer may request rescheduling or cancellation of product by providing 60 day notice to Elantec provided, however, that Elantec is not obligated to accept such notice but if such notice is given and is accepted by Elantec, then Elantec has the right to deliver and be paid by the Buyer for:

1. 100% quantity within 60 days following written receipt of said notice;
2. All additional work in process scheduled within the 16 week delivery time period shall be paid for by Buyer at a price based on the percentage of completion of such inventory applied to the price for the finished product. Buyer shall also promptly pay to Elantec; (a) costs of settling and paying claims arising out of termination of work under Elantec's subcontracts or vendors; (b) reasonable costs of settlement, including engineering, development, accounting, legal and clerical costs; (c) twenty percent (20%) of the purchase price of the purchase order to be canceled.

16. ASSIGNMENT

Any assignment by Buyer of this order or of any rights or obligations in connection therewith shall be void without the written prior consent of the Seller.

17. EXPORT TO NON-APPROVED COUNTRIES

Buyer agrees to take all reasonable and necessary precautions to prevent ultimate exportation of Elantec products to countries prohibited by rules or regulations of the United States Government, and to obtain all export licenses and other governmental approvals necessary prior to the export of any Elantec products.

18. MISCELLANEOUS

The validity, performance and construction of these terms and conditions of sale and any sale hereunder shall be governed by the laws of the state of California.

The invalidity, in whole or in part, of a y provision herein shall not affect the validity or enforce ability of any other provision herein.

Any representation, warranty, course of dealing or trade usage not contained or referenced herein shall not be binding on Seller.

No modification, amendment, recision, waiver or other change in these terms and conditions shall be binding on Seller unless assented to in writing by Seller's duly authorized representative.

Seller reserves the right to manufacture and/or assemble its products in any of its worldwide facilities unless otherwise agreed to in writing with Buyer.

Elantec Applications Articles

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Applications Articles

The following is a list of informative applications articles written by Elantec engineers, as well as editors from the major electronics publications. Reprints are available, consult factory.

A Linear, Tunable Sinewave Oscillator	Barry Harvey, Elantec Electronic Design—June, 1993
DC Restored 100 MHz Current Feedback Video Amplifier Applications Note #3	John Lidgey & Chris Toumazou LTP Electronics, Inc.—October, 1993
50 MHz AGC Circuit Restores DC Level	Barry Harvey, Elantec EDN—September, 1993
EL4083/EL4084 Current Mode, Four Quadrant Multiplier Applications Note #4	Ron Dow, Elantec August, 1993
A Current Feedback Fader/Variable-Gain Control Multiplexer	Barry Harvey, Elantec August, 1993
Current Feedback Op Amp Limitations: A State-of-the-Art Review	Barry Harvey, Elantec May, 1993
Active Integrator Employs CMF	Stuart Smith, Elantec Electronic Design—January, 1993
High Frequency Amplifier Instability	Barry Siegel, Elantec October, 1992
Buffer splits power supply	Stuart Smith, Elantec EDN—August, 1992
Quad op amp implements unusual notch filters	Michael Sedayao, Elantec EDN—July, 1992
Macromodels aid in use of current-mode feedback amps	Joe Tabor, Barry Siegel, Elantec Electronic Products—April, 1992
A Low-Noise Variable Gain Control Applications Note #1	Barry Harvey, Elantec April, 1992
Thermal Considerations of the SO-8 Applications Note #2	Barry Siegel, Elantec March, 1992
Buffer goes solo in fast active filter	Michael Sedayao, Elantec EDN—March, 1992
Reliability and the electronics engineer	Barry Siegel, Elantec October, 1991
Analog Multiplier IC Works from DC to 200 MHz	Frank Goodenough, Senior Editor Electronic Design—Feb. 28, 1991
FET-input amplifier settles fast	Barry Siegel, Elantec EDN—December, 1990
Loop-through amp rejects common-mode noise	Barry Siegel, Elantec EDN—December, 1990
Using gain buffer can improve precision performance	Barry Siegel, Elantec EDN—November, 1990

APPLICATIONS ARTICLES

A Simple Method for Characterizing Hybrid Package Thermal Impedances	Barry Siegel, Steve Ott, Elantec Hybrid Circuit Technology—June, 1990
Alternative to Laser Trim: Zapping Zenners, Blowing Fuse Links	Caleb Brown, Elantec Electronics Test—Sept. 1989
Build a Circuit Board Tester with Your PC	Barry Harvey, Elantec Electronic Design—Feb. 9, 1989
Current-mode Speeds Video Amps	Electronic Design—July 27, 1989
Delta Modulators Simplify A/D Conversion	Barry Harvey, Elantec EDN—June 22, 1989
Simple Techniques Help You Conquer Op Amp Instability	Barry Siegel, Elantec EDN—March 31, 1989
Precision Comparators Ease Oscillator and Data-converter Design	Jon Dutra, Barry Harvey EDN—Feb. 18, 1989
Special Circuit Simplifies Testing of Voltage Comparators	Barry Harvey, Elantec EDN—Oct. 15, 1987
Simple Circuits Provide Accurate AC Testing of Op Amps	Barry Harvey EDN—May 14, 1987
Low-Cost IC Amp Carries Video	Frank Goodenough, Senior Editor Electronic Design—April 16, 1987
Take the Guesswork Out of Settling-time Measurements	Barry Harvey, Elantec EDN—Sept. 19, 1985

Tutorials

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

Reliability and the Electronic Engineer
by Barry Siegel

Introduction

There is probably no more crucial issue than Reliability at the system level to both the component vendor and the systems house, and surprisingly there is very limited understanding of the mechanisms that yield to failures. This paper sets forth simply what the electronic Design Engineer needs to know with regard to calculating a given component's Mean Time Between Failure (MTBF), Failure Rate (FR), Failures In Time (FITS), and what all this jargon means.

Reliability Overview

Contrary to popular opinion, all integrated circuits begin "dying" the moment they are born, and in general, raising the average junction temperature will result in increasing the failure rate. The Arrhenius relationship which is common in many physical and chemical processes has been found to fit the failure rates in IC's as well. Equation (1) expresses the relative failure rate for temperatures, T1 and T2, and the ratio, R2/R1, is often referred to as the Acceleration Factor.

$$\frac{R2}{R1} = e - \left(\frac{EA}{KT2} - \frac{EA}{KT1} \right) \qquad (1)$$

Where:

R = Failure Rate

EA = Activation Energy (typically 0.5 eV to 1 eV)

T = Absolute Temperature (°K)

K = Boltzmann's Constant (1.38×10^{-23})

One very significant issue is the assumed Activation Energy. Illustrated in Figure 1 is the Failure Rate for 0.5 eV and 1 eV as a function of temperature. Significantly, at junction temperatures above 100°C, the failure rate at 1 eV is 1,000 times that of 0.5 eV.

Reproduced in Figure 2 are the reported Activation Energies for various kinds of components. At Elantec, we use 0.8 eV to 1.0 eV, which is best suited to the kinds of processes that we employ.

In order to calculate MTBF we will also need to obtain reliability data from the IC vendor. Virtually all manufacturers routinely run life tests on devices which span their product line and package repertoire. Life test usually means placing devices in a burn-in oven, under power, at temperatures which are typically set at 125°C for 1,000 hours or more. Shown in Figure 3 is data taken from a slice in time for a variety of devices manufactured by Elantec. As indicated, a total of 692 devices were tested at 125°C, and the total device hours were 867,520. Failure Rate and MTBF are given by:

$$FR = \frac{\text{No. of Failures}}{\text{Total Device Hours}} \qquad (2)$$

$$MTBF = \frac{1}{\text{Failure Rate}} \qquad (3)$$

Since we had two failures in 867.5K hours, the FR is 2.3 per million hours, and the MTBF is 433.8K hours (at 125°C). Suppose we wanted to know what the FR and MTBF would be at 25°C. Using Equation (1) and assuming that the Activation Energy is 1 eV, we calculate an Acceleration Factor of:

$$\frac{R2}{R1} = e - \left(\frac{EA}{KT2} - \frac{EA}{KT1} \right)$$

$$= e - \left[\frac{1.6E-19}{1.38E-23} \left(\frac{1}{398°K} - \frac{1}{298°K} \right) \right]$$

$$= 17{,}698$$

Then we multiply the 125° MTBF of 433.8 hours by 17,698 to obtain 7.7 billion hours and corresponding FR of 0.13 per billion hours.

Another often heard term is FITS which stands for Failures in Time and is defined as the number of failures per billion hours. For the example above, FITS is equal to 0.13.

The Real World

It turns out that the foregoing analysis isn't quite right, and the reason is that our calculation was based on a relatively small sample of devices. To prove the point without thinking about it too much, suppose that we had observed zero failures in the earlier example. That would lead us to the false conclusion that the MTBF was infinite and the FR was zero. What do we do now?

Reliability and the Electronic Engineer Tutorial #1

Fortunately, we can turn to Poissan statistics to bail us out. And we all thought that the statistics course in school would never be of any benefit. Equation (4) predicts the probability (of failure), P(X), of finding X failures in a sample whose average failure rate is A.

$$P(X) = \frac{e^{-A} A^X}{X!} \quad (4)$$

P(X) = Probability (of failure)
X = Failures observed
A = Average number of failures

Suppose we ran a large number of such life tests (say 1,000) which actually had an average failure rate of 3.12. Figure 4 summarizes the statistics of equation (4). The table predicts that 4.4% of the time (or in 44 life tests) we would observe no failures, 13.7% of the time we would observe one failure, 21.5% of the time we would observe 2 failures, etc. We could say that 39.6% of the time we would observe either no failures, 1 failure, or two failures. Probably a better way of looking at this data is that in 1,000 tests we would anticipate observing more than 2 failures 60.4% of the time. Therefore, if we ran only one test and observed 2 failures, we would have to say, "with a confidence level of 60.4%, that the actual failure rate is 3.12."

We should use 3.12 average failures in all of our calculations instead of our 2 observed failures, and we should always add, "to a 60% confidence level" to all the numbers we quote. So, our experimental data from Figure 3 boils down to an MTBF of 867,520 hours divided by 3.12 or 278,051 hours at 125°C to a 60% confidence level.

Fortunately, we don't have to go through all this convoluted reasoning each time we want to make calculations because the statisticians have calculated fudge factors for us which are summarized in Figure 5.

Note that this solves our "zero observed failure problem" by assigning 0.916 average failures to the case of zero observed failures to a 60% confidence level.

On the other hand, 60% confidence level doesn't sound very confident. If we wanted to be more conservative, we could use a fudge factor from a 90% confidence level. Now our 3.12 average failures become 5.3, and that makes our failure rate and MTBF look a lot worse. Most semiconductor manufacturers have historically used 60% confidence levels.

The Bottom Line

To ascertain the system level FR and MTBF, we must perform a thermal analysis for a given device to calculate average junction temperature. We will then use the Arrhenius Relationship and the IC manufacturer's reliability data and Activation Energy to predict FR and MTBF. For example, an EL2044 packaged in a plastic DIP is operated from 15V rails at an ambient temperature of 70°C. The output voltage is 2V and the load, R_L, is 150Ω; the feedback resistor, R_F, is 300Ω. Th quiescent power, Pq, is simply:

$$Pq = (V+ - V-)(Is) \quad (5)$$

The power dissipated due to load, Pl, is:

$$Pl = (V+ - V_{OUT})\left(\frac{V_{OUT}}{R_L \,||\, R_F}\right) \quad (6)$$

The total power is given by:

$$Pt = Pq + Pl \quad (7)$$

From the datasheet, we obtain an Is of 7.6 mA, so Pq is 228 mW. Pl is 260 mW, and Pt is equal to 488 mW.

$$T_J = (Pt)(\theta_{JA}) + T_A \quad (8)$$

θ_{JA} obtained from the datasheet is 95°C per watt which results in a junction temperature of 116°C. The datasheet states that the maximum allowable junction temperature is 150°C, so the application is okay from that point of view.

The life test circuit for the EL2044 indicates that the test is done with 15V supplies and essentially no load at 125°C under "ambient" conditions; hence, the life test data reported by Elantec would be under these conditions. The average power dissipation using equation (5) would be 228 mW, and the corresponding junction temperature per equation (8) would be 147°C.

We can now examine the predicted impact on MTBF and FR resulting from operating the junctions at 116°C. Using the Arrhenius Relationship we derive an Acceleration Factor of:

$$AF = \frac{R2}{R1}$$

$$= e^{-\left[\frac{1.6E-19}{1.38E-23}\left(\frac{1}{389°K}-\frac{1}{420°K}\right)\right]}$$

$$= 9.0$$

The corrected (for finite sample size) MTBF with a 60% Confidence Factor that we calculated earlier was 278K hours. To obtain the "worst case" MTBF, simply multiply by 9.0 to obtain 2.5 million hours with a corresponding Failure Rate of 0.4 per million hours.

2.5 million hours seems like a long time, but presumably there could be many devices in the system. If, for example, there were 100 amplifiers, we would expect an MTBF of about 34 months.

The moral of the story is that heat is the implacable enemy of integrated circuits. In order to insure the system reliability, junction temperature must be minimized by every available means. This might mean putting a heat sink on the package or reducing the power supply voltages, or increasing the load resistance, or all of the above.

In summary, in order to calculate MTBF or FR in a system, we need to determine the device's average junction temperature in our system, obtain the Activation Energy and Failure Rate data from the vendor, calculate the Acceleration Factor for our specific application, and correct the failure rate for finite sample size at a Confidence Factor commensurate with the system's needs.

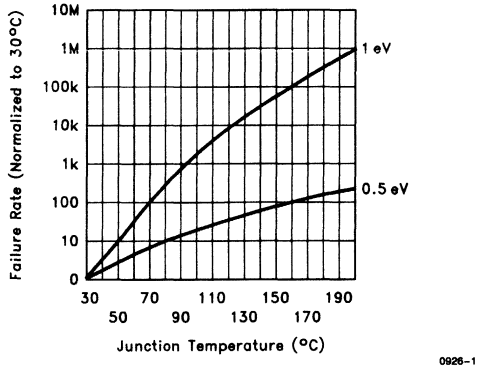

Figure 1

Activation Energy

Component and Mechanism	Reported EA (eV)	
	Main Population	Weak Population
Silicon Semiconductor Devices		
Silicon Oxide and Si/Sio2 Interface		
Surface Charge Accumulation, Bipolar	1.0	
Surface Charge Accumulation, MOS	1.2	
Slow Trapping Charge Injection	1.3–1.4	
Metalization		
Electro-Migration	0.5–1.2	
Corrosion (Chemical, Galvanic, Electrolytic)	0.3–0.6	
Bonds		
Intermediate Growth Al/Au	1.0	
N-Channel Si Gate Dynamic RAM		
Slow Trapping	1.0	
Contamination	1.4	1.4
Surface Charge	0.5–1.0	
Polarization	1.0	
Electro-Migration	1.0	
Oxide Defects	0.3	0.3
FAMOS Transistors		
Charge Loss	0.8	

Source: *Burn-In*, F. Jensen, N. Petersen, Wiley and Sons, New York, 1982

Figure 2

Device Type	Quantity	Failures	Hours	Device-Hours
EL2020CN	45	0	1,000	45,000
EL2020CN	45	0	1,000	45,000
EL2028J	105	1	1,000	105,000
EL2020J/883	105	0	1,000	105,000
EL2030CN	77	1	1,234	95,020
EL2033CN	105	0	1,000	105,000
EL2037CM	105	0	2,500	262,500
EL2190L/883	105	0	1,000	105,000
TOTALS	692	2	9,732	867,520

Figure 3. Partial Summary of Elantec Reliability Data

Poisson Distribution Table

X	Average = X!	3.12 P(X)	Sum (P(X))
0	1	0.044157	0.044157
1	1	0.137770	0.181927
2	2	0.214921	0.396849
3	6	0.223518	0.620367
4	24	0.184344	0.794712
5	120	0.108790	0.903503
6	720	0.056571	0.960074
7	5040	0.025214	0.985289
8	40320	0.009833	0.995123
9	362880	0.003409	0.998532
10	3628800	0.001063	0.999595
11	39916800	0.000301	0.999897
12	4.8E+08	0.000078	0.999975
13	6.2E+09	0.000018	0.999994
14	8.7E+10	0.000004	0.999998
15	1.3E+12	0.000000	0.999999

Figure 4

Number of Failures	50%	60%	70%	80%	90%	95%
0	0.693	0.916	1.204	1.990	2.305	2.990
1	1.678	2.022	2.439	2.990	3.890	4.740
2	2.674	3.120	3.615	4.280	5.300	6.300
3	3.672	4.160	4.762	5.500	6.700	7.750
4	4.671	5.250	5.891	6.700	8.000	9.150
5	5.970	6.300	7.005	7.900	9.250	10.50
6	6.669	7.350	8.111	9.100	10.55	11.85
7	7.669	8.400	9.209	10.25	11.75	13.15
8	8.669	9.450	10.30	11.40	13.00	14.45
9	9.668	10.50	11.38	12.50	14.20	15.70
10	10.66	11.55	12.47	13.65	15.40	16.95

Figure 5. Average Failures Confidence Level

High Frequency Amplifier Instability
by Barry L. Siegel

Introduction
High frequency amplifiers pose unique, often puzzling, and frustrating instability problems which can manifest themselves as oscillation, peaking, or overshoot. This paper will address the classic causes of instability starting with the Bode plot and phase margin. Problems unique to high frequency amplifiers will then be addressed covering input capacitance, load capacitance, power supply inductance and decoupling, the use of buffers in the feedback loop, the effects of source and feedback impedance on stability and settling time, and driving loads such as flash Analog-to-Digital converters.

Classical Instability
The classical cause of instability; i.e., the one we learned in school, was due to phase shift through the amplifier which results in a feedback phase of zero degrees "around the loop." Illustrated in Figure 1 is the Bode plot of an amplifier whose unity gain crossing frequency is about 100 MHz with a Phase Margin of about 45°. Phase margin is simply the difference between the output's phase lag relative to the input at unity gain and 180°. Since the op amp gives us 180° gratis, the circuit would oscillate under closed loop conditions if we somehow lost the 45°. The key thing to remember is that any loss of Phase Margin will result in peaking, overshoot, or degraded settling time. Figure 2 illustrates Normalized Gain for various Phase Margins for a single pole response system. For the purpose of our discussion, any departure from an ideal response of an amplifier which results in degraded settling time, overshoot, peaking, or oscillation will be called instability.

Buffers in the Feedback Loop
There are occasions when an open loop buffer is inserted within the feedback loop to drive heavy load currents or to isolate perturbations on the output from the input. The parameter to pay attention to is the phase shift of the buffer at a frequency equal to the unity gain crossing frequency of the amplifier. The reason, of course, is that the phase lag through the buffer may be sufficient to erode or eradicate the phase margin of the amplifier, and the net result is instability. The only solution, assuming that the bandwidth of the amplifier is mandatory, is to select a buffer with sufficient bandwidth and minimum phase lag, or to put the buffer outside of the loop.

Power Supply Decoupling
Unfortunately, in the real world of high speed amplifiers, there are many and often more dominant causes for instability. Illustrated in Figure 3 is an amplifier whose power supply leads exhibit significant self inductance. The time varying load current flowing through the supply inductance induces a voltage which is essentially in phase with the input. A vestige of this voltage can be coupled to the input through parasitic capacitance on the printed circuit board (or on the amplifier) which results in instability particularly if the source impedance is high.

The obvious solution is to decouple the power supply leads. The question is with what kind of capacitor. The answer is, in general, with a ceramic disc capacitor. A surprising aspect is that 0.01 μF capacitors actually do a better job than 0.1 μF in that the latter exhibits more self inductance. Chip capacitors reduce the inductance to a minimum and should always be used when the manufacturing process allows. Recently, Tantalum electrolytics have improved but tend to cost more and take up more space. In applications requiring large output currents, Tantalum electrolytics are mandatory, and a good rule of thumb is 4.7 μF per 100 milliampere. Clearly, both rails have to be bypassed, the capacitors placed as close to the package pins as possible, and must be terminated in the ground plane.

More often than not, the compensation capacitor on the chip uses one of the rails as "AC ground", and many amplifiers (and comparators) oscillate due to poor bypassing of the rails. Futhermore, the PSRR of most amplifiers is degraded at high frequency, and "system" noise will corrupt the signal.

Input Capacitance

The source impedance and any parasitic capacitance at the amplifier's input form a low pass filter and its attendant phase shift which can and will degrade the Phase Margin of the system. The change in Phase Margin is given by:

$$d\phi = \arctan(f_u/f_c) \quad (1)$$

where f_u is the amplifier's unity gain crossing frequency and:

$$f_c = \frac{1}{2\pi(R_G||R_F)(C_S)}$$

For the "simple" voltage follower of Figure 4 (C_S = 2 pF), the degradation in Phase Margin is 51°, which means that the 100 MHz amplifier of our earlier example would oscillate.

The feedback resistor, R_F, can be bypassed with a capacitor, but the optimum value is largely a function of parasitics and is always a low and non-standard number. The best solution is to keep the impedance levels as low as possible. Some amplifiers will require a small value for R_F when operated as a voltage follower. The issue in this instance is isolating the input capacitance from the output.

Current Feedback Amplifiers are simply a special case in that R_F is selected for bandwidth. The main issue here is minimizing capacitance at the inverting input.

Load Capacitance

A simple way looking at instability resulting from loading the amplifier with a capacitor is to assume that the open loop output impedance and the load create a low pass filter and its attendant phase shift akin to the problem created by input capacitance as shown in Figure 5. A formula similar to equation (1) results:

$$d\phi = \arctan(f_u/f_c) \quad (2)$$

where f_u is the amplifier's unity gain crossing frequency and:

$$f_c = \frac{1}{2\pi(R_O)(C_L)}$$

R_O = The Amplifier's open loop output impedance

A better way is to realize that, to the first order, the output impedance of the amplifier behaves very much like an inductor. Most amplifiers employ class AB compound emitter follower output stages, and since hfe decreases as a function of frequency, R_O increases from 10Ω or 20Ω at low frequency to 100Ω or more at high frequency—precisely the behavior of an inductor. An inductor in parallel with a capacitor creates a tank circuit, and a tank circuit can and will oscillate. Whereas, this analysis is not rigorous, it does lend an intuitive insight to a straightforward technique for eliminating or minimizing load induced instability.

The technique employs the use of a "snubber"; i.e., a resistor in series with a capacitor from the amplifier's output to ground as illustrated in Figure 6. The obvious question is what value R and C should be used? The quickest answer can be obtained using an oscilloscope and operating the amplifier under conditions that it will see in the end application. The frequency of the "ring" in response to step input (or oscillation frequency) is observed, and R is calculated by:

$$R = \frac{1}{2\pi f C_L} \quad (3)$$

where f is the "ring" frequency, and C_L is the load. The value for C should be made equal to C_L.

The values may have to be iterated somewhat to achieve optimum performance, but as illustrated in Figure 7, excellent results can be achieved in very short order. In this instance, the 100 MHz op amp can be tamed quite nicely using this technique.

High Frequency Amplifier Instability Tutorial #2

Current feedback amplifiers offer a unique solution to this problem in that the bandwidth is determined by the feedback resistor. In this instance, R_F can be increased to a value sufficient to kill the instability but small enough to achieve the desired slew rate and bandwidth.

The classical technique is shown in Figure 8, which appears on many datasheets in applications in which the amplifier is used to drive the input (capacitance) of a flash A-to-D. The primary limitation of this approach is that 6.9 time constants will be required for the input to settle to 0.1%, and R is chosen to keep the amplifier from peaking. The net result is that the time constant and settling time may not be compatible with the required conversion time of the system. The "snubber", on the other hand, does not impact the settling time except to eliminate the peaking.

Ground Planes and Layout Considerations

There is, of course, no such thing as "ground" outside of the classroom. The use of ground planes is mandatory in high speed applications. It is frankly difficult to communicate the "art" involved in the design of good ground planes in a paper like this, but there are some general rules that we will discuss. Contrary to popular notion, the ground plane should be terminated in the vicinity of the inputs to minimize input capacitance. The ground plane is also selectively removed to prevent load and supply currents from flowing near the input nodes. At Elantec, we use ground planes on both sides of a test fixture which are selectively connected at various points on the printed circuit board.

We also make extensive use of semi-rigid coaxial cable to route signals to and from a device under test. Stripline techniques can also be employed, but take longer to develop. We "breadboard" critical applications using double-sided copper clad board, hand cutting the ground plane to achieve optimum performance. The final production fixture usually employs a gold plated pattern identical to the "breadboard" which we have found eliminates subtle parasitic changes. For example, one such series of boards which was developed for frequency domain testing is flat to under 0.1 dB at frequencies in excess of 500 MHz. In the final analysis, most manufacturers offer "demo boards" for use with their products, and they are an excellent platform to initiate breadboard testing and a basis for your artwork.

Component Selection

Let's eliminate one component right off the bat. Don't use a socket particularly for SO packages. If you are compelled to offer removability, use pin jacks for DIP packages.

As suggested earlier, chip capacitors and resistors are best for high frequency applications. Metal film construction may be mandated in some applications, and it is, therefore, very prudent to ascertain a given resistor's self-inductance on an impedance bridge before using in production. Clearly, an inductive resistor used as a gain setting resistor is an invitation to disaster. Carbon film resistors with their leads cut to $1/16$ of an inch exhibit excellent high frequency characteristics.

Oscilloscope Probes

We have no quarrel with probes, but they do require matching and calibration, exhibit fairly high input capacitance, and grounding is always a problem. For example, the Tektronix P6137 10 MΩ probe recommended for use with 2465 oscilloscope exhibits an input capacitance of about 12 pF which translates to 37Ω at 400 MHz. The first thing to do is to throw away the alligator clip. Chassis mounting probe tip jacks such as the Tektronix part number 131-0258-00 can be soldered directly to ground plane, or alternatively, the Tektronix 013-0084-01 probe tip adaptor can be used in conjunction with a standard BNC coaxial connector. Lastly, remember there can be bandwidth or rise time contraction which results from "RMS-ing" the probe and instruments bandwidths.

At Elantec, we tend to "roll your own" scope and network analyzer probes as illustrated in Figure 9. The mismatch created by the 450Ω resistor is minimal, tpd skew is much, much less than 1 ns for equal lengths of coax, any gain ratio can be used assuming that the amplifier can drive the impedance, and capacitive loading is minimal.

Diagnostics and Conclusion

The frequency at which an amplifier is oscillating or peaking can, ironically, be a clue as to the cause. For example, if the amplifier is oscillating at several hundred Megahertz, the odds on bet is that the output stage whose transistors exhibit ft's in that range is the problem. If the load is capacitive, a snubber may be in order. Power supply bypassing problems also result in oscillations (or ring frequencies) in that range. If the oscillation is detectable on the power supply, the bypassing is inadequate. On the other hand, if the problem is at or close to the gain-bandwidth product, loop oscillations caused by input capacitance or source impedances is the likely culprit.

High speed analog applications stripped of their mystery are no more difficult to design or troubleshoot than precision circuits, for example. Follow a few simple rules, and when all else fails, call the vendor's Applications department.

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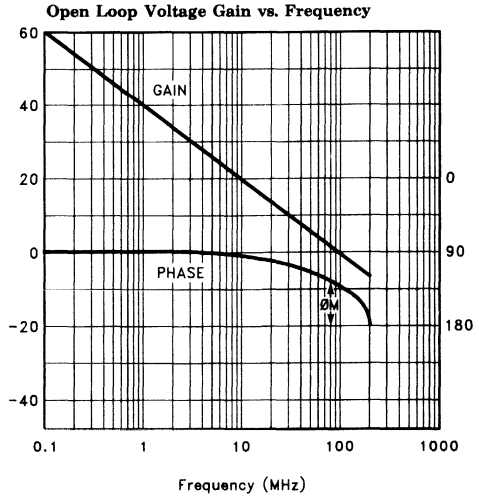


Figure 1. EL2041 Bode Plot

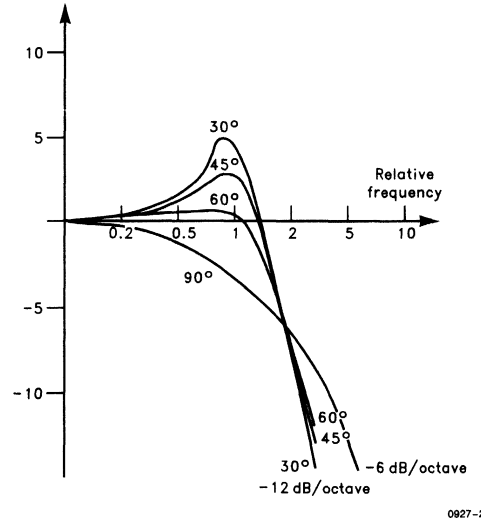


Figure 2. Normalized Gain for Various ϕM

High Frequency Amplifier Instability Tutorial #2

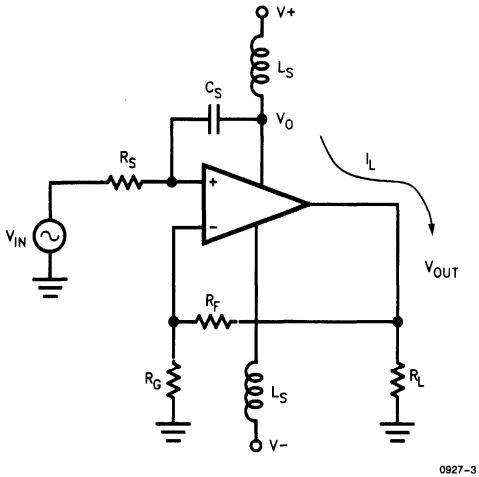


Figure 3. Power Supply Induced Oscillations

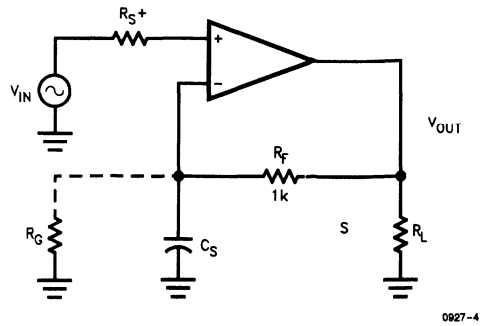


Figure 4. Source Impedance Effects

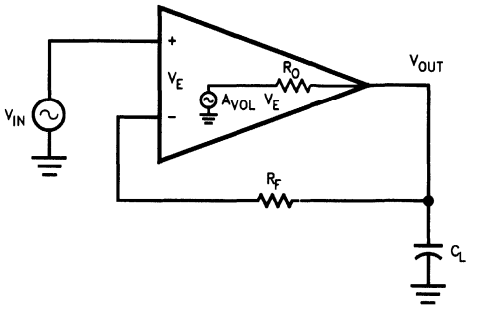


Figure 5. Capacitive Loads

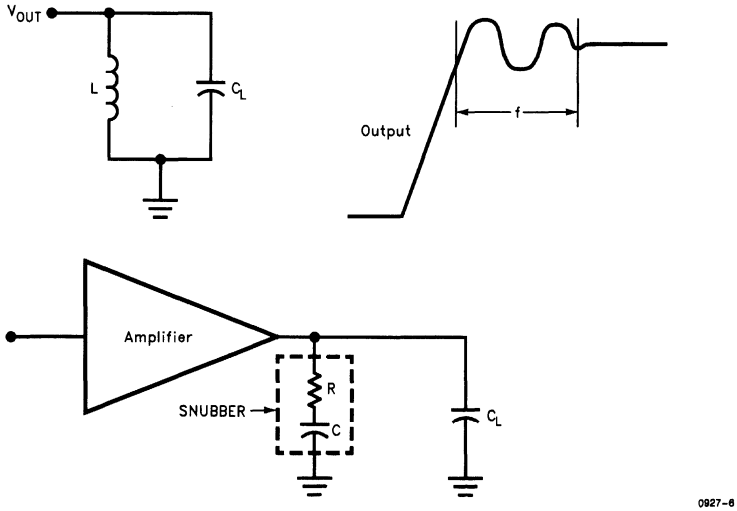


Figure 6. Snubbers

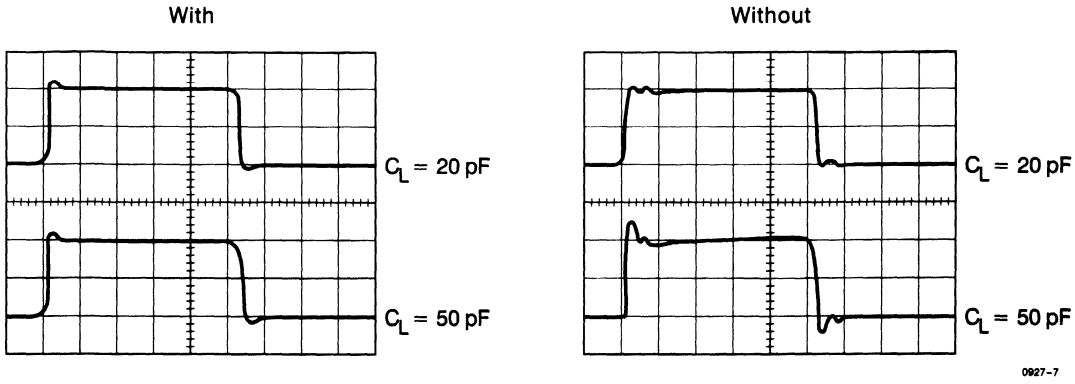


Figure 7. Response with and without a Snubber

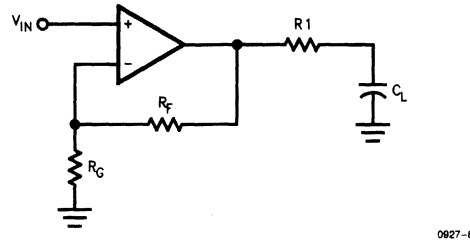
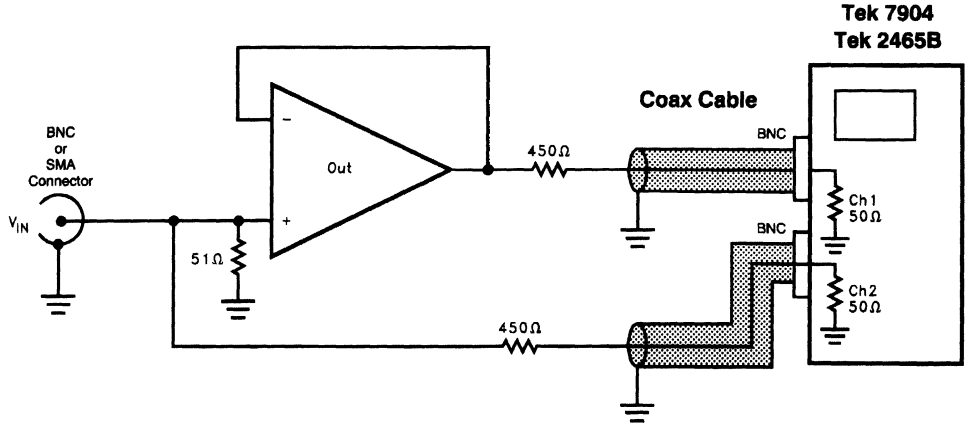


Figure 8. "Standard" Technique



Equal Length Coax, L ≤ 1M

Figure 9. Make Your Own Oscilloscope Probe

Practical Current Feedback Amplifier Design Considerations by Barry Harvey

The current-feedback (CMF) amplifier is a fundamentally different approach to high-frequency gain blocks. Not just an input stage, it is a full amplifier topology. It has outstanding characteristics in several areas: very high slewrates, −3 dB bandwidth which is almost constant with increasing circuit gain, and low high-frequency distortion. Almost all commercial CMF products offer these benefits, but, sadly they also exhibit limitations that are seldom publicized. This article is intended to point out the theoretical basis for the CMF amplifier's strengths and weaknesses, and some ways of coping with its problems.

Figure 1 shows the modern fundamental CMF circuit, with feedback applied through R_F to implement an operational voltage follower. Q1 through Q4 form a complementary buffer. The terminal called −Input is thus actually an output, a buffered replica of the voltage at +Input. Q3 and Q4 idle at a quiescent current proportional to the geometric mean of I1 and I2 and a scale factor dependent on the relative sizes of Q1 through Q4. When the feedback loop is at null, no error current will flow to the −Input, and Q3 and Q4 draw equal collector currents (we will ignore base current errors in this discussion). Q3's collector current is mirrored by Q8 and Q9 and delivered to the gain node. Q4's collector current is mirrored by Q5 and Q6 and sent to the gain node to balance against the previous mirrored current. Transistors Q11 through Q14 buffer the voltage at the gain node and present it as the output voltage.

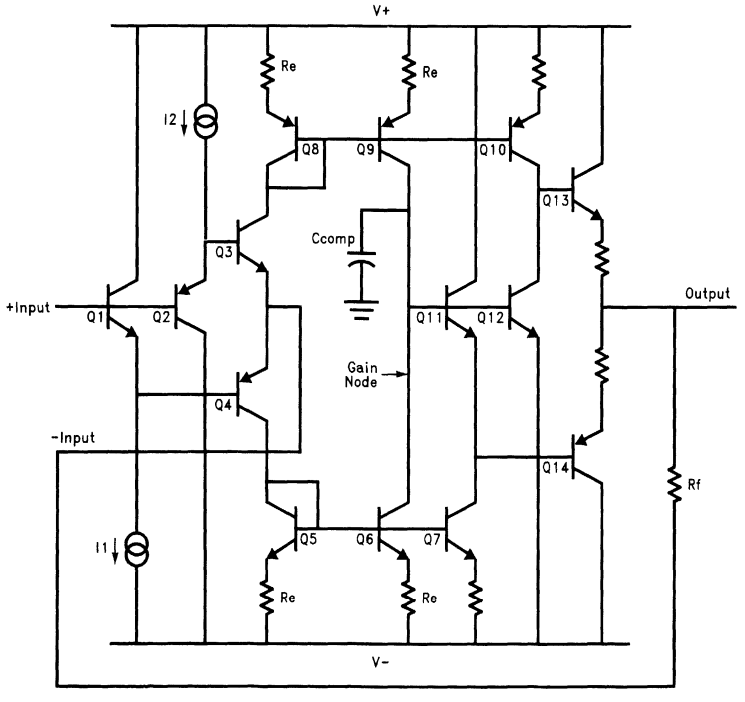


Figure 1. A Typical Current-Feedback Amplifier Connected as a Unity-Gain Follower

To understand the behavior of the circuit, imagine that the +Input and the output had been resting at zero volts and a one-volt positive step is delivered to the +Input. The input buffer Q1 through Q4 will very quickly replicate the step at the −Input terminal and the step voltage is thus impressed upon the feedback resistor R_F, since the output has not yet had time to move. Let us assume that R_F is 1 kΩ, a typical value. The one-volt step then will cause a transient one milliampere current to flow through R_F, increasing Q3's current by 500 μA and decreasing Q4's current by 500 μA. Q9's collector current will then increase by 500 μA and Q6's collector current will decrease by 500 μA, assuming the current mirrors have a gain of one. The milliampere of transient error current through R_F thus is transferred to the gain node of the amplifier and serves to slew the node positive, at a rate determined by C_{COMP}. The output, following the gain node, will move positive until equilibrium is reached where no current flows through R_F and currents to the gain node balance.

Slewrate

The output slewrate is the feedback current divided by C_{COMP}. If the input step were increased to two volts, twice the previous error current would flow through R_F and twice the slew current delivered to C_{COMP}, yielding twice the previous slewrate. Even if the error current through R_F exceeded the quiescent idle currents through Q3 and Q4, one of the two transistors would simply turn off and all error current would be delivered through the other transistor and associated current mirror in class A-B operation. In essence there is no slewrate limit in the conceptual CMF amplifier, and all step inputs produce the ideal single-pole exponential output response.

The high-frequency advantages of the CMF topology are manifold. The absence of slew limitation yields low distortion for large and high-frequency signals, even up to the normal small-signal bandwidth limitation. Since slew current is produced by the feedback error signal, the idle currents can be low without seriously affecting slew rate. And as we will see, the bandwidth is determined mainly by R_F and C_{COMP} and does not diminish rapidly with increasing closed-loop gain.

As in all circuits, there are limitations. We will consider time domain aberrations first. For increasingly large input steps and slewrates, the error current through R_F also increases. A fast 10V input step could produce a 10 mA peak error current, and this would not be supportable in many amplifiers. Typically, transistors in the current mirrors would saturate during the transient, causing slew and settling aberrations. Monolithic amplifiers support 500V/μs to 2000V/μs slewrates, but many devices display full-out step response that is "out of control". Saturation also occurs more readily at high temperatures, and takes longer to settle out, so amplifiers that seem to not exhibit saturation distortions at room temperature often do when hot.

The other slew distortion mechanism is input stage slew limitations. Q1 has an essentially unlimited positive slew capability, but its negative-going slewrate is limited by I1 and parasitic capacitance at Q1's emitter. Q2 similarly is not restricted in its negative-going slewrate, but I2 limits its positive slewrate. The result is that the replicated voltage presented at −Input is limited in each direction of slew by the respective current-source and parasitic capacitance. The maximum input slewrate might be less than the output slewrate (the slew allowed by the supportable error current from R_F mirrored to C_{COMP}), or it may be more. If the input slewrate is less than the output slewrate, −Input will "float" toward the new +Input voltage and the output will follow that slew-limited response.

Some CMF amplifier designs are simply not recommended for positive gain connections. These amplifiers are to be connected in inverting gain mode so that the +Input does not see signals at all. Their +Input is not a high impedance and does not offer good input slewrate.

This is the ultimate workaround to input stage limitations: connect the amplifier as an inverter.

This runs counter to most instrument designs, and as we will see, can often be inconvenient in many other ways. Fortunately, there are many CMF amplifier products designed to work well in the non-inverting mode.

Settling Behavior

With their large slewrates, one would expect the CMF amplifier to settle very quickly to high accuracies. This is only partly true; the CMF amplifier can settle very fast to moderate accuracies but displays large thermal settling tails. To see why this is true, consider the offset voltage between −Input and +Input. There is the difference of V_{be}(PNP) − V_{be}(NPN) at −Input relative to +Input. If we raise +Input by one volt, Q1 will dissipate less power since its V_{ce} was reduced, and V_{be}(NPN) will increase slightly as the transistor cools. Conversely, Q4 will gain a volt in V_{ce}, so its V_{be}(PNP) reduces as it warms. Unfortunately, the drift in V_{be}'s do not cancel. Note that these are *device* thermals; the device dissipates power just under its emitter in the collector region. The heat source is so physically small that it spreads and diminishes in a space smaller than the overall size of a transistor, and no device-to-device thermal coupling can be employed in an integrated layout to remove the effect.

To get an idea of the magnitude of the thermal settling errors, let us assume all transistors run at quiescent currents of 1 mA and that each device has a 70°C/W thermal coefficient. Each transistor changes dissipation by 1 mW, causing a 0.07°C temperature change. Since a silicon junction voltage changes by 1.7 mV/°C each device V_{be} changes 120 μV, for a total thermal error of 240 μV per volt of input. This 0.024% thermal error eliminates any concept of 0.01% settling, at least in positive-gain connections, and most CMF amplifiers are specified for 0.1% settling times instead. Figure 2 shows the settling response for an EL2020 to a 10V step in unity-gain connection. It settles very quickly to 0.1% bounds, 70 ns for a 10V step, but has a thermal input tail that pushes 0.01% settling much longer out.

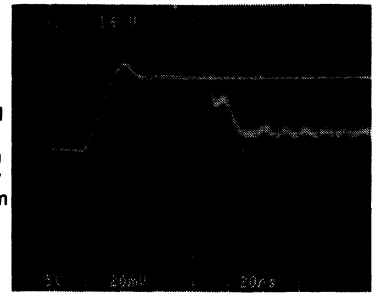


Figure 2. Short-Term Settling Characteristic of EL2020 (Unity Gain Mode)

Further settling aberrations can be generated as feedback current errors into the −Input terminal. The current errors are multiplied by R_F to contribute an output voltage error. Assuming the current mirrors have a unity gain, any current variation into the gain node has a direct contribution to the feedback error current. The main source of error current, as far as settling is concerned, is thermal error within the current mirrors. There are two popular topologies of CMF design where in one case the current mirrors add little to feedback current errors and in the other case their effect dominates all other settling errors. The simple two-transistor current mirrors Q5/Q6 and Q8/Q9 shown in Figure 3 is an example of the error-prone kind.

Settling Behavior — Contd.

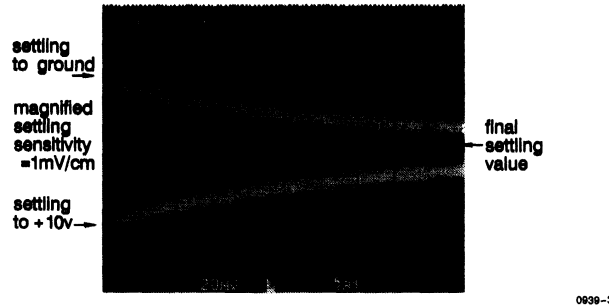


Figure 3. Long-Term Settling Tail of EL2020 (Unity Gain Mode)

Let us assume that R_F = 1 kΩ and Re = 300Ω. Assume the gain node and output voltage move by one volt in response to a signal. Further assume that Q6 and Q9 have 1 mA quiescent current and have a 70°C/W thermal coefficient. As in the previous thermal calculation, the volt of V_{ce} change across the transistors will cause a 0.07°C temperature change in the device, for a V_{be} change of 120 μV. The diode-connected transistors Q5 and Q8 do not share in this temperature change, so the V_{be} change, divided by Re = 300Ω, creates a 0.4 μA error into the gain node. This error is doubled and reflected as a current error into −Input. The 0.8 μA error, multiplied by R_F = 1 kΩ, yields an additional 0.08% thermal settling error.

This simple current mirror offers the widest bandwidth, greatest high-frequency linearity, most docile behavior for its bandwidth, and transient current capability, but much worse thermal errors than the more common Wilson type. Generally, CMF amplifiers whose transimpedance is greater than 150 kΩ have Wilson mirrors.

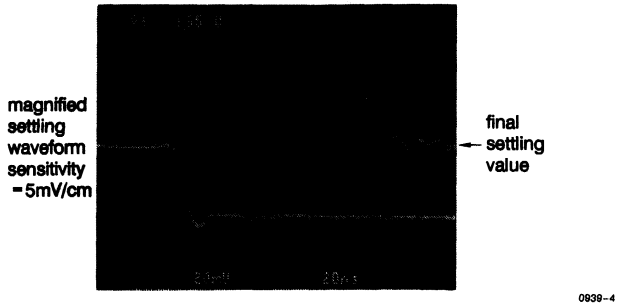


Figure 4. Short-Term Settling Characteristic of EL2020 (Inverting Gain of −1)

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Settling Behavior — Contd.

Figure 4 shows the settling response of the EL2020 connected in inverting mode (Av = −1). Because the input stage does not have to move with the signal, it does not add thermal error and only −Input error current limits settling quality. Although the 0.1% settling time is slowed to about 100 ns, the amplifier can now settle to 0.01% in 130 ns. As the figure shows, the settling tail reduced from the 0.024% size of Figure 2 to 0.007% in this connection.

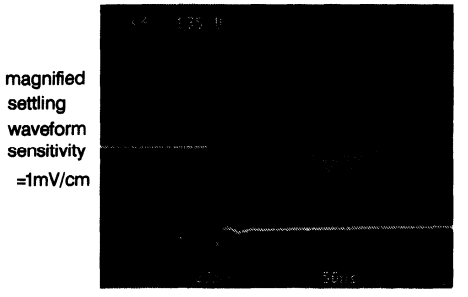

Figure 5. Magnified Short-Term Settling Characteristic of EL2020 (Inverting Gain of −1)

In any event, the CMF amplifier is still prone to load-driving thermal feedback effects. The input and current mirror stages are very hard to place on an IC so as to completely reject temperature changes on the die emanating from the output transistors. In general, if quality settling or best DC accuracy is desired, the CMF amplifier should be loaded as lightly as possible. 50Ω or 75Ω systems are poor choices for moving quality settling signals; direct device-to-device connection is best to avoid load-induced thermals.

Ultimately, the CMF is not the best choice for very high-accuracy settling, although it excels in the 8–10-bit realm. At 12-bit accuracy and above, properly designed traditional voltage feedback amplifiers dominate.

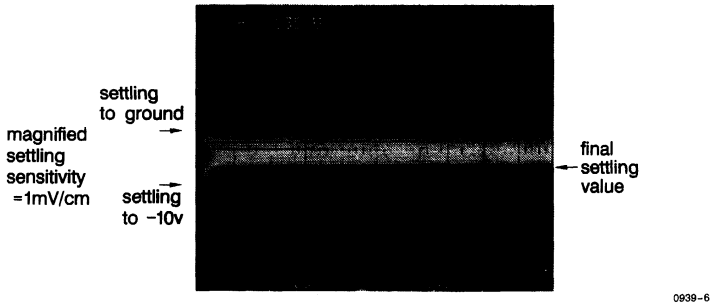

Figure 6. Long-Term Settling Tail of EL2020 (Inverting Gain of −1)

Gain Accuracy

Figure 7 shows the small-signal macro-model of a CMF, used in positive-gain connection. The input buffer presents a copy of the +Input to the −Input terminal, but has an output impedance of R_{IN}^-. The dotted line emanating from the side of the input buffer represents a connection to a current source whose value is a copy of the current flowing into −Input. This current is applied to the gain node, which is loaded at DC by R_{OL} and over frequency by C_{COMP}, the compensation capacitor. The external gain-setting resistors are the previous R_F and an added R_G. Finally, C_{IN}^- is the external parasitic capacitance at the −Input terminal.

The ideal gain of the fed-back amplifier is:

$$\frac{V_O}{V_{IN}} = \frac{R_F + R_G}{R_G}$$

which we will term A_0.

The precise expression for the fed-back gain is

$$\frac{V_O}{V_{IN}} = A_0 * \frac{1}{1 + \frac{R_F + A_0 * R-}{R_{OL}}}$$

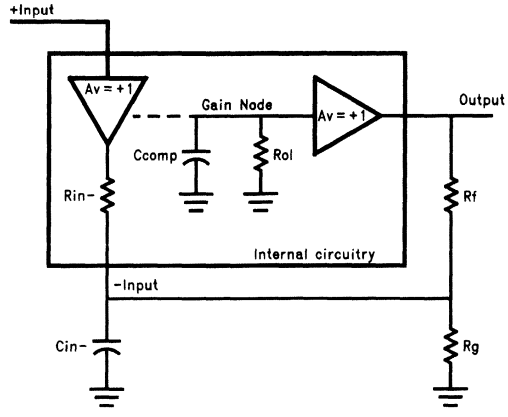

Figure 7. Small-Signal Equivalent Circuit of the Current-Feedback Amplifier

The added term is near unity since R_{OL} is a large number. This term is the gain accuracy expression as a function of amplifier characteristics and feedback resistors. The gain error can be approximated as

$$\text{Gain Error} = \frac{R_F + A_0 * R-}{R_{OL}}$$

There is no occurrence in the equations of A_{VOL}, the open-loop gain of the CMF amplifier. Actually, A_{VOL} is an "imaginary" parameter which is a holdover from voltage-feedback days and has no meaning with respect to the CMF amplifier. Unfortunately, few data sheets offer R−. R− can be estimated as

$$R- = \frac{R_{OL}}{A_{VOL}}$$

Gain Accuracy — Contd.

This is mathematically exact, but the typical R_{OL} and A_{VOL} numbers offered in data sheets may not give precise estimates of R−. For CMF amplifiers drawing supply currents around 16 mA, R− ranges from 10Ω to 25Ω; for lower currents around 8 mA, R− typically increases to 50Ω. Using R_{OL} = 1 MΩ, R− = 50Ω, and R_F = 1 kΩ, the gain error is 0.105% for unity fed-back gain and increases rapidly beyond a gain of 20. This is a key consideration in the CMF amplifier: gain accuracy is seldom as good as in most voltage-feedback amplifiers.

Furthermore, gain accuracy reduces with heavy output loading since the output buffer reflects the load as a reduction in R_{OL}. The CMF is seldom used for closed-loop gains of more than 50, since amplifier gain and the value of R_G become too small to retain gain accuracy.

On the other hand, the gain accuracy did not reduce appreciably between the closed-loop gains of 1 and 10. This gain range is the "sweet range" of CMF amplifiers. Note that this relatively limited gain accuracy does not suggest a non-linear situation; the CMF is much more linear open-loop than voltage-feedback amplifiers and does not rely on massive voltage gain to be linear in feedback.

This discussion of gain accuracy was based on open-loop gain; there are three subtle aberrations that make this value optimistic. The first effect is the input common-mode rejection ratio, or CMRR. This effect places an offset on −Input proportional to the signal level on the +Input terminal. The offset is indistinguishable from an input signal, and in non-inverting gain configuration creates a gain error. The typical CMRR for the CMF amplifier is 50 dB to 60 dB, so that gain error can be as poor as 0.3%.

The second gain error is due to voltage sensitivity in the −Input terminal's bias current. As the +Input terminal voltage moves with signal, early errors between Q3 and Q4 modulate their alphas and thus mismatch their quiescent collector currents. The mismatch in currents must be made up for as −Input bias current variation. The term for this effect is −ICMR. A −ICMR error, multiplied by R_F, creates an output error similar to CMRR errors. −ICMR quantities range from 0.2 μA/V to 10 μA/V. In our CMF amplifier example −ICMR would be around 1 μA/V. Using a 1 kΩ feedback resistor would create an output error of 1 mV/V, indistinguishable from a 60 dB CMRR input error in unity gain connection. The −ICMR error is an output error, and reduces in input effect as the overall fed-back gain is increased. For instance, a gain of +10 causes −ICMR errors to be ten times less significant.

The third such error source is the thermal settling error previously discussed. At frequencies below 1 kHz, the settling error is indistinguishable from CMRR or open-loop gain limitations. At frequencies above 100 kHz, however, thermal time responses are too slow to make appreciable errors, and gain accuracy can actually improve. The amplifiers will show a small drop in gain below these frequencies and a small increase in gain above. The variation in gain is about the same magnitude as the settling tail. Thus, the better-settling CMF amplifiers will show thermal errors too small to affect overall gain accuracy over (low) frequency, while the poorest-settling amplifiers can display as much as a 0.2% gain bump in mid-band frequencies.

Frequency Response

For the best gain accuracy, therefore, the inverting connection should be used. Ideal frequency response is calculated by inserting C_{COMP} in parallel with R_{OL}:

$$\frac{V_O}{V_{IN}} = A_0 * \frac{R_{OL}}{(R_{OL} + R_F + A_0 * R-) + s\,C_{COMP}\,R_{OL}\,(R_F + A_0 * R-)}$$

Frequency Response — Contd.

The −3dB bandwidth of this expression occurs at a frequency of

$$F_0 = \frac{1}{2\pi C_{COMP}(R_F + A_0 * R-)} * \frac{R_{OL} + R_F + A_0 * R-}{R_{OL}}.$$

The term on the right is quite close to unity for any CMF application and will be ignored. Since $A_0 * R-$ is usually much less than R_F, R_F dominates the expression for bandwidth over a wide range of closed-loop gain. This gives a bandwidth relatively independent of gain (or R_G), a major advantage for the CMF amplifier. The bandwidth falls to ½ of maximum when the gain is equal to $R_F/R-$, or 20 in our example.

This first-order analysis ignores the effect of $C_{IN}-$ and is an expression of what we will refer to as the "natural bandwidth" of the CMF amplifier. We will use the term natural instead of dominant pole because the pole is not completely dominant in every CMF design. The effect of $C_{IN}-$ is to insert a secondary pole in the frequency response of the circuit. This secondary pole usually coincides with the output resonance of both the input and the output buffers, and the overall frequency response is further complicated by phase delays in the current mirrors.

Figure 8 is a simulation of the frequency response of the idealized circuit of Figure 7 at unity gain with a variety of $C_{IN}-$ values, for a C_{COMP} of 3 pF. With a $C_{IN}-$ of zero, the frequency response is single-pole in nature and the −3dB bandwidth coincides with the "natural bandwidth". With increasing $C_{IN}-$, a high-frequency zero is introduced which tends to maintain gain over frequency. At a gain of +1, the zero caused by $C_{IN}- = C_{COMP}$ would potentially cancel the pole caused by C_{COMP} itself. Unfortunately, nature is not so generous and this is an unattainable trick.

Figure 9 shows the effect of $C_{IN}-$ on a realistic CMF model. The current mirrors and output stage were modeled as having 200 MHz single-pole bandwidths each, a realistic value in our example where the natural bandwidth is 50 MHz. The limited bandwidths of the mirrors and output stage cause $C_{IN}-$ to produce different abberations. $C_{IN}-$ still causes the bandwidth to expand, but at the expense of peaking. Peaking causes undesirable ringing in transient responses, and about 2dB of peaking is generally a gracious maximum. Only about 2.5 pF of $C_{IN}-$ can be tolerated for 2dB of peaking in our example, and this is a practical value. However, R_F and R_G must be connected directly to the −Input pin on the package to maintain so small a parasitic capacitance, and a socket is probably too capacitive to use.

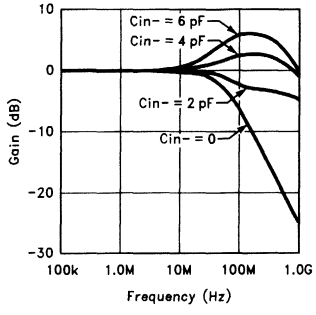

Figure 8. Ideal CMF Response with Various Values of C_{IN}

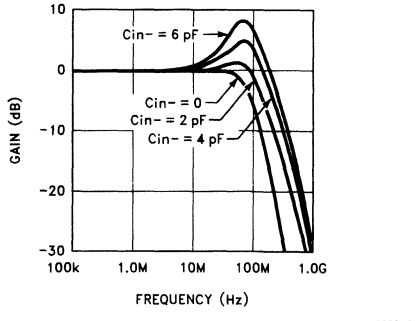

Figure 9. Realistic CMF Response with Various Values of $C_{IN}-$

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Settling Behavior

The small tolerated values of $C_{IN}-$ scale with the effective C_{COMP} of the CMF amplifier. Higher values of feedback resistor require smaller C_{COMP} for a given natural bandwidth and thus less $C_{IN}-$ can be tolerated. Since 1.5 pF is a minimum practical value for the parasitic $C_{IN}-$, almost no CMF designs use R_F values greater than 1.3 kΩ. Higher frequency amplifiers use R_F values around 300Ω to mitigate the $C_{IN}-$ problem.

As shown in Figure 9, our natural bandwidth of 50 MHz was expanded to a −3dB frequency of over 100 MHz. This design is typical for the moderate supply current devices; there is not enough quiescent current to maximize the current mirror and output stage bandwidths. Higher supply current amplifiers or amplifiers built from very high-frequency IC processes have more bandwidth in the mirrors and output stage and display less peaking for a given bandwidth and give more reproducible frequency responses. Our definition of "moderate" supply current will again be CMF amplifiers that draw about 8 mA–10 mA; optimized amplifiers draw around 16 mA.

The ratio of −3dB frequency to natural bandwidth is an interesting number. In high frequency circuits it is always greater than unity. The closer to unity this "Bandwidth Expansion" ratio is, the better-behaved the amplifier. That is, a ratio close to one makes the CMF more tolerant to $C_{IN}-$ and varying values of R_F, and it also makes the −3dB bandwidth at higher gains maximized. If the bandwidth ratio is high, say around 2, then the natural bandwidth of the amplifier is substantially lower than the unity-gain −3dB frequency, and the peaking which caused a −3dB bandwidth increase at unity gain fades and allows the more modest natural bandwidth to dominate the higher gains. Figure 11 shows this effect. The higher gains do not show peaking and the ideal bandwidth loss-vs.-gain relationship holds.

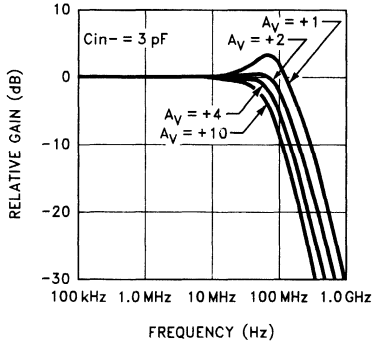


Figure 10. Realistic CMF Response with Various Closed-Loop Gains

The higher-gain bandwidths can be made closer to the unity-gain −3dB frequency by reducing R_F. The strategy is to make the quantity $R_F + A_0 * R-$ constant by reducing R_F as A_0 increases. In our example, the natural bandwidth was based on $R_F + A_0 * R- = 1050\Omega$. At a gain of +10, we could reduce R_F to 550Ω and obtain maximum −3 dB bandwidth

The Inverting Connection

When the CMF amplifier is configured as an inverting operational amplifier, as shown in Figure 11, the ideal gain in this configuration is

$$\frac{V_O}{V_{IN}} = -\frac{R_F}{R_G}$$

which we will term $-A_0$.

The precise expression for the fed-back gain is

$$\frac{V_O}{V_{IN}} = -A_0 * \frac{1}{1 + \frac{R_F + (A_0 + 1) * R-}{R_{OL}}}.$$

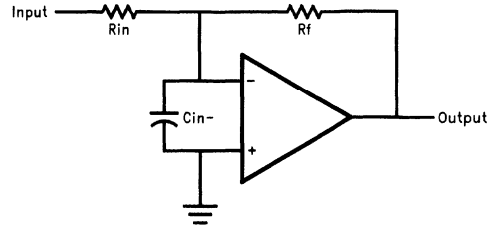


Figure 11. The CMF Connected as an Inverting Amplifier

The Inverting Connection — Contd.

The ideal gain error is close to that of the non-inverting case, and the ideal bandwidth also almost the same, with the A_0 term replaced by $(A_0 + 1)$. Because the amplifier inputs remain near ground as signals are passed, CMRR and −ICMR errors do not occur, and the ideal gain terms are maintained.

The inverting connection's input impedance is essentially R_{IN}. With $R_F = 1\ k\Omega$, a practical maximum gain for the inverting connection is about −20, since the input impedance drops to 50Ω. Even if the signal source could comfortably drive very low input impedances, simple interconnect inductances reduce bandwidths beyond 100 MHz. The practical maximum gain is even less for CMF amplifiers that use lower value feedback resistors.

Another virtue of the inverting connection is that the sensitivity to C_{IN}^- is substantially reduced. The inverting input is a virtual ground for low frequencies, and is a naturally low impedance R− at medium and high frequencies. Thus, the signal magnitudes are low at the inverting input and little current will flow into a C_{IN}^- to upset the ideal frequency response. Figure 12 shows our previous realistic CMF amplifier model's frequency responses with various values of C_{IN}^-. Note the reduced peaking from C_{IN}^-. With the flatter frequency response, the 0.1dB bandwidth improves, since the gain does not peak up and out of the ±0.1dB bound, as does the response of the non-inverting connection due to C_{IN}^-. The −3dB bandwidth is usually less than that of the non-inverting connection because of the diminished peaking.

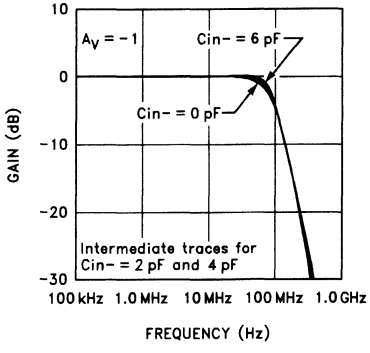


Figure 12. Inverting CMF Response with Various Values of C_{IN}^-

It must be remembered that the input and output impedances of the integrated amplifiers are quite complex over frequency. The terminals themselves can exhibit resonances with connected impedances independent of feedback. These resonances will be exhibited generally between one and five times the natural bandwidth of the CMF amplifier. For instance, few amplifiers tolerate load capacitance well. Those that can tolerate capacitive loading are designed to simply "wimp out" at high frequencies and lose gain accuracy and load-driving capacity. Many amplifiers do not like to see inductive or high input impedances, and some amplifiers built with very high-frequency processes resonate with $C_{IN}-$ even in the inverting mode. This term "resonance" can mean oscillation.

Noise

Noise performance of the CMF amplifier is characterized by four quantities, as shown in Figure 13. There is the typical input voltage noise V_n, generally placed in series with the +in terminal, the noises generated by R_F and R_G, and a noise current i_n which is peculiar to CMF amplifiers. This noise current is represented as being sent to the −in terminal from internal sources.

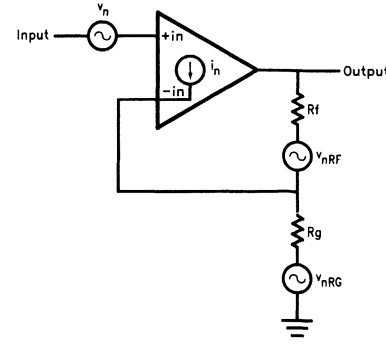


Figure 13. Noise Sources in a Positive-Gain CMF Amplifier

Practical Current Feedback Amplifier Design Considerations Tutorial #3

Noise — Contd.

For positive-gain connections, the noise contributions are so:

$$v_{in,total}^2 = v_n^2 + \left(\frac{4\,K\,T\,R_F}{A_V^2}\right) + \left(\frac{4\,K\,T\,R_G\,(A_V - 1)^2}{A_V^2}\right) + \left(\frac{i_{in}\,R_F}{A_V}\right)^2$$

Input-referred noise is in volts-squared per hertz here. K is the Boltzmann constant, and T is absolute temperature. The noise terms are, left to right, the −Input noise current, R_F resistor noise, R_G resistor noise, and input noise current. Note that all noise contributors except the input voltage noise itself reduce in magnitude as the gain A_V increases. Since R_G can be expressed in terms of R_F and A_v, we can simplify the expression:

$$v_{in,total}^2 = v_n^2 + \left(\frac{4\,K\,T\,R_F}{A_V}\right) + \left(\frac{i_n\,R_F}{A_V}\right)^2$$

CMF amplifiers have low values of v_n, ranging from 2 nV/$\sqrt{Hz}$ to 8 nV/$\sqrt{Hz}$. A 1 kΩ resistor has a thermal noise of 4 nV/$\sqrt{Hz}$, a value that can be neglected at even modest gains. The current noise has values ranging from 10 pA/$\sqrt{Hz}$ to 40 pA/$\sqrt{Hz}$. A CMF amplifier designed to use a 1 kΩ feedback resistor would convert a typical 20 pA/$\sqrt{Hz}$ noise current to a 20 nV/$\sqrt{Hz}$ voltage, the largest term in the expression until A_V is greater than about 3.

Figure 14 shows the input-referred noise versus A_V for two CMF designs. One amplifier uses a 1 kΩ feedback resistor, and has a 6 nV/$\sqrt{Hz}$ input noise. The other is designed for a 250Ω feedback resistor and has a 4 nV/$\sqrt{Hz}$ input noise. Both amplifiers have a 20 pA/$\sqrt{Hz}$ noise current. The first amplifier is typical of lower-power designs; the second typical of the fastest designs. Clearly, the higher supply-current amplifiers that use low-value feedback resistors are the quietest.

At low frequencies, in the audio region, v_n and i_n have 1/F excess noise. For v_n, the 1/F corner is typically around 200 Hz. For i_n, it is typically at 2000 Hz. These 1/F extra noise quantities do not typically increase the total integrated noise voltage much, due to the large bandwidth beyond the audio frequencies that the CMF amplifier has to accumulate thermal noise over, but they do prevent instrumentation-quality DC performance.

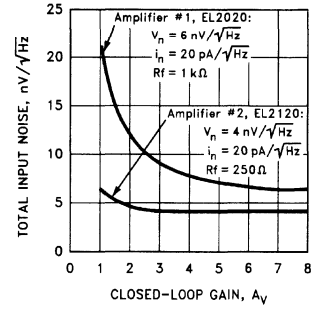


Figure 14. Noise vs Gain for Two CMF Amplifiers

Summary

The CMF amplifier has virtues unavailable in the traditional voltage-feedback design and it also has its own weaknesses. Enough variety exists among CMF products so that attention to individual amplifier characteristics is required to assure optimum circuit performance.

Dielectric Isolation

Introduction

In an integrated circuit, the individual transistors must be isolated from each other for correct circuit operation. In most IC processes, this is done by using reverse biased PN junctions and the technology is referred to as junction isolation (J.I.). The degree of isolation is limited by collector-substrate leakage currents and voltage modulated collector-substrate capacitance. An ideal isolation technology would not have leakage and capacitive coupling between devices.

Elantec uses a Dielectric Isolation (D.I.) bipolar process which differs radically from conventional bipolar J.I. processes in that the individual transistors are electrically isolated from their neighbors by a layer of glass. With the Elantec D.I. process, a layer of glass (SiO_2) surrounds the transistors on all four sides and the bottom. This totally isolates the individual transistors and provides essentially ideal isolation.

Dielectric Isolation (D.I.) is a way of building monolithic integrated circuits which have performance that rivals a multi-chip hybrid.

Elantec D.I. Process

Elantec uses D.I. to make both NPN transistors and PNP transistors in a high frequency vertical structure as shown in the figure. There are two collector, two base, and two emitter diffusions. Therefore, each transistor type can be optimized without compromising its complement. In analog circuit design, both NPN and PNP transistors are in the signal path. Thus the slower of the two transistors determines the overall circuit speed limitations. Most J.I. processes use lateral structure PNP transistors which have speed characteristics (f_t) that are 50 to 100 times slower than the NPNs. Thus most J.I. processes are 50 to 100 times slower than Elantec's D.I. process.

D.I. also has the capability of operating at a given high frequency with lower power consumption than conventional bipolar processes of similar geometry due to the reduced collector-substrate capacitance. These stray capacitances require extra supply current to charge them, supply current that is otherwise unnecessary in the circuit. Collector to substrate capacitances in D.I. are about one-tenth of those in J.I.

D.I. is an isolation technique and as such is a process technology platform which may be used as a starting point in more esoteric process development. Elantec's advanced D.I. process today uses implanted resistors, MOS capacitors, and Schottky diodes in addition to high performance, totally implanted complementary transistors. Other elements may be added such as BiFETS and thin film resistors. CMOS or even combined CMOS and bipolar (BiCMOS) can be implemented on D.I. In all cases, the D.I. lend its superb isolation, low leakage, and high-speed characteristics to the process.

Elantec's patented D.I. technology has been improved substantially from the original process. Performance and device density have been increased resulting in costs equaling that of standard J.I. Elantec's latest process has NPN and PNP Ft's of 4 GHz at 40 V, 2 micron CMOS and very low defect density.

D.I. Benefits

Speed

Speed is improved in D.I. integrated circuits for two reasons. First, since the collector substrate capacitance is smaller than J.I. by a factor of 10, the slew rate of an internal node can be 10 times as fast as the same node in J.I., using the same amount of current. Second, it is very difficult to build fast vertical PNP transitors with J.I., so most J.I. circuits settle for using a lateral PNP transistor somewhere in the signal path. With D.I., fully isolated fast vertical PNP and NPN transistors can be made on the same chip, and therefore performance need not be compromised by a slow transistor.

Temperature Performance

All junctions have leakage currents directly impacted by temperature. Higher temperatures create higher leakages. Many integrated circuits stop working if stray leakages between adjacent transistors are too high. Thus at high temperatures, these I.C.s cease working. With D.I., the

Dielectric Isolation Tutorial #4

high temperature leakages between adjacent transistors do not exist and the circuit can continue to work at high temperatures. Applications such as oil wells, where the temperatures may reach 200°C, are prime examples where D.I. is necessary for its temperature characteristics.

Radiation Hardness

The same leakages affected by temperature are also affected by radiation. The radiation may be from either a nuclear event or from deep space radiation. Because the D.I. glass layer is unaffected by radiation, the performance of D.I. circuits in the presence of radiation makes D.I. the mandatory technology for many military applications.

Freedom From Latch-up

Many J.I. devices are prone to latch-up. That is, under some external conditions the circuit will become stuck in a particular internal condition and will not function properly until the power is removed. Sometimes the circuit will self destruct due to latch-up. A key factor in this latch-up is the participation of the isolation junction in the circuitry that creates a parasitic SCR (Silicon Controlled Rectifier). In D.I., since there is no isolation junction, there can be no latch-up.

Elantec D.I. Advantages Over J.I.

- Speed

—Fast (vertical) PNP's and NPN's

—Lower Collector to substrate capacitance

—Collector to substrate capacitance not modulated by collector voltage

- No Possibility of Circuit Latch-up via Parasitic SCR's

—No parasitic devices with D.I.

- Operates in High Temperature and Radiation Environments

—Leakage currents are blocked by D.I. walls

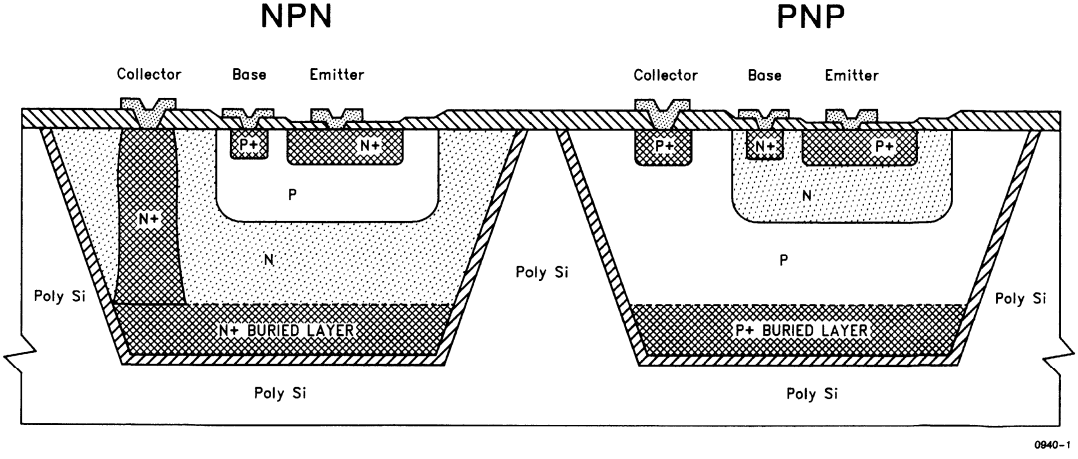
- High Voltage Operation

—Device to device breakdown >2000 V

- Mixed Technologies on Same Chip

—Bipolar transistors, diffused resistors and MOS can be done on the same monolithic chip

Elantec Complimentary D.I. Process



Applying Power MOSFET Drivers by Bruce Rosenthal

Overview

The EL7xxx series of high speed power MOSFET drivers achieve noteworthy improvements in speed, efficiency, input impedance, and functionality thru the application of advanced CMOS technology and novel circuit design. However, their ability to deliver high peak currents with rapid dv/dt's makes them susceptible to over stress. Recommended design practices will be discussed to assist the designer in achieving reliable operation.

Common Causes Resulting in MOSFET Driver Problems

Cause 1

CMOS Latch-up: Inherent to CMOS integrated circuitry, is a parasitic SCR which can be triggered by injecting current thru any input or output pad. This occurs whenever the input/output pins exceed the supply rails by more than 0.6V. This condition may exist for any one of the following reasons.

1. During the power up/power down sequence, when voltage is applied to an input without supply voltage.
2. Ground or V_{DD} "bounce" (relative to the input) during switching. This is often attributed to inductance in the current path.
3. Inductive kick-back from the output load.

Cause 2

Over-Voltage Spikes: Power line spikes will occur when a rapid change in current (typical during switching) is present on an inductive supply line. Exceeding the maximum supply voltage can rupture the internal transistor gate oxide, causing catastrophic failure.

Cause 3

Insufficient Overdrive: During switching, some ground bounce is going to occur. If the ground bounce is greater than the overdrive to the input, oscillation may result as the effective drive to the input is modulated. Since the typical input delay is only 20 ns, a slowly rising drive waveform will still be very close to the threshold when the output switches. The ensuing ground bounce may be enough to toggle the input.

Cause 4

Thermal Overload: The high peak drive capability of the Elantec power MOSFET drivers, far exceeds their continuous rating. Limited by the high thermal resistance associated with PDIP and SOIC packages, junction temperatures can exceed the 125°C rated maximum. Users should be aware of those factors which contribute to the total power dissipated, including quiescent current, conduction losses, and switching losses.

Guidelines for Improved Operation

The most important thing to remember in applying CMOS drivers is to minimize inductance to the power pins as illustrated in Figure 1.

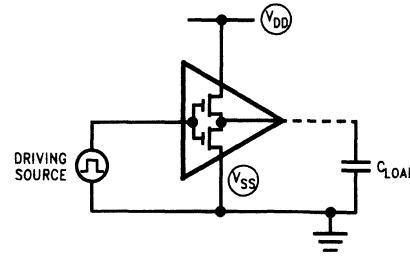


Figure 1. Trouble Prone Configuration

Applying Power MOSFET Drivers Tutorial #5

Guidelines for Improved Operation — Contd.

To prevent CMOS latch-up restrict the inputs/outputs from exceeding the power rails. This may require the use of clamping diodes, output snubbers, power supply bypassing and decoupling. Effective bypassing requires a minimum path length between capacitor and supply pins. Choose a capacitor with good high frequency characteristics, such as ceramic and/or tantalum construction. Refer to Figure 2.

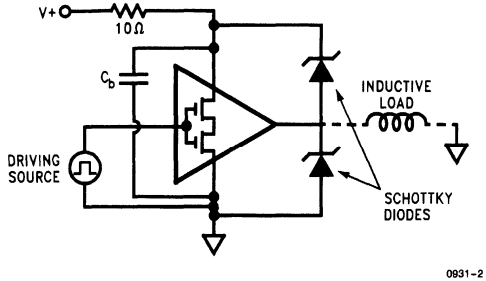
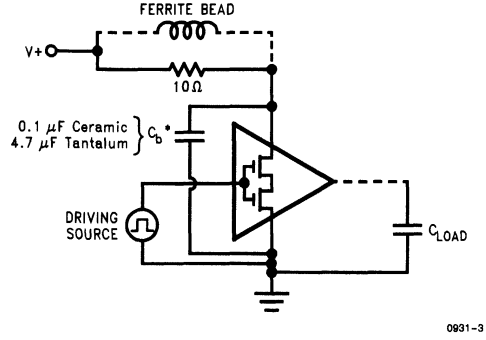


Figure 2. Suggested Configuration for Driving Inductive Loads

Overvoltage spikes can be controlled with decoupling. A small resistor (10Ω) from the supply, or a ferrite bead, followed by a 4.7 μF tantalum capacitor with short leads to the power pins is very effective. The suggested configuration is shown in Figure 3.



*C_b should be physically located close to the power pins.

Figure 3. Suggested Decoupling/Bypassing

Sensitivity to insufficient drive is most pronounced at supply voltages greater than 12V due to the higher internal peak currents. Where high supply voltage operation is required, 0V to 5V input drive is suggested, with a minimum rise/fall time of 200 ns.

Excessive power dissipation typically results when driving large capacitive loads at high frequencies. These losses are described by:

$$P = CV^2F \quad \text{where}$$

P = Power
C = Capacitance (Internal and External)
V = Supply Voltage
F = Clock Frequency

Internal dissipation can be reduced by adding an external resistor or inductor, as shown in Figure 4. Since the power varies as the square of the voltage, a reduction in supply voltage from 15V to 12V results in a 33% power savings.

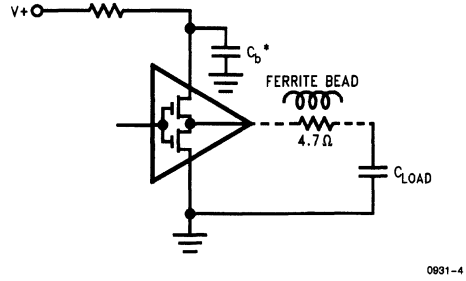


Figure 4. Reducing CV^2F Losses

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Glossary of Technical Terms

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HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

AC Coupled. AC coupling is a method of connecting a signal to any circuit in a way that removes the DC offset. The DC offset is the overall voltage level that the video signal "rides" on. One way to find the signal is to remove the DC offset by AC coupling, and then do a DC restore to add in a known DC offset (one that we selected). Another reason AC coupling is important is that it can remove harmful DC offsets.

Analog-to-Digital (A/D). This device is what all digital imaging systems use to get real-world pictures—from a TV camera, for example—into a computer. An A/D for digitizing video must be very fast, capable of sampling at clock rates of 10 to 30 million samples per second (MSPS).

Back Porch. The area of the composite video waveform following the horizontal sync pulse and right before the active video or before the terminating edge of horizontal blanking.

Bandwidth or 3 dB Bandwidth (BW, SSBW). A figure of merit of an amplifier or buffer which delineates the frequency at which the output is reduced to 0.707 (−3 dB) of the low frequency value when passing a small signal sine wave.

Black Burst. The video waveform without the active video part. Black burst is used to sync various video boxes together so that their video output is all aligned. Black burst tells the video gear the vertical sync, horizontal sync, and the chroma burst information.

Black Level. This level represents the darkest an image can get. This defines what black is for the particular image system. If for some reason the video dips below this level, it is referred to as blacker-than-black.

Blanking. On the screen, the scan line moves from the left edge to the right edge, jumps back to the left edge, and starts out all over again, on down the screen. When the scan line hits the righthand limit and is about to be brought back to the lefthand edge, the video signal is blanked so that one can't "see" the return path of the scan beam from the right to the lefthand edge. To blank the video signal, the video level is brought down to the blanking level, which may or may not be the black level if a pedestal is used. The vertical retrace is also blanked between fields.

Blanking Level. That level of the video waveform defined by the system to be where blanking occurs. This could be the black level if a pedestal is not used or below the black level if a pedestal is used.

Breezeway. The portion of the video waveform that sits between the end of the horizontal sync and before the start of burst.

Brightness. This is the intensity of the video level and refers to how much light is emitted by the display.

Burst Gate. This is a signal that tells the systems where the color burst is located within the scan line (video waveform).

Channel Separation (CHSp, CS). A figure of merit applicable to a dual, triple, or quad amplifier which specifies the ratio of the (spurious) output voltage of an undriven amplifier to the output of a driven amplifier.

Chroma Bandpass. In an NTSC or PAL video source the luma (black and white) and chroma (color) information are combined together. If you want to display an NTSC or PAL source, the luma and chroma must be split apart. The chroma bandpass filter removes the luma information from the chroma information, leaving the chroma information relatively intact. The NTSC or PAL video signal is fed into the chroma bandpass filter, where only a certain portion of the video signal is let through the portion containing the chroma information. This works reasonably well except in certain images where the luma information and chroma information overlap, meaning that we have luma and chroma information at the same time.

Glossary of Terms

Chrominance. The NTSC or PAL video signal contains two pieces that make up what you see on the screen: the black-and-white part, and the color part. Chrominance is the color part—a.k.a. chroma.

Clamp. This is basically another name for the DC-restoration circuit. It can also refer to a switch used within the DC-restore circuit. When it means DC restoration, then it's usually used as "clamping." When it's the switch, then it's just "clamp."

Closed Loop Gain (Avcl, Av). The ratio of the output voltage to the input voltage for an amplifier which is established with feedback using one or more resistors. The non-inverting closed loop gain is given by:

$$Av = \frac{Rf}{Rg} + 1$$

where: Rf = The feedback resistor (output to $V_{IN}-$)

Rg = The gain setting resistor ($V_{IN}-$ to ground)

Inverting closed loop gain is given by:

$$Av = \frac{Rf}{Rg}$$

Color Bars. This is a test pattern used to check whether a video system is calibrated correctly. A video system is calibrated correctly if the colors are the correct brightness, hue, and saturation. This can be checked with an oscilloscope and vector scope in the NTSC space, or by looking at the RGB levels in the RGB space.

Color Burst. Often referred to as "burst." That portion of the video waveform that sits between the breezeway and the start of active video. It tells the color decoder in the receiver how to decode the color information contained in the next line of active video. By looking at the burst, the receiver can determine what's blue, orange, or magenta. Essentially, the receiver figures out what the correct color is.

Color Decoder. This is the circuit in the video system that uses the chrominance portion of NTSC/PAL to derive the two color difference signals. The color decoder sits right after the Y/C split and before the color space convertor. The color decoder needs a 3.58 MHz signal that is accurately phase locked (PLL) to the burst. If it isn't locked well enough, then the color decoder can't figure out the right colors.

Color Encoder. The color encoder does the exact opposite of the color decoder. It takes the two color difference signals, such as I and Q in the NTSC system, and combines them into the chroma signal. The color encoder, or what may be referred to as the color modulator, uses the color subcarrier to do the encoding.

Common Mode Rejection Ration (CMRR). A figure of merit of an amplifier or buffer which delineates the ratio of the change in input common mode voltage (peak to peak) to the change in input offset voltage (peak to peak) usually specified over the common mode range of the device.

Common Mode Range or Input Voltage Range (CMIR, CMR). A figure of merit of an amplifier, buffer, or comparator which delineates the range of the input common mode voltage relative to the power supply voltage beyond which the device will malfunction. This parameter is often "specified" implicitly by CMRR by use of a specific common mode voltage.

Common Mode Voltage (Vcm). The average of the voltages applied to the inputs of a differential input amplifier. In the case of an operational amplifier, the feedback loop strives to make the inverting input equal to the non-inverting input, and the common mode voltage is essentially equal to either input.

Composite Video. If a video system is to receive video correctly, it must have several pieces of the puzzle in place. It must have the picture that is to be displayed on the screen, and it must be displayed with the correct colors. This piece is called the active video. The video system also needs information that tells it where to put each pixel. This is called sync. The display needs to know when to shut off the electron beam so the viewer can't see the spot retrace across the display. This piece of the video puzzle is called blanking. Now, each piece could be sent in parallel over three separate connections, and it would still be called video and would still look good on the screen. This is inefficient, however, because all three pieces can be combined together so that only one connection is needed. Composite video is a video stream that combines all of the pieces required for displaying an image into one signal, thus requiring only one connection. NTSC and PAL are examples of composite video. Both are made up of: active video, horizontal sync, horizontal blanking, vertical sync, vertical blanking, and burst. RGB is not an example of composite video, even though each red, green, and blue connection may contain composite sync, because all three conections are required to display the picture with the right colors.

Contrast. A video term referring to how far the whitest whites are from the blackest blacks in a video waveform. If the peak white is far away from the peak black, the image is said to have high contrast. With high contrast, the image is very stark and very "contrasty." If the two are very close to each other, the image is said to have poor, or low, contrast. With poor contrast, an image may be referred to as being "washed out"—you can't tell the difference between white and black, and the image looks gray.

Cross Conduction. A common problem in half bridge and full bridge topologies resulting in extra current flow between the upper and lower transistors during switching. This occurs when the turn-off of one transistor overlaps the turn-on of the alternate transistor.

Cross Talk (CT). See Channel Separation.

Current Feedback Amplifier (CFA). A type of operational amplifier wherein the inverting input impedance is low and is a buffered version of the voltage at the non-inverting input. A feedback resistor is always required (even when a CFA is used as voltage follower). CFA's offer very high slew rates, high frequency linearity, and exhibit bandwidths which are substantially independent of closed loop gain.

dV/dT. The change in voltage relative to time.

di/dT. The change in current relative to time.

DAC. DAC is short for digital-to-analog convertor.

DC Restoration. DC restoration is what you have to do to a video waveform after it has been AC coupled and has to be digitized. Since the video waveform has been AC coupled, we no longer know absolutely where it is. In fact, not only don't we know where it is, it also changes over time, since the voltage level of the active video changes over time. Since the resistor ladder on the flash A/D is absolutely tied to a pair of voltage references, the video waveform needs to be referenced to some known DC level in order to digitize it correctly. DC restoration is essentially putting back the DC component that was removed to make an AC coupled signal. In trying to digitize video, the DC level that we DC restore to is such that the back porch, or the blanking level if a pedestal is present, is set to the A/D's $-V_{REF}$ DC level. Therefore, when black is digitized it will be assigned the number zero and when peak white is digitized, it will be assigned the number 255, in an 8-bit system.

Glossary of Terms

Decoder. The word "decoder" has several meanings:
Color Decoder. See definition under Color Decoder.
Image Compression Decoder. This is the part of an imaging system that takes the compressed image and restores it to look like the original.

Differential Gain (dG). A figure of merit of an amplifier or buffer that relates the incremental change in closed-loop gain resulting from a change in input and output voltage referenced to zero volts for a specific frequency. The gain of most amplifiers is not constant with varying DC offsets added to a constant frequency AC input signal. The parameter is most useful in applications of composite video signals and is usually expressed in percent. A standard measurement condition is for input offsets which are changed from zero to ±0.714V with an input signal of 100 mV at 3.58 MHz for NTSC and 4.43 MHz for PAL.

Differential Phase (dP). A figure of merit of an amplifier or a buffer that relates the incremental change in closed-loop phase resulting from a change in input and output voltage referenced to zero volts for a specific frequency. The phase shift through an amplifier is not completely constant with varying DC offsets added to a constant frequency AC input signal. The parameter is most useful in applications of composite video signals and is usually expressed in degrees. A standard measurement condition is for input offsets which are changed from zero to ±0.714V with an input signal 100 mV at 3.58 MHz for NTSC and 4.43 MHz for PAL.

Disable Time (t_{dis}, t_{off}). Some amplifiers provide a logic pin which enables and disables the amplifier. Usually, the supply current is reduced and the output stage is placed at a high impedance when disabled. Disable time is defined as the time from the edge of the disabling pulse to the time that the output of the amplifier falls to 50% of the pre-disabled value.

Enable Time (t_{dis}, t_{off}). Some amplifiers provide a logic pin which enables and disables the amplifier. Usually, the supply current is reduced and the output stage is placed at a high impedance when disabled. Enable Time is defined as time from the edge of the enabling pulse to the time that the output of the amplifier has increased to 50% of its final (non-disabled) value.

Encoder. As with decoder, there are two meanings to this word:
Color Encoder. See definition under Color Encoder.
Image Compression Encoder. This is the part of the imaging system that takes the original image and squeezes out redundant information so that the image will take up less space than before.

Equalization Pulses. These are two groups of pulses, one that occurs before the serrated vertical sync and another group that occurs after. These pulses happen at twice the normal horizontal scan rate. The reason these pulses exist are to ensure the 2:1 interlacing of the NTSC or PAL systems. (See "field.")

Fade. Fading is a method of switching from one video source to another video source.

Fall Time (tf). See Transient Response Time.

Field. A TV screen is made using two fields, each one containing half of the scan lines needed to make up one frame of video. One field contains the even-numbered scan lines while the other field is made up of the odd-numbered scan lines. Each field is displayed in its entirety-therefore, all of the odd-numbered scan lines are displayed, then the even, then the odd, and so on.

Fields only exist for interlaced scanning systems such as NTSC or PAL. So for NTSC, which has 525 lines per frame, a field has 262½ lines, and two fields make up a frame.

Filter. In general, a filter is used to remove unwanted information from the input signal. Every signal has a spectrum, which is the amount of different frequencies contained within the signal. Filtering lets you subtract or "filter" out certain frequencies. If you have some high-frequency information, such as noise, in with the signal that you really want, then a low-pass filter is used. A low-pass filter "passes" frequencies below a certain point and stops frequencies above that same point. A high-pass filter does just the opposite—it stops low frequencies and passes the high frequencies. A bandpass filter lets through frequencies within a certain range of "band," but stops frequencies outside of the band.

Flash A/D. This is a really fast method for digitizing a signal. The signal to be digitized is provided as the source for one input of a whole bank of comparators. The other input is tied to a tap of a resistor ladder, with each comparator tied to its own tap. This way, when the input voltage is somewhere between the top and bottom voltages connected to the ladder, the comparators output a code. This means that all the comparators output a "yes" up to the input voltage and a "no" above that. The A/D then takes this string of Yes's and No's and converts them into a binary number which tells where the Yes's turned into "No's." See the definition of resistor ladder for more details, if you're interested.

Flicker. Flicker occurs when the frame rate of the video is too low.

Front Porch. This is the area of the video waveform that sits between the start of horizontal blank and the leading edge (start of) horizontal sync.

Full Bridge. Two half bridges. (See Half Bridge.)

Gain Bandwidth Product (GBW). The frequency where the open loop gain of a voltage feedback amplifier falls to one (0 dB). Sometimes the Gain is measured at a frequency lower than the one at which the gain is equal to unity. The product of the measured gain at the test frequency is then cited as GBW on the data sheet.

Gain Flatness (GFP, GFR). A figure of merit of an amplifier that delineates the closed loop deviation of the gain over a range of frequencies. It is an expression of how constant the response of an amplifier or network is over a specified range of frequencies.

Gate Oxide. The dielectric between the channel and control gate of an mos transistor.

Genlock. A video source provides all of the information necessary to view—or in the case of a computer, grab—the picture. This includes the information from the scene itself, color decoder information, and synchronization information so the receiver knows where to put the picture. When a computer is involved, it has its own sync signals that are running independently of the sync signals sent by the camera. Genlocking is the act of getting the computer's sync signals to line up with the camera's sync signals. The sync signals from the camera and the computer must be locked together if the picture from the camera is to be shown correctly on the computer's screen. This is performed by a genlock circuit. A genlock circuit may employ several techniques to do its job, with the most popular being a phase locked loop.

Glossary of Terms

Half Bridge. A circuit topology consisting of an upper transistor going to V_{DD}, a lower device going to V_{SS}, and a common node in between.

Horizontal Scan Rate. This is how fast the scanning beam in a display or a camera is swept from side to side. In the NTSC system this rate is 63.556 μs, or 15.734 kHz.

Horizontal Sync. This is the portion of the composite video signal that tells the receiver where to place the image in the left-to-right dimension. The horizontal sync pulse tells the receiving system where the beginning of the new scan line is.

Hysteresis. Positive feedback applied to increase noise immunity by varying the switch point depending on which state the device is in.

Input Bias Current (Ib, I_I, Ib+, Ib−). A figure of merit an amplifier, buffer, or comparator which delineates the input currents of the amplifier under linear (normal) operating conditions. Input bias current is often the average of the two input currents and may be sensitive to the common mode input voltage.

Input Impedance (R_{IN}). A figure of merit of an amplifier, buffer, or comparator which delineates the ratio the change in input voltage to the change in input current. In general, voltage feedback amplifiers and comparators exhibit high input impedance at both the inverting and non-inverting inputs, but current feedback amplifiers exhibit low input impedance at the inverting input by design. Users should be aware that the "Input Impedance" is a DC figure of merit and that, in general, there is an input capacitance as well in parallel with the input impedance. The inverting input of a Current Feedback Amplifier can also appear to be inductive.

Differential Input Impedance applies to amplifiers with differential inputs and is measured by applying a small differential voltage to the inputs while measuring the change in bias current.

Input Noise Voltage ($\overline{en}$). A figure of merit of an amplifier, or buffer that delineates the average noise voltage referred to the input under specific operating conditions. Usually, a curve of the noise characteristics is presented in the typical performance curves of the data sheet. A simple way of thinking of noise is to consider it "AC" offset voltage which dictates the overall system accuracy and the minimum signal which can be resolved. The noise source is often modeled as noise generator in series with one of the (differential) inputs of the amplifier.

Input Noise Current ($\overline{in}$). A figure of merit of an amplifier or buffer that delineates the average noise current at the inputs. Since the noise current usually flows through resistors in a typical application, it is converted to a noise voltage referred to the input. It is usually modeled as a current source from each input to ground.

Input Offset Current (I_{OS}). A figure of merit of an amplifier or comparator which delineates the difference in the currents into or out of the input terminals when the output is zero for an amplifier or to a specified output voltage for a comparator.

Input Offset Voltage (V_{OS}). A figure of merit of an amplifier or comparator which is the voltage that must be applied to the inputs of an amplifier to make the output zero or the output of the comparator a specified voltage.

Input Resistance. See Input Impedance.

Large Signal Voltage Gain (A_{VOL}). An open loop figure of merit for an amplifier or comparator which is the ratio of the output voltage to the change in input voltage required to move the output from zero volts to the specified voltage.

Latch-up. Results from parasitic action of the scr in CMOS circuits.

Locked. When one signal is synchronized to another by feedback, usually using a PLL.

Loop Gain. The difference between the open loop gain and closed loop (noise gain) of the circuit.

Luminance. As mentioned in the definition of chrominance, the NTSC and PAL video systems use a signal that has two pieces: the black-and-white part, and the color part. The black-and-white part is the luminance. It was the luminance component that allowed color TV broadcasts to be picked up by black-and-white TVs and still remain viewable.

Monochrome. A monochrome signal is a video source having only one component of color.

NTSC. An abbreviation for National Television Standards Committee.

Open Loop Transimpedance (R_{OL}). A figure of merit for a Current Feedback Amplifier which delineates the ratio of the change in output voltage to the change in current of the inverting input. R_{OL} is similar to Large Signal Voltage Gain, A_{VOL}, of a voltage feedback operational amplifier and is usually expressed in megohms.

Output Current (I_{OUT}). A figure of merit of an amplifier or buffer which delineates the current that can be sinked or sourced by the device under linear operating conditions.

Output Impedance (R_{OUT}). A figure of merit for an amplifier for a buffer or an amplifier which delineates that ratio of the change in output voltage to the change in output current usually for a specific load (R_L) and source (R_S) resistance. In general, output impedance for an amplifier is not particularly meaningful since the open loop output impedance is reduced by the loop gain of the amplifier. The output impedance for an (open loop) buffer, on the other hand is very meaningful in that, to the first order, it dictates the voltage gain of the device for a given load resistance (R_L).

Output Resistance. See Output Impedance.

Output Voltage Swing (V_{OUT}). A figure of merit of an amplifier which delineates the voltage that can be obtained from the device under linear conditions without clipping.

Offset Voltage Drift (dV_{OS}/dT or TCV_{OS}). A figure of merit of an amplifier, buffer, or comparator which delineates the average change in input offset voltage due to thermal effects over the specified operating temperature range of the device. It is often expressed in μV per degree Centigrade.

Overshoot (OS). A figure of merit of an amplifier or buffer which delineates the departure from the output from the final value usually on the rising or falling edge under small signal closed loop conditions.

PAL. PAL stands for Phase Alternate Line and PAL is to Europe as NTSC is to North America and Japan. In other words, PAL is the video standard used in Europe and a few other countries. There are a few differences. PAL uses 625 lines per frame while NTSC has 525 lines. Therefore, PAL has higher resolution. The frame rate of NTSC is 60 fps while for PAL it is 50 fps. This means the update rate for NTSC is higher and therefore there is more flicker with PAL. PAL uses the YUV color space while NTSC uses YIQ. PAL alternates the phase of every line color. The color-phase sequence of the chrominance signal is periodically reversed to cancel out hue errors. It is becoming increasingly important for imaging systems suppliers to produce equipment that can be sold worldwide without many manufacturing difficulties.

Peak White. Peak white is the highest point in the video waveform that the video level can reach and still stay within spec. If for some reason the level does become greater than peak white, it's referred to as whiter-than-white.

Glossary of Terms

Pedestal. Pedestal is an offset used to separate the active video from the blanking level. When a video system uses a pedestal, the black level is above the blanking level by a small amount. When a video system doesn't use a pedestal, the black and blanking levels are the same.

Phase Margin. A figure of merit of an amplifier that delineates the difference between the phase of the output voltage and 180 degrees when the gain is one.

Pixel Clock. The pixel clock is used to divide the incoming horizontal video into pixels. This pixel clock has to be stable (a very small amount of jitter) relative to the incoming video or the picture will not be stored correctly. The higher the frequency of the pixel clock, the more pixels that will appear across the screen.

Power Supply Rejection Ratio (PSRR). A figure of merit of an amplifier, buffer, or comparator that delineates the ratio of the change in input offset voltage to the change in power supply voltage producing it.

Rails. Refers to the positive and negative supplies.

Response Time (tpd). A figure of merit of a comparator that delineates the time between the application of input step and the time that the output crosses a specified logic threshold.

Retrace. Retrace is what the electron beam does when it gets to the righthand edge of the display to get back to the lefthand edge. Retrace happens during the blanking time.

Rise Time (tr). See Transient Response Time.

S-VHS. S-VHS is an enhancement to regular VHS. S-VHS provides better resolution and less noise than VHS. S-VHS requires the luma and chroma components to be separate inputs to the VCR, while standard VHS only requires the compositie NTSC signal. That's one of the reasons for the improved quality. S-VHS doesn't combine the luma and chroma so they don't have to be split apart. In the world of electronics, any time you combine two signals together, generally the two signals are degraded somewhat after you split them back out.

Saturation. Saturation is the amount of color present. For example, a lightly saturated red looks like pink, while a fully saturated red looks like the color of a red crayon. Saturation does not mean the brightness of the color, just how much "pigment" is used to make the color. The more "pigment," the more saturated the color is.

Scan Line. A scan line is an individual sweep across the face of the display by the electron beam that makes the picture.

Secam. This is another TV format similar to PAL. The difference between the two is that in secam, the chrominance if FM modulated.

Serration Pulses. Serration pulses appear in the broad vertical sync pulse interval at a 2H line rate in order to maintain H-lock during vertical retrace.

Settling Time (ts). A figure of merit of an amplifier or buffer that relates the time between the initiation of an input step to the time that the output voltage has settled to a specified error band. If the output is ringing, the last reentry into the settling bound is defined as the end of the settling event. Settling time is usually a function of the input step size.

Shoot-Thru. Same as Cross Conduction.

Skew (clock). When two complementary signals have unbalanced delay.

Slew Rate (SR). A figure of merit of an amplifier or buffer which delineates the ability of the amplifier to accurately follow a large input step voltage. It is usually measured from the 20% to 80% point (and vice versa) of the output wave form.

Super Invertor. A circuit configuration which minimizes cross conduction.

Supply Current (Is, I_{CC}, I_{EE}, Is+, Is−). A figure of merit of an amplifier, buffer, or comparator that delineates the current required from the power supplies to operate the device with no load and the output at zero volts.

Sync. Sync is a fundamental piece of information for displaying any type of video. Essentially, the SYNC signal tells the display where to put the picture. The horizontal sync, or HSYNC for short, tells the display where to put the picture in the left-to-right dimension, while the vertical sync (VSYNC) tells the display where to put the picture from top to bottom.

Sync Generator. A sync generator is a circuit that provides sync signals. A sync generator may have a genlock input, or may not.

Sync Noise Gate. The sync noise gate is used right before the sync stripper to define an area within the video waveform where the sync stripper is to look for the HSYNC pulse. Anything outside of this defined window will be rejected by the sync noise gate and won't be passed on to the sync stripper. The main purpose of the sync noise gate is to make sure that the output of the sync stripper is nice, clean, and correct.

Sync Stripper. A composite video such as RS-170, NTSC or PAL contains the video information, which is the picture to be displayed, and information that tells the receiver where to put this video information on the display. The latter piece of information is called sync. A sync stripper pulls out the sync information from the composite video waveform and throws the rest away.

Transient Response Time (tr, tf). A figure of merit of an amplifier or buffer that delineates the closed loop response of the output of an amplifier in response to a small signal step input. Rise Time (tr) is usually specified from the 10% to the 90% point of the output and refers to the positive going edge; whereas Fall Time (tf) refers to the negative going edge of the output (or from 90% to 10%).

Unity Gain Bandwidth. A figure of merit of an amplifier that delineates the frequency where the amplifiers Large Signal Voltage Gain, A_{VOL}, has rolled off to unity. For amplifiers that are unity gain stable, the unity gain bandwidth and Gain Bandwidth product are identical, but decompensated amplifiers often specify Gain Bandwidth Product at frequencies that are below the point where the amplifier's A_{VOL} is one.

Vertical Sync. This is the portion of the compositie video signal that tells the receiver where the top of the picture is.

Video Mixing. Video mixing is taking two independent video sources and editing them together to create a new, third video source. This can be done by fading from a one source to the other.

Glossary of Terms

Video Waveform. The video waveform is what the signal "looks" like to the receiver or TV. The video waveform is made up of several parts that are all required to make up a TV picture that can be accurately displayed. Each component is necessary.

White Level. This level represents the lightest an image can get, and defines what white is for the particular image system. By calibration, this is the highest video level allowed in the system. If for some reason the video goes above this level, it is referred to as "whiter-than-white."

Y/C. The Y/C designation is shorthand for luminance and chrominance. You will also see this term used in the description of the S-VHS video tape format. The S-VHS format records the luma and chroma separately while standard VHS records them together.

Y/C Split. A Y/C splitter circuit is what's used in a TV set or imaging device to pull the luminance and chrominance apart in an NTSC or PAL system. This is the first thing that any NTSC or PAL receiver must do. The composite video signal is first fed to the Y/C splitter so that the luma and chroma can then be decoded further. The two popular methods for implementing a Y/C split are a chroma bandpass/chroma trap combo or a comb filter arrangement.

YIQ. YIQ is the color space used in the NTSC color system. The Y component is the black-and-white, (luma) portion of the image. The I and Q parts are the color components placed over the black-and-white, or luma, component.

YUV. YUV is the color space used by the PAL color system. As with the YIQ colorspace, the Y is the luma component while the U and V are the color components.